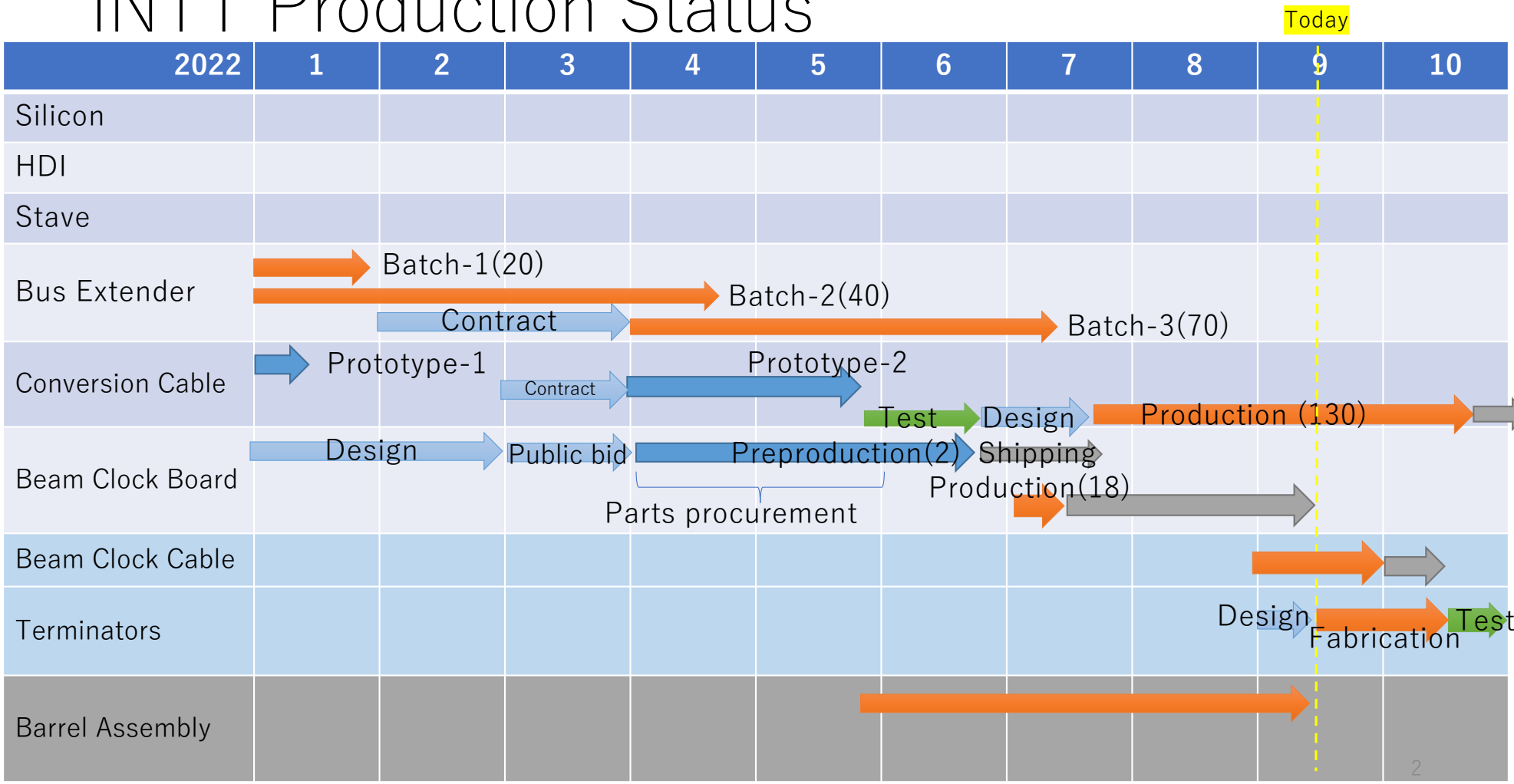
Production Status

RIKEN/RBRC
Itaru Nakagawa

INTT Production Status



1008 ROC Test Status

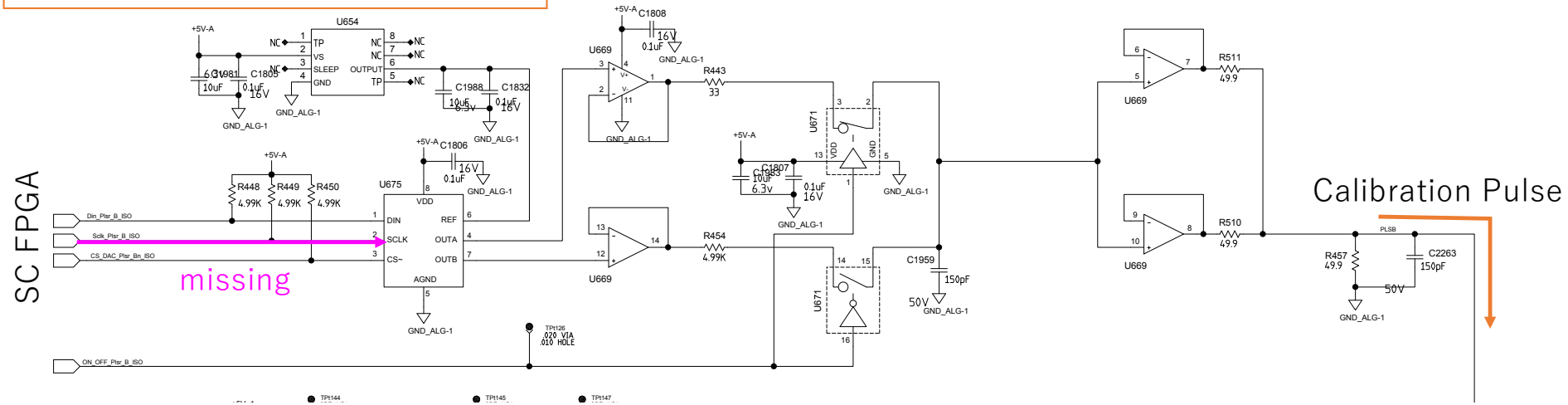
Suggested BNL ROC Configuration

Sent from RIKEN

Index	ROC #	FVTX	Regulator Upgrade	Location	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3	Issue	Status
12	19	NE5	✓	BNL	3										F			Fiber Sync	Debug w/ John K. → Barrel
13	9	-	✓	BNL	1			R											→ Barrel
14	24	SE4	✓	BNL	2			F							F			Fiber Sync	Waiting for NE5 debug → John K.
15	16	NE3	✓	BNL	3				C	C	C							Calib Pulse	Waiting for SC-FPGA downlaod

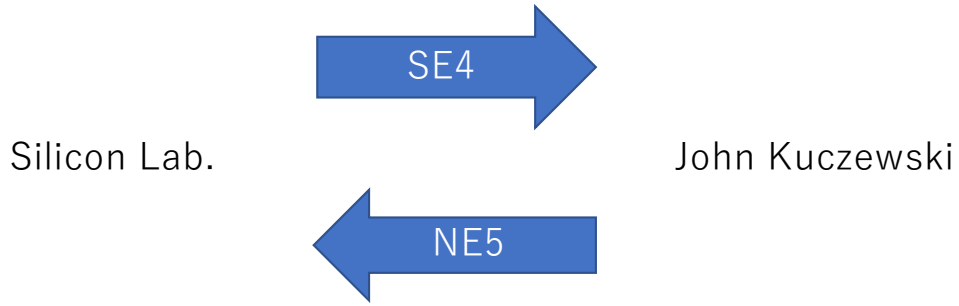
SE4 needs download to ROC SC-FPGA. → 2nd Felix/Windows

Calibration Pulse Generator Circuit



SE4 ROC Fiber Latch Problem

- A3, D1 Ports have the fiber latch problem. They have never been successful in fiber latching, i.e. always fail.

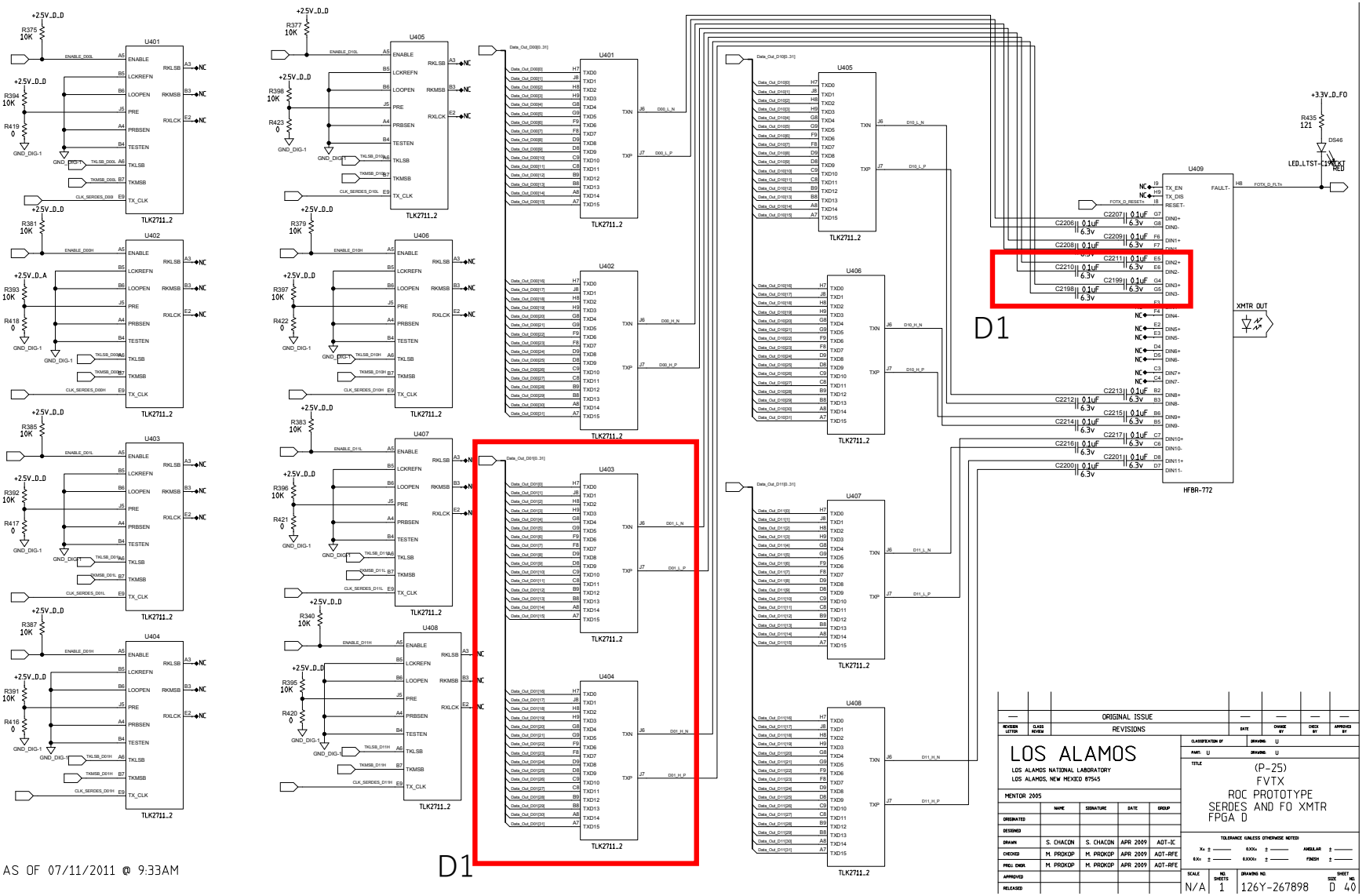


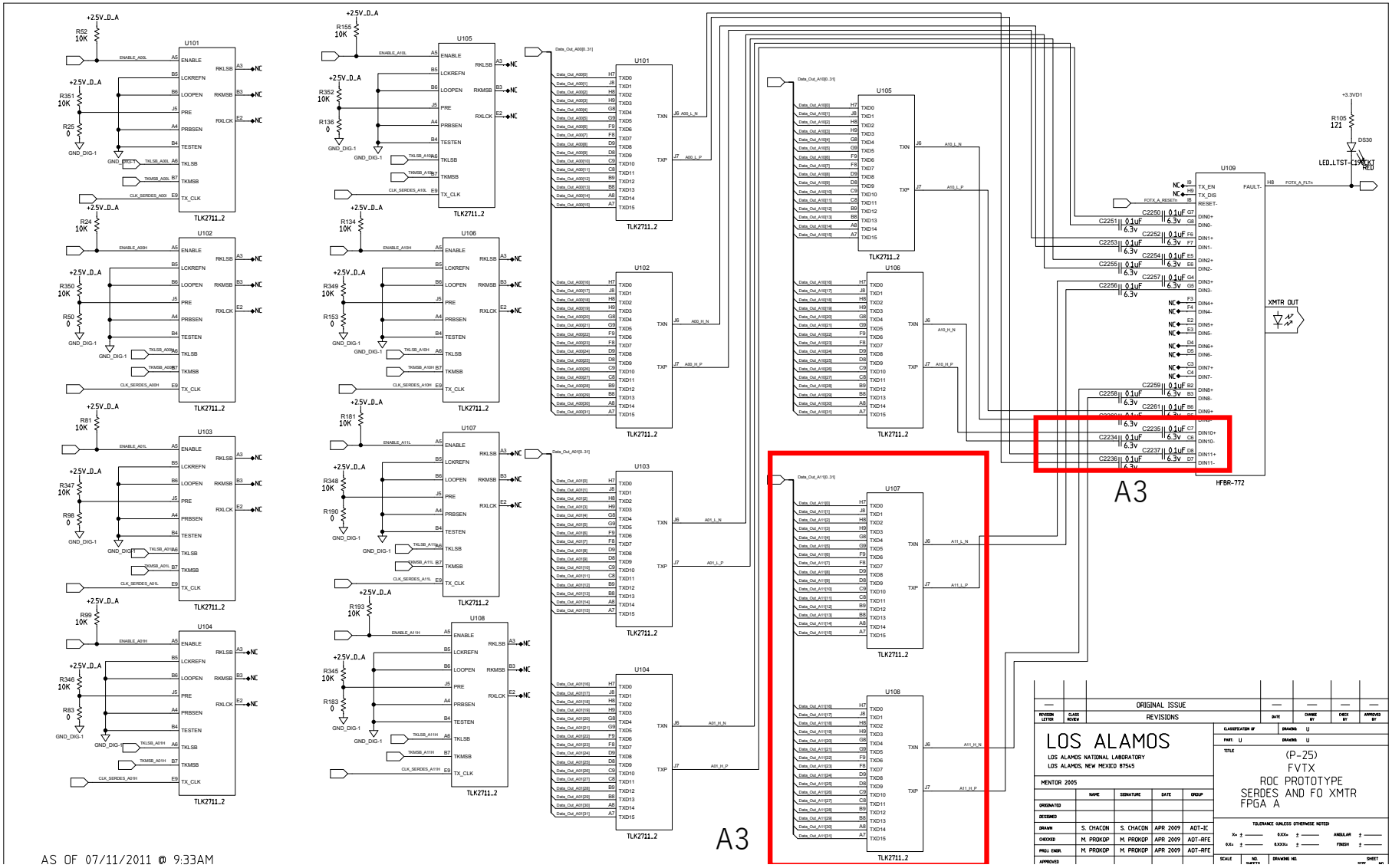
ROC Repair Status

12 Class-1 ROCs

Delivery by the end of Sept except for NE1

Index	ROC #	FVTX	Regulator Upgrade	Location	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3	Issue	Status
1	6	NW2	✓	BNL	1														
2	13	NE4	✓	BNL	1														
3	18	NE1	✓	BNL	1														
4	26	SE3	✓	BNL	1														
5	28	SE0	✓	BNL	1														
6	29	-	✓	BNL	1														
7	20	SW5	✓	BNL	1														
8	22	SE2	✓	BNL	1														
9	23	SE1	✓	BNL	1														
10	31	NW1	✓	BNL	1	R	R	R											
11	32	NE2	✓	BNL	1							R	R	R					
12	19	NE5	✓	BNL	3										F			Fiber Sync	Debug w/ John K.
13	9	-	✓	BNL	1			R											
14	24	SE4	✓	BNL	2			F							F			Fiber Sync	Waiting for NE5 debug
15	16	NE3	✓	BNL	3				C	C	C							Calib Pulse	Waiting for SC-FPGA downlaod
14	15	NE0	✓	RKN	2	F									F			Fiber Sync	Waiting for NE5 debug
16	2	NW4	✓	RKN	3														
19	7	-	✓	RKN	3													Fiber Sync	Replaced all DF18
17	21	-	✓	REPIC	3	R			C		R		R		C				
18	10	-	✓	REPIC	3					R									
15	17	NW3	✓	REPIC	2				F									Fiber Sync	Waiting for NE5 debug
20	3	NW5		REPIC		F											F		
21	27	SE5		REPIC											P	P	P	No fiber light	L12 be replaced
22	14	NE1		REPIC								C	C	C	P	P	P	Calib Pulse	

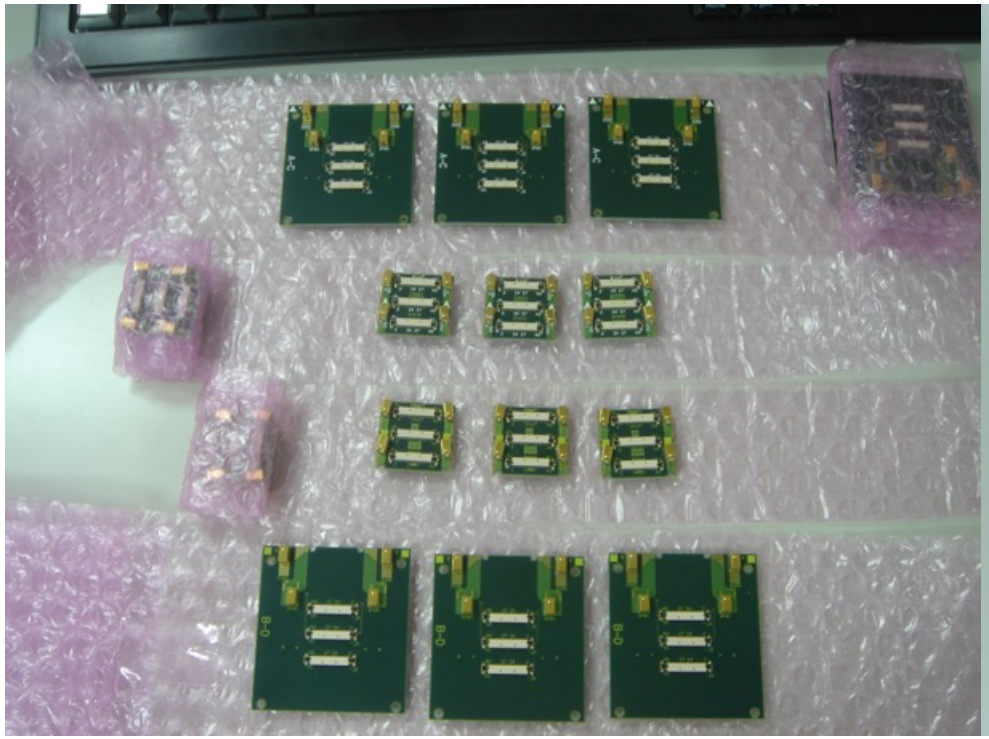

U401
U402
U403
U404
U405
U406
U407
U408
U409
TLK2711_2
HFBR-772
D1
D1
XMTR OUT
LOS ALAMOS
LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545
MENTOR 2005
ORIGINAL ISSUE
REVISIONS
(P-25)
FVTX
ROC PROTOTYPE
SERDES AND FO XMTR
FPGA D
126Y-267898
AS OF 07/11/2011 @ 9:33AM

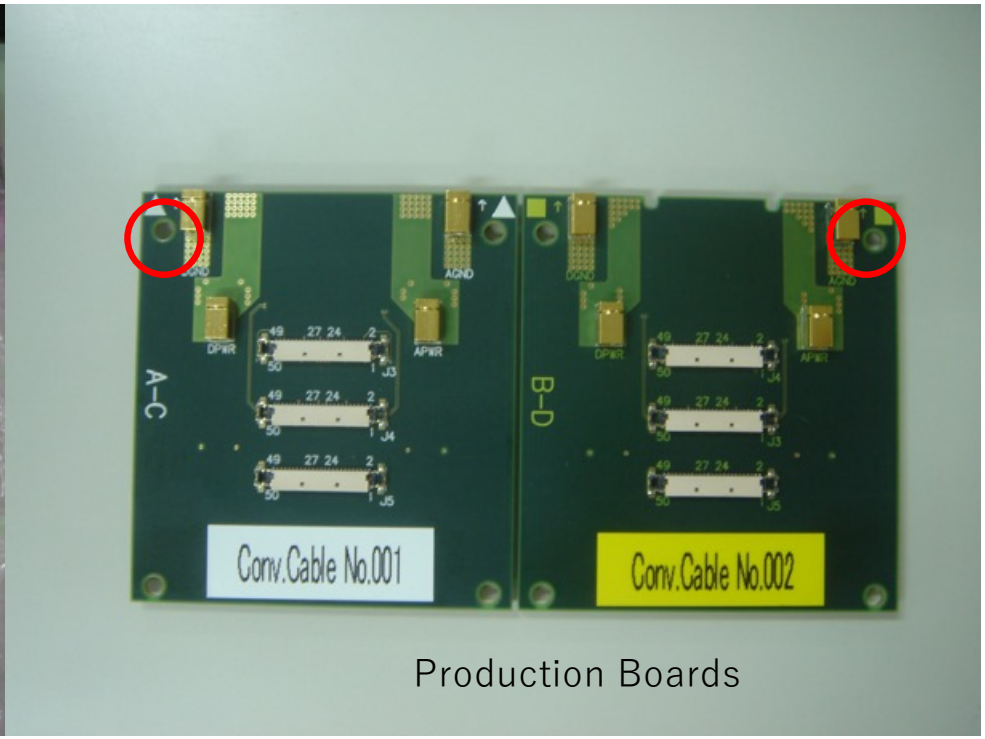


AS OF 07/11/2011 @ 9:33AM

μ-Coax Cable

Fabrication of Production Boards for μ-Coax





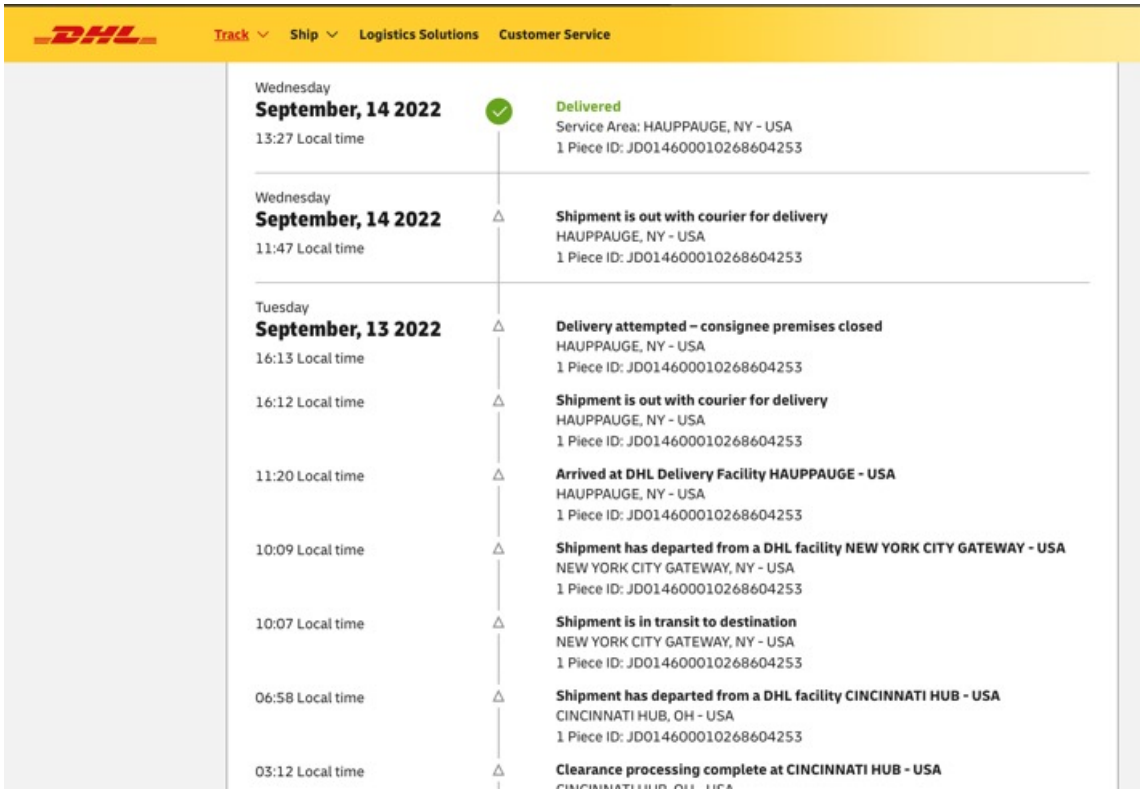
Production Boards

Fabrication of production boards of conv. cable has been completed by now. Waiting for μ-Coax to be delivered by early next week. Then start tape lapping -> assembly -> testing -> Delivery by the middle of October. Earliest forwarding to BNL is end of October.

Beam Clock Boards

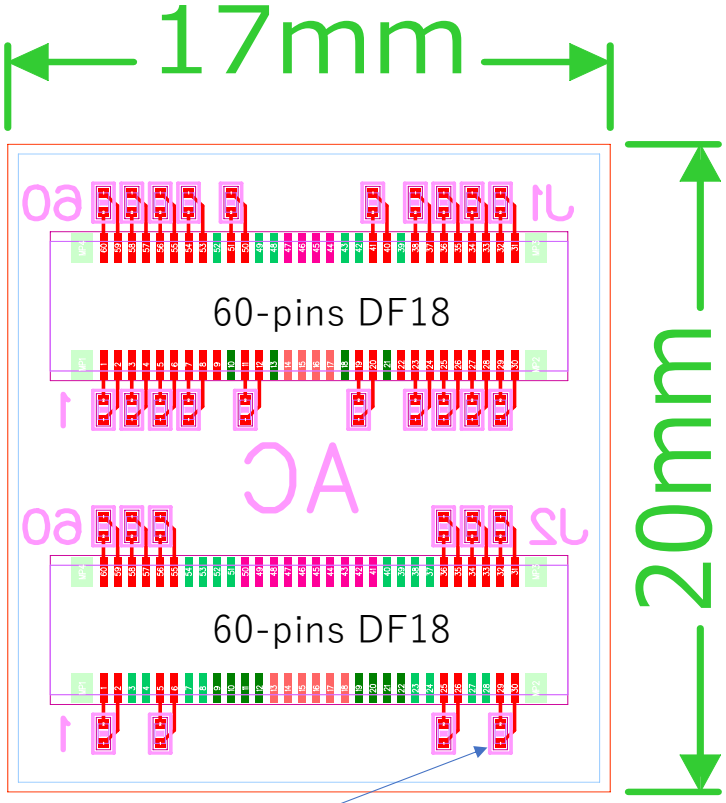
Production Beam Clock Boards Exporting

Passed US custom successfully.
To be delivered to physics soon.



LVDS Terminator

Terminator Prototype Design

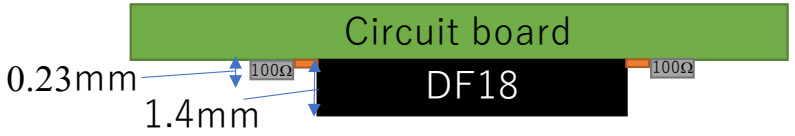


Double Layer

Side View

- 😀 No interference of resistance with DF18 on ROC
- 😰 Costly in fabrication
- 😰 Touched by finger to plug in

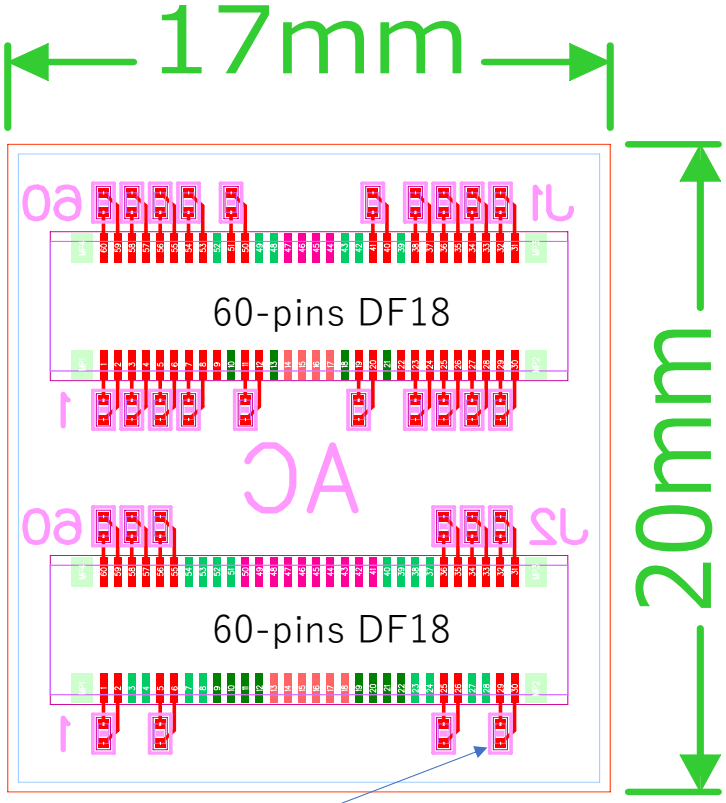
Single Layer



Side View

- 😀 Cheaper fabrication
- 😀 Will not touch surface mount resistance by finger
- 😰 Possibly scraped off when plugging in

Terminator Prototype Design



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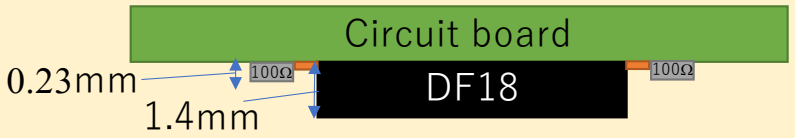
Single Layer



Side View

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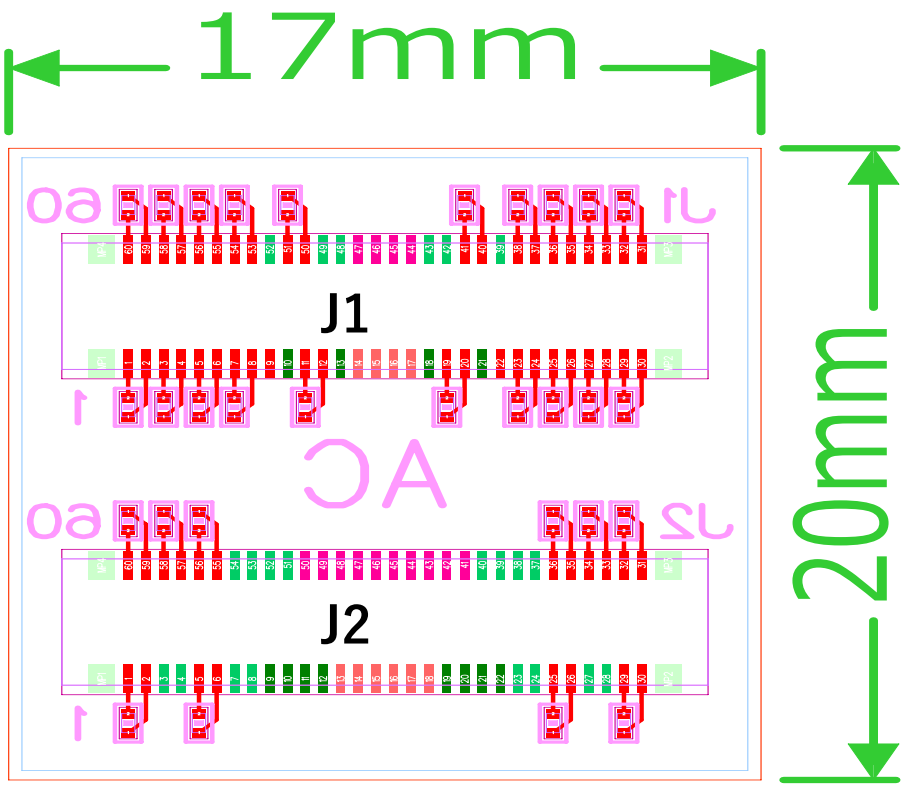
Terminator Prototype Design



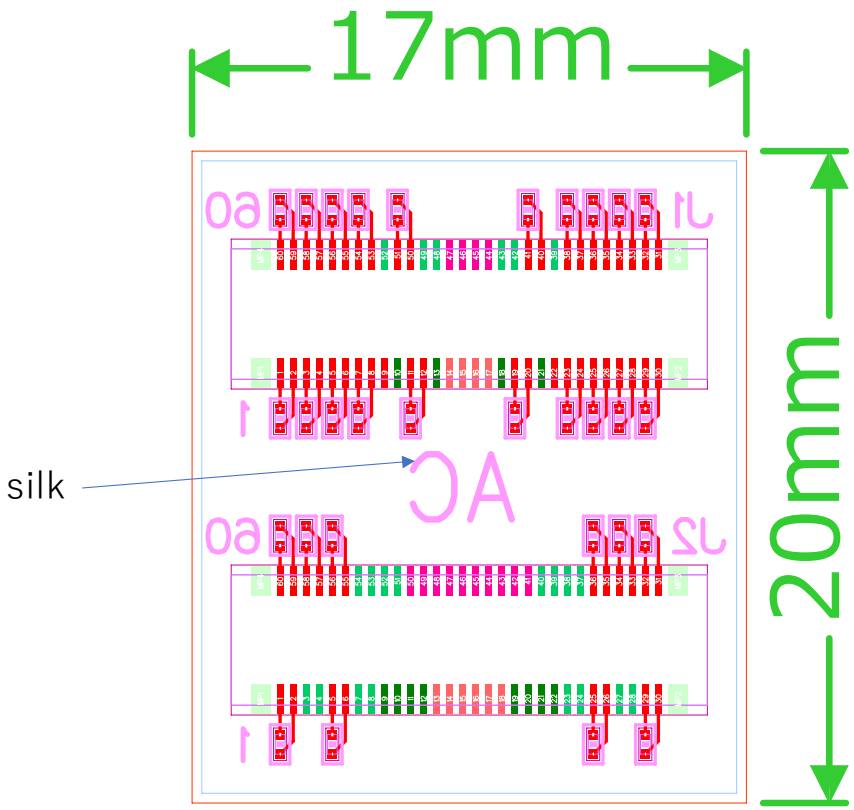
Small DF18 Channel Map

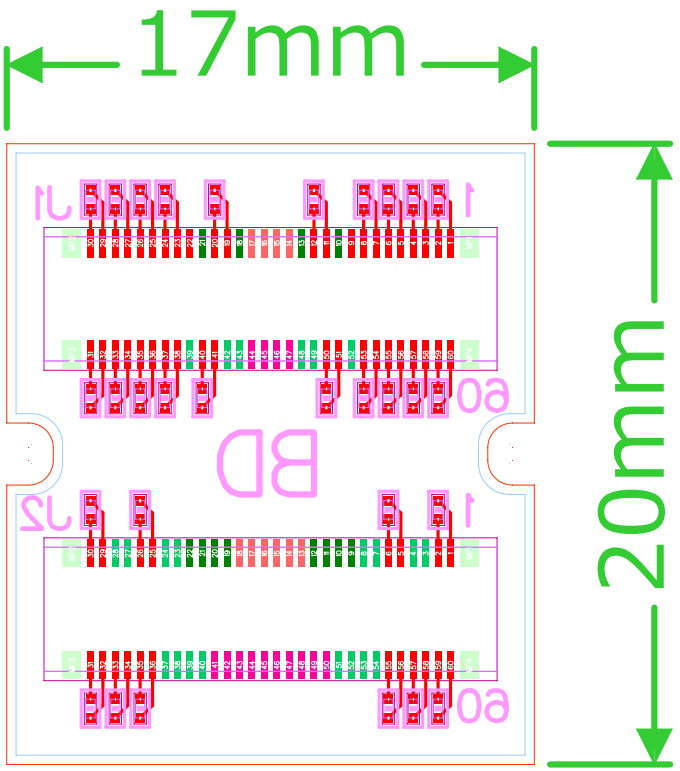
RECEPTACLE (TOP)							
J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	1_CHIP1_OUT 1P	60	1_CHIP1_OUT 0P	1	OUT_CLK1n		BCO_CLK1p
2	1_CHIP1_OUT 1N	59	1_CHIP1_OUT 0N	2	OUT_CLK1p		BCO_CLK1n
3	1_CHIP2_OUT 1P	58	1_CHIP2_OUT 0P	3	DGND		RESET1p
4	1_CHIP2_OUT 1N	57	1_CHIP2_OUT 0N	4	DGND		RESET1n
5	1_CHIP3_OUT 1P	56	1_CHIP3_OUT 0P	5	SC_IN1n		SC_OUT1p
6	1_CHIP3_OUT 1N	55	1_CHIP3_OUT 0N	6	SC_IN1p		SC_OUT1n
7	1_CHIP4_OUT 1P	54	1_CHIP4_OUT 0P	7	DGND		DGND
8	1_CHIP4_OUT 1N	53	1_CHIP4_OUT 0N	8	DGND		DGND
9	CAL_INJECT1	52	DGND	9	AGND		DGND
10	AGND	51	1_CHIP5_OUT 0N	10	AGND		DGND
11	1_CHIP5_OUT 1P	50	1_CHIP5_OUT 0P	11	AGND		+2.5VD
12	1_CHIP5_OUT 1N	49	DGND	12	AGND		+2.5VD
13	AGND	48	DGND	13	+2.5VA		+2.5VD
14	+2.5VA	47	+2.5VD	14	+2.5VA		+2.5VD
15	+2.5VA	46	+2.5VD	15	+2.5VA		+2.5VD
16	+2.5VA	45	+2.5VD	16	+2.5VA		+2.5VD
17	+2.5VA	44	+2.5VD	17	+2.5VA		+2.5VD
18	AGND	43	DGND	18	+2.5VA		+2.5VD
19	0_CHIP5_OUT 0P	42	DGND	19	AGND		+2.5VD
20	0_CHIP5_OUT 0N	41	0_CHIP5_OUT 1N	20	AGND		+2.5VD
21	AGND	40	0_CHIP5_OUT 1P	21	AGND		DGND
22	0_CAL_INJECT0	39	DGND	22	AGND		DGND
23	0_CHIP4_OUT 0N	38	0_CHIP4_OUT 1N	23	DGND		DGND
24	0_CHIP4_OUT 0P	37	0_CHIP4_OUT 1P	24	DGND		DGND
25	0_CHIP3_OUT 0N	36	0_CHIP3_OUT 1N	25	SC_IN0n		SC_OUT0p
26	0_CHIP3_OUT 0P	35	0_CHIP3_OUT 1P	26	SC_IN0p		SC_OUT0n
27	0_CHIP2_OUT 0N	34	0_CHIP2_OUT 1N	27	DGND		RESET0p
28	0_CHIP2_OUT 0P	33	0_CHIP2_OUT 1P	28	DGND		RESET0n
29	0_CHIP1_OUT 0N	32	0_CHIP1_OUT 1P	29	OUT_CLK0n	32	BCO_CLK0p
30	0_CHIP1_OUT 0P	31	0_CHIP1_OUT 1N	30	OUT_CLK0p	31	BCO_CLK0n

プロット エリア

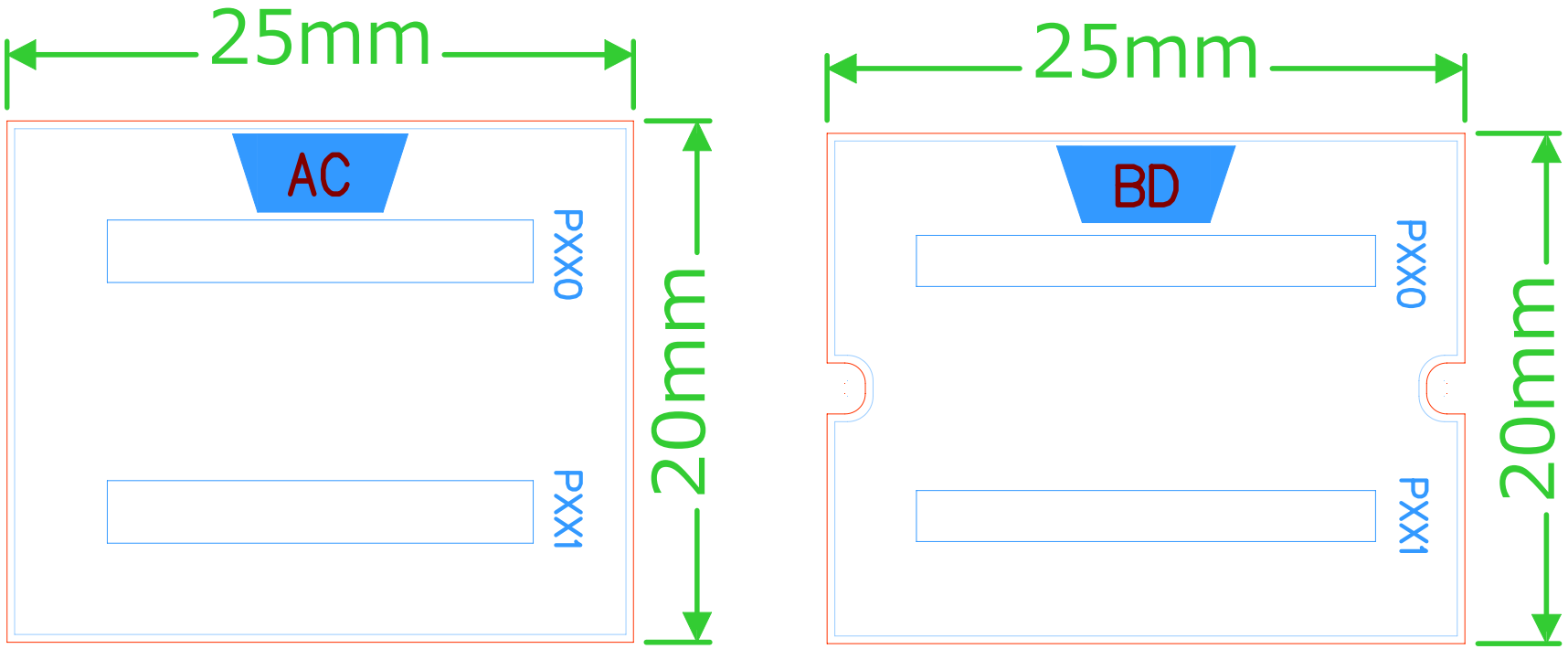
All LVDS pairs are terminated by 100Ω resistances regardless if output/input for ROC FPGA.
J1 and J2 patterns are different and thus incompatible.

Small Type Terminator Design (Primary Side)

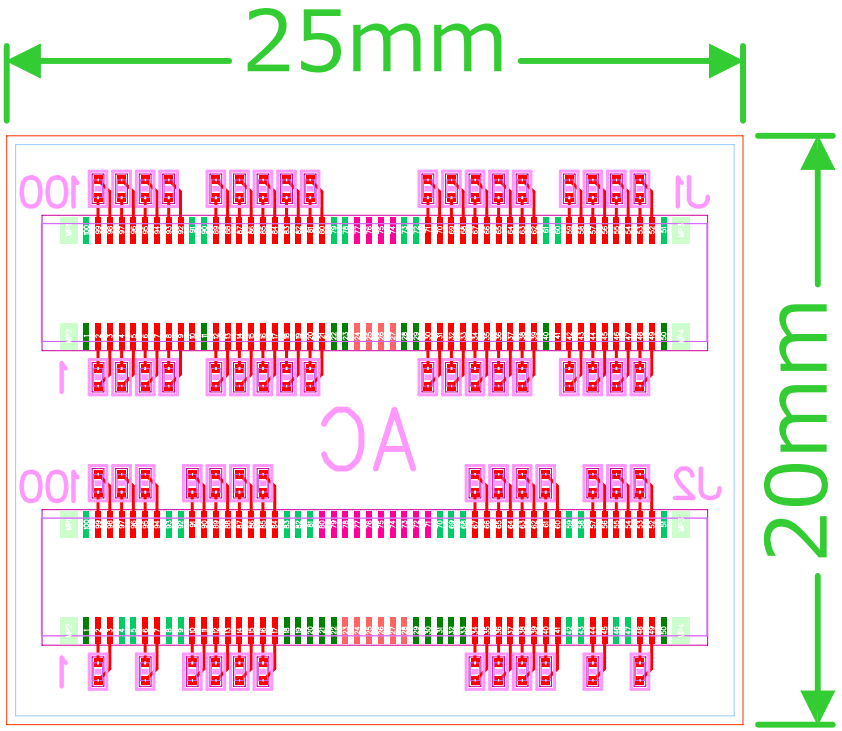


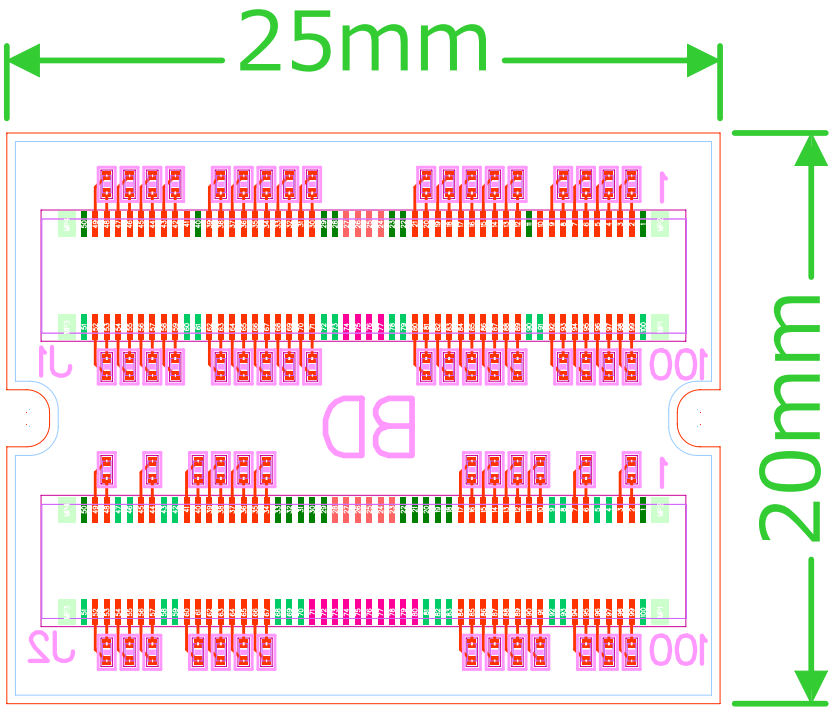


Small Type Terminator Design (Back Side)

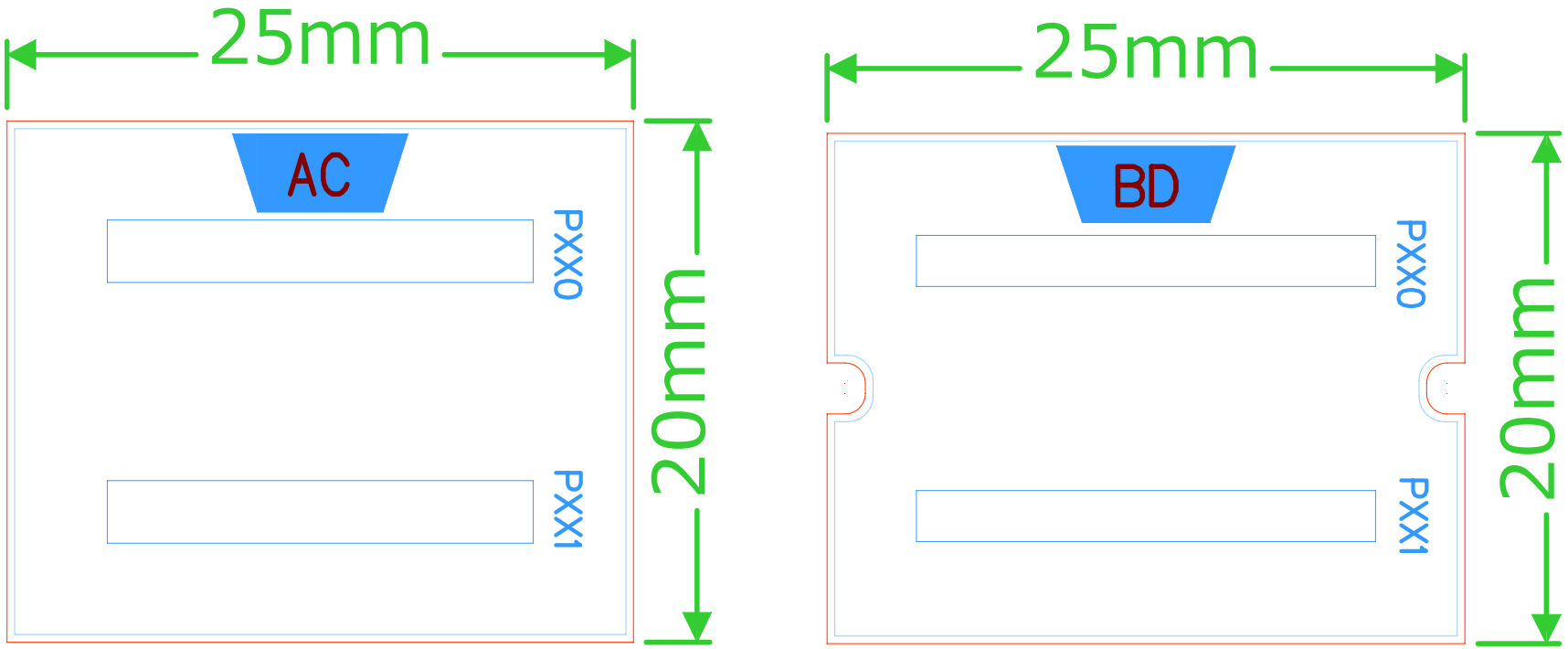


Large Type Terminator Design (Primary Side)

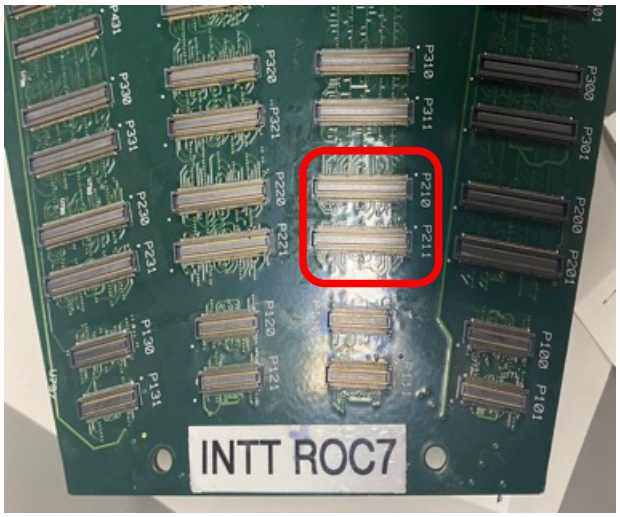




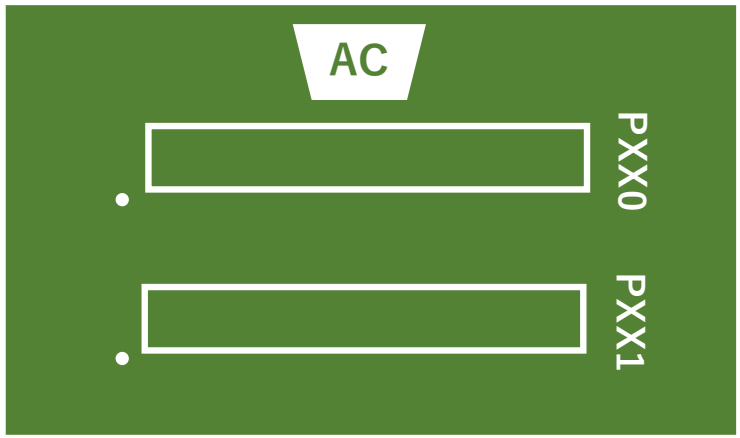
Large Type Terminator Design (Back Side)

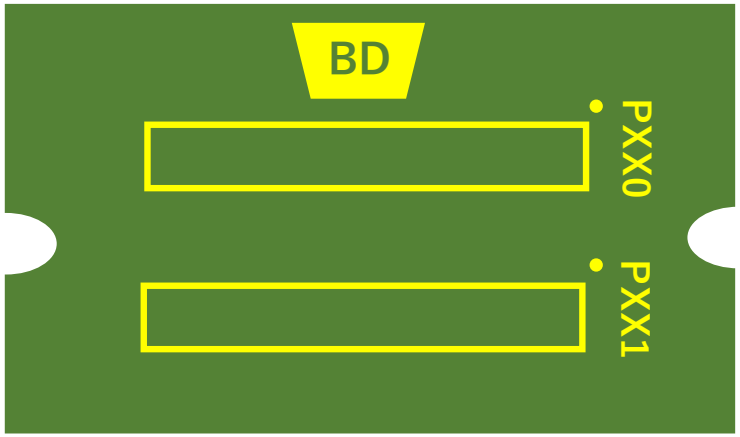


Symbols to avoid misconnection

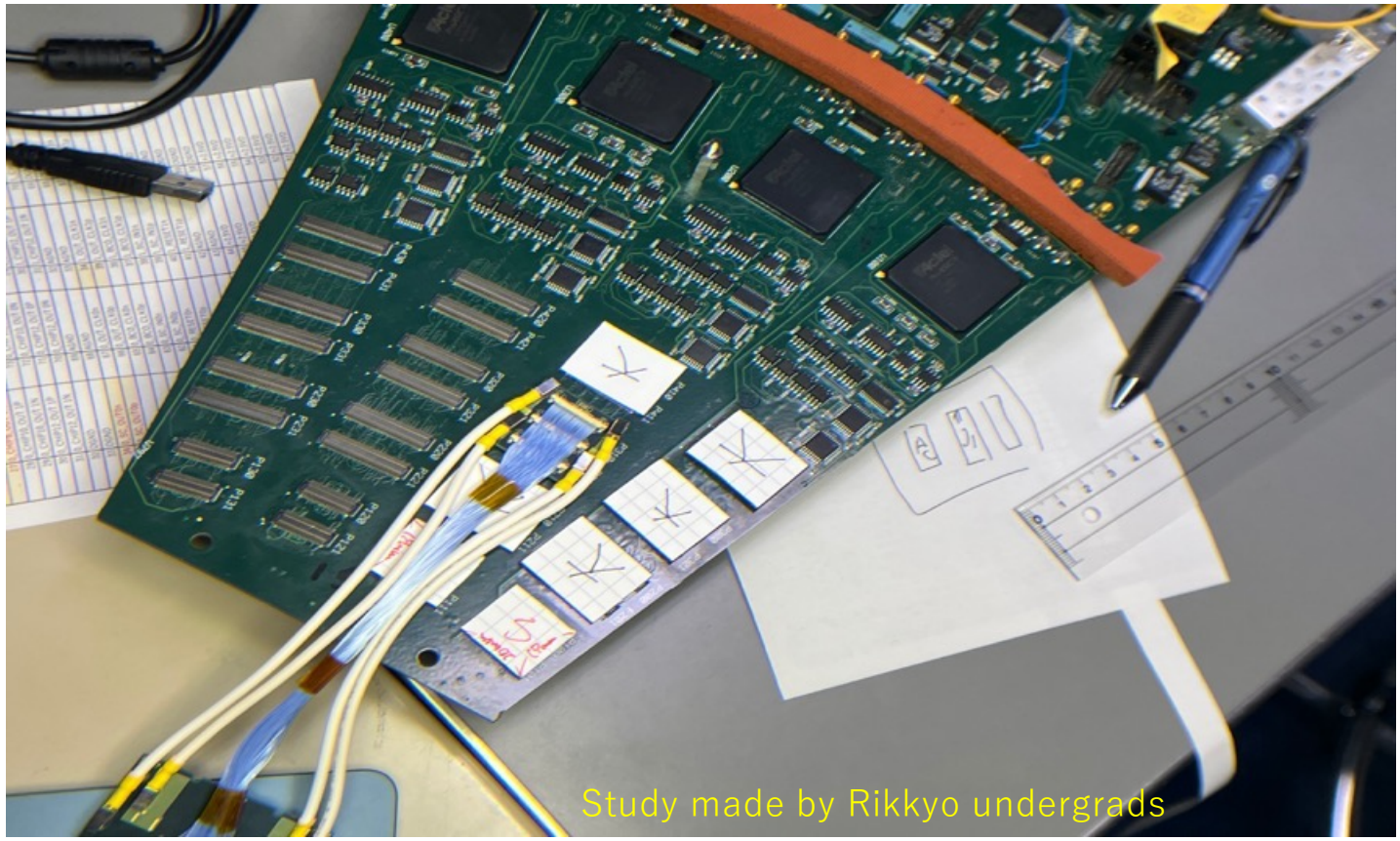


1. Following the same scheme of the conversion cable, the silk color is white for AC-type and yellow for BD type.
2. BD-type have half circle cuts on both sides as well.
3. Orientation is indicated by PXX0 and PXX1, plus trapezoid shape which mimics the shape of ROC board.





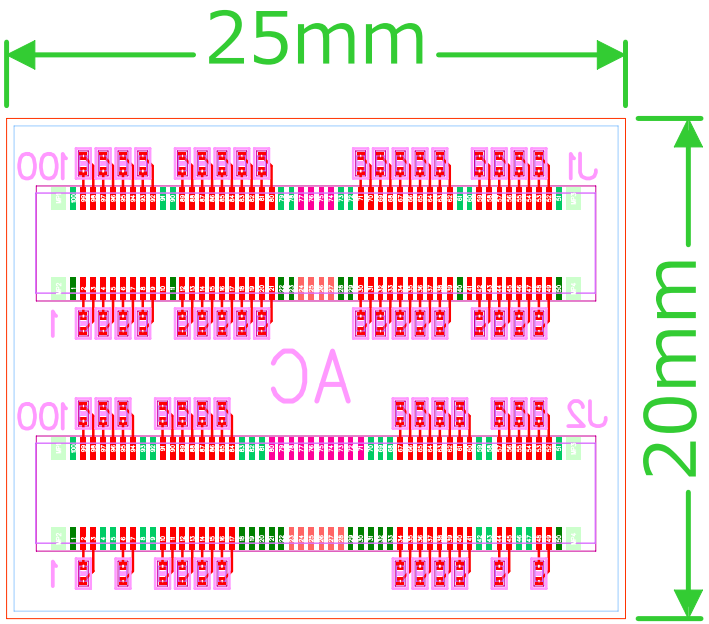
Interference Check between adjacent connectors



Large terminators are slightly smaller than ROC side boards of the conversion cable. Thus they shouldn't interfere with adjacent boards.

ROC Side Connector of Conversion Cable

Terminator



ROC Side connector of CC