Precision clock distribution for the CMS Phase II timing detectors

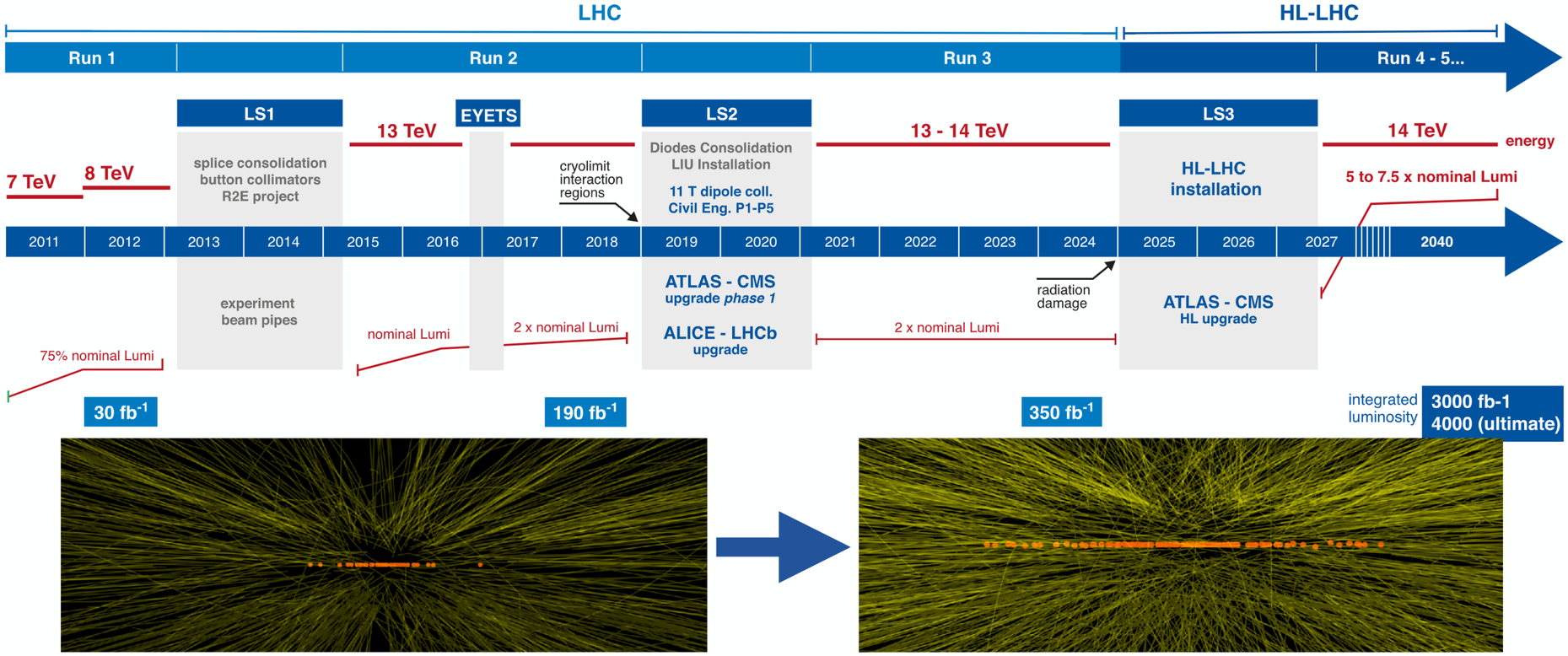
Outline

HL-LHC and CMS
- Case for timing in Phase II
- MIP timing detector

DAQ and clock distribution network
Jitter
Component validation
Monitoring

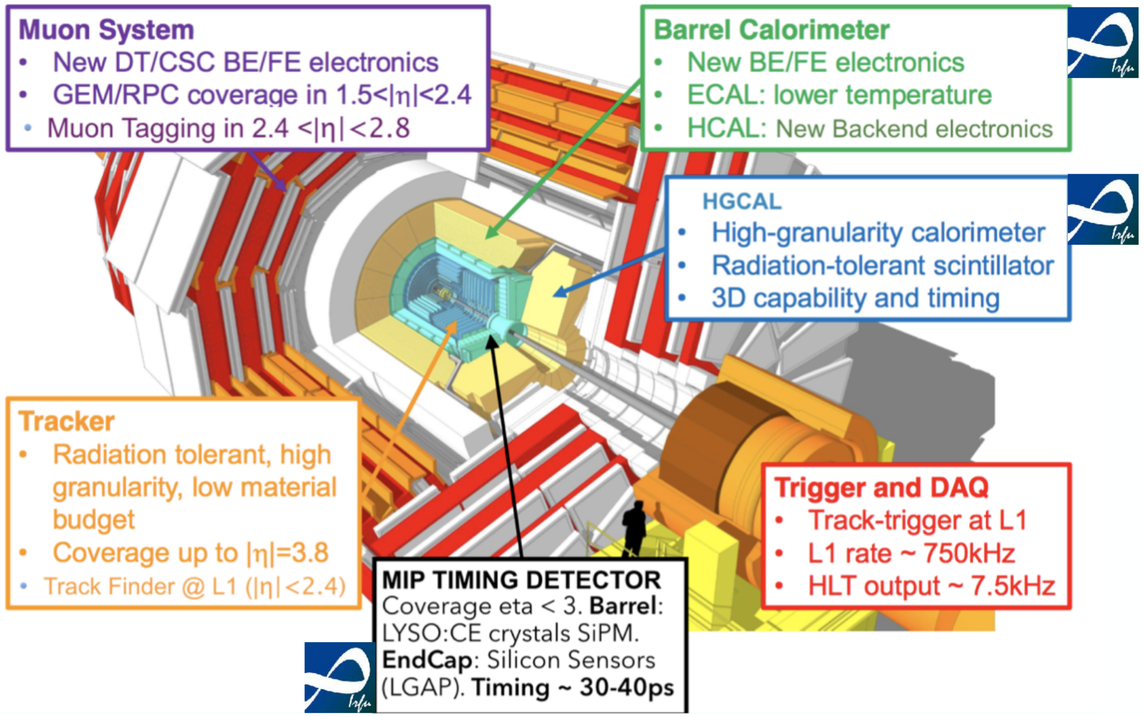
Özgür Sahin
CEA Saclay / Irfu
On behalf of large number of people from
CEA Saclay, CERN, Imperial College and other institutes

HL LHC



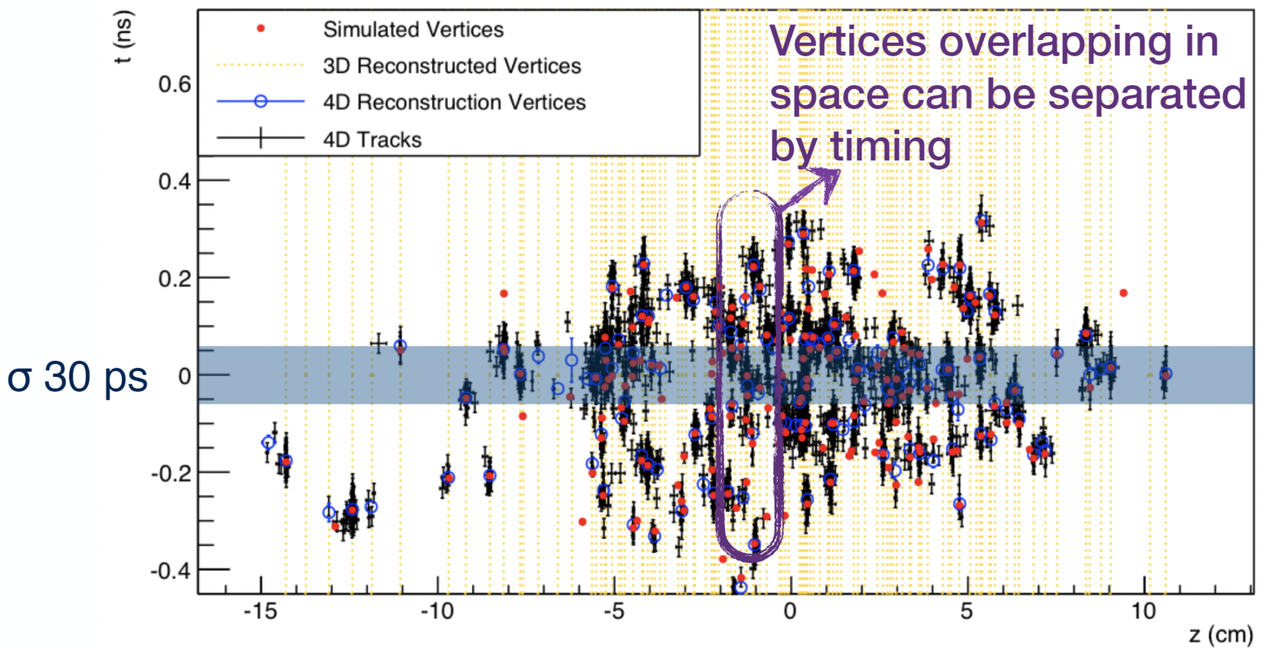
- We have 40.0788 MHz bunch crossing rate at the LHC with a 40 average number of pile up interactions.
- High Luminosity - Large Hadron Collider will deliver 10 times more integrated luminosity.
  - Significant challenge for the detectors; up to 5 times more average pile-up interactions.
- CMS and ATLAS detectors will be upgraded (Phase II - HL upgrade)
  - Cope with the challenging conditions
  - Extend the physics reach.

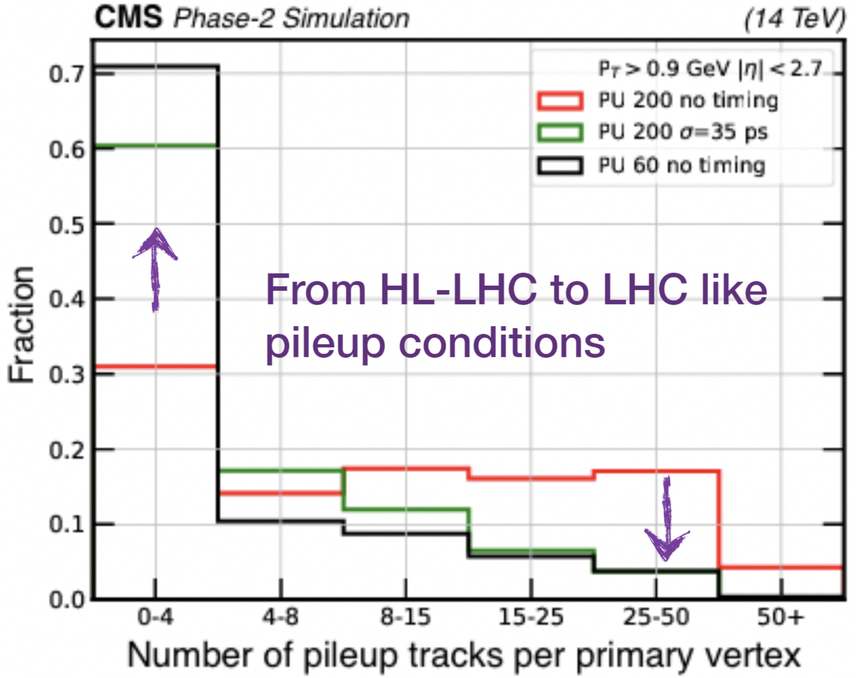
CMS Phase II



- At Irfu we are already involved in three major upgrades and most of them are relating us to the precision timing measurements.
- We are also responsible for the clock distribution for these ‘timing sensitive’ detectors.
  - This talk will focus on MIP Timing Detector as it has the most stringent conditions.

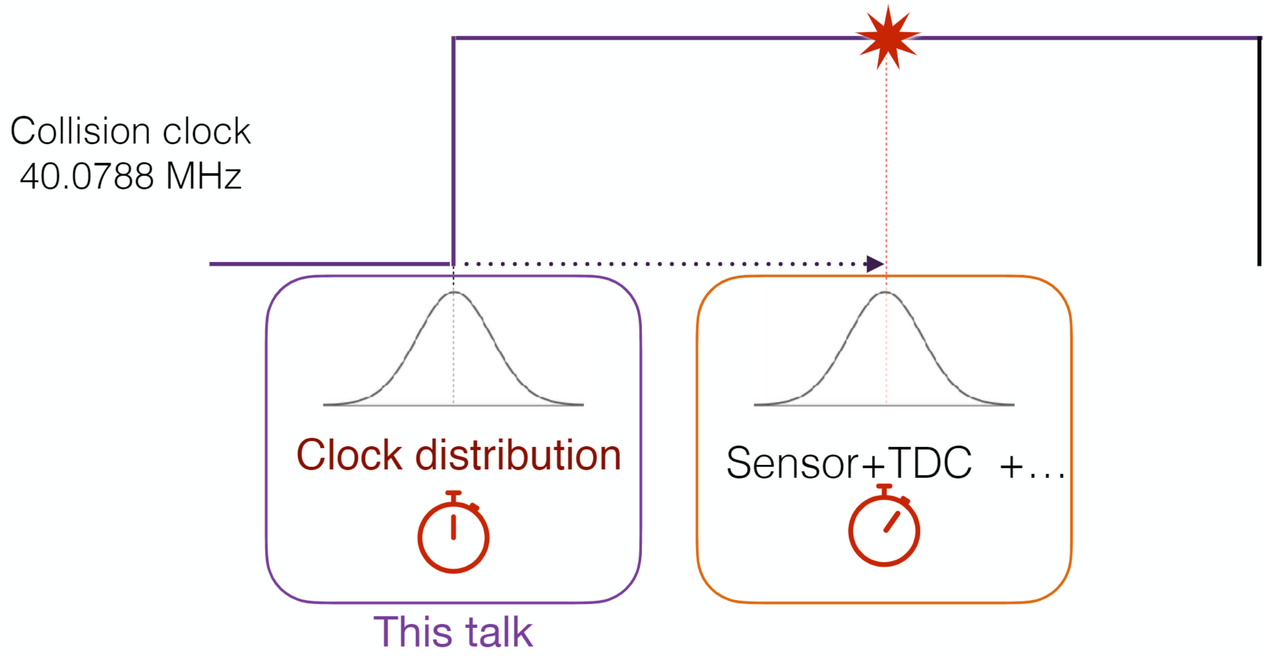
Case for precision timing at the CMS detector





- Increase in the pileup interactions deteriorates association of the tracks with the hard interactions hence worsen the physics performance.
- A timing detector that measures precisely the production time of MIPs will **mitigate the pileup impact and enable new physics** reach such as search for long-lived particles.

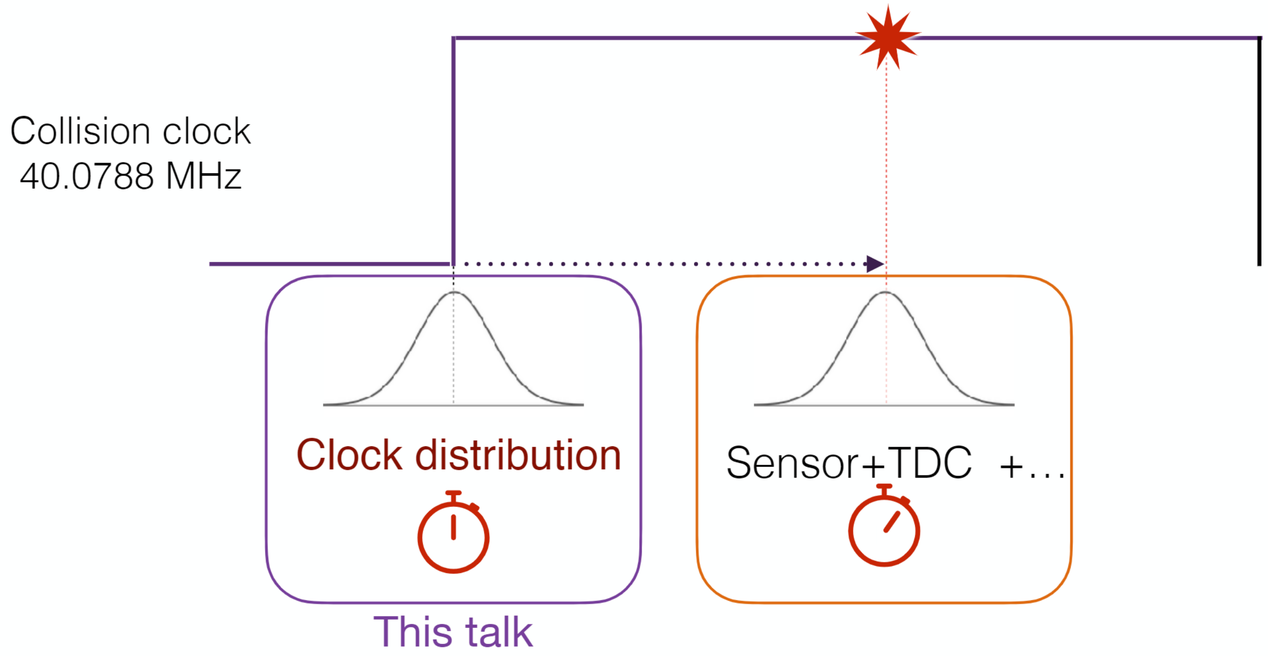
Precision timing jitter



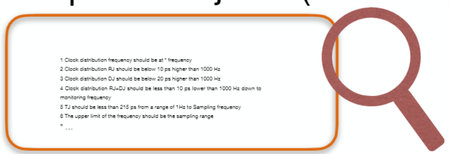
- The time to digital converter (TDC) opens a time window with the arrival of the synchronization (clock) signal.
- The window is closed with the arrival of signal from the sensor.
- The timing resolution directly depends on the Sensor and TDC resolution as well as the jitter from the clock distribution signal.
  - We want the RMS jitter of the clock distribution between few ten thousands of the links to be less than 15 ps RMS jitter ([1] [2] [3] [4] [5] [6] *)!

[1] Clock distribution frequency should be at * frequency
[2] Clock distribution RJ should be below 10 ps higher than 1000 Hz
[3] Clock distribution DJ should be below 20 ps higher than 1000 Hz
[4] Clock distribution RJ+DJ should be less than 10 ps lower than 1000 Hz down to monitoring frequency
[5] TJ should be less than 210 ps from a range of 1 Hz to Sampling frequency
[6] The upper limit of the frequency should be the sampling range
* : …

Precision timing jitter

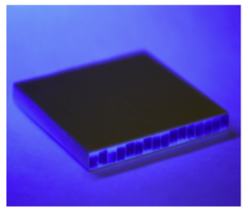


- The time to digital converter (TDC) opens a time window with the arrival of the synchronization (clock) signal.
- The window is closed with the arrival of signal from the sensor.
- The timing resolution directly depends on the Sensor and TDC resolution as well as the jitter from the clock distribution signal.
  - We want the RMS jitter of the clock distribution between few ten thousands of the links to be less than 15 ps RMS jitter ([1] [2] [3] [4] [5] [6] *)!

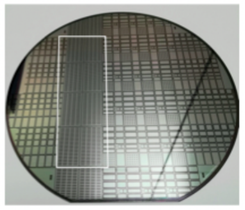


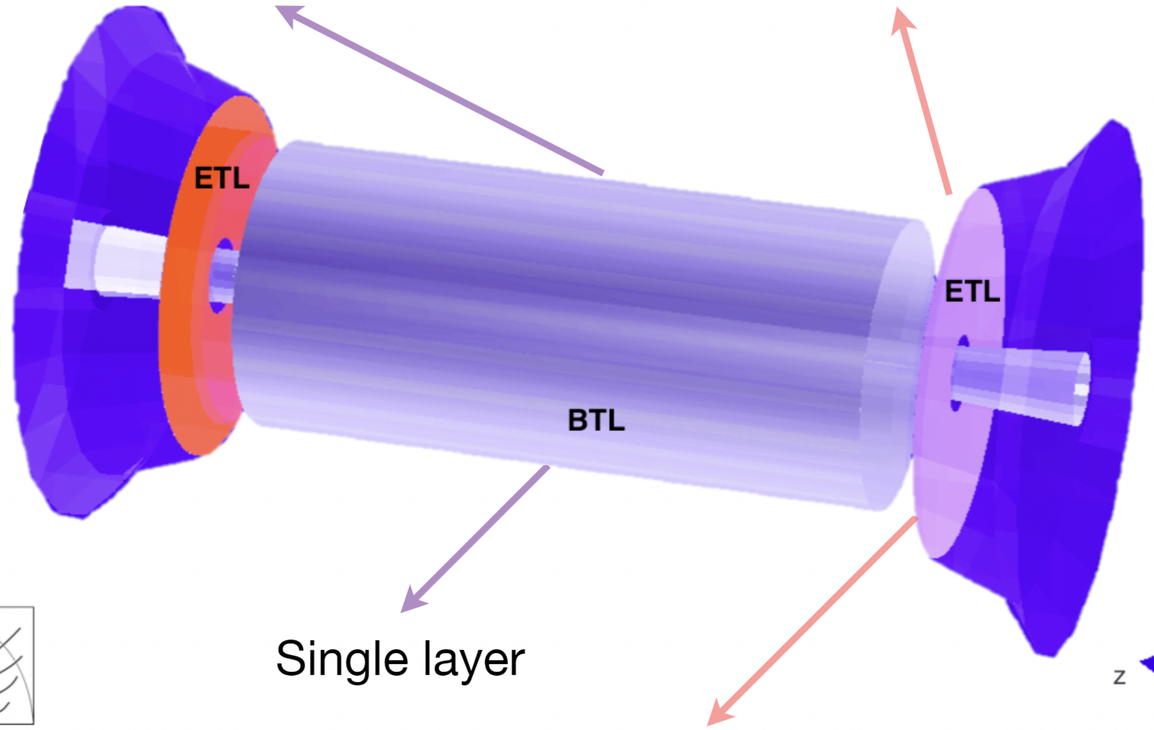
MIP Timing Detector

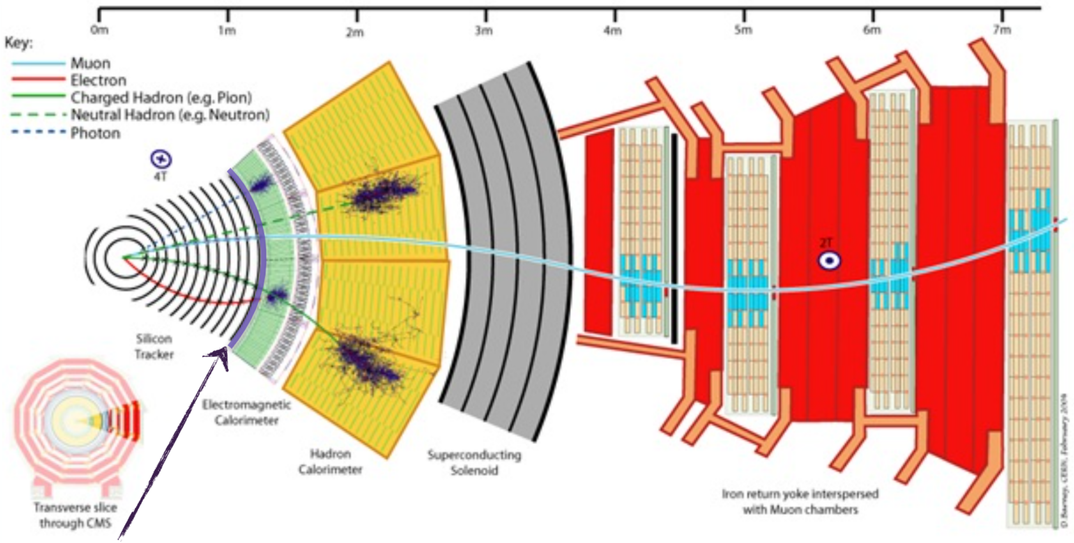
BTL: LYSO bars + SiPM readout:
- TK / ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm (40 mm thick)
- Length: ±2.6 m along z
- Surface ~38 m^2; 332k channels
- Fluence at 4 ab^{-1}: $2x10^{14}$ n_{eq}/cm^2



ETL: Si with internal gain (LGAD):
- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: $315 < R < 1200$ mm
- Position in z: ±3.0 m (45 mm thick)
- Surface ~14 m^2; ~8.5M channels
- Fluence at 4 ab^{-1}: up to $2x10^{15}$ n_{eq}/cm^2



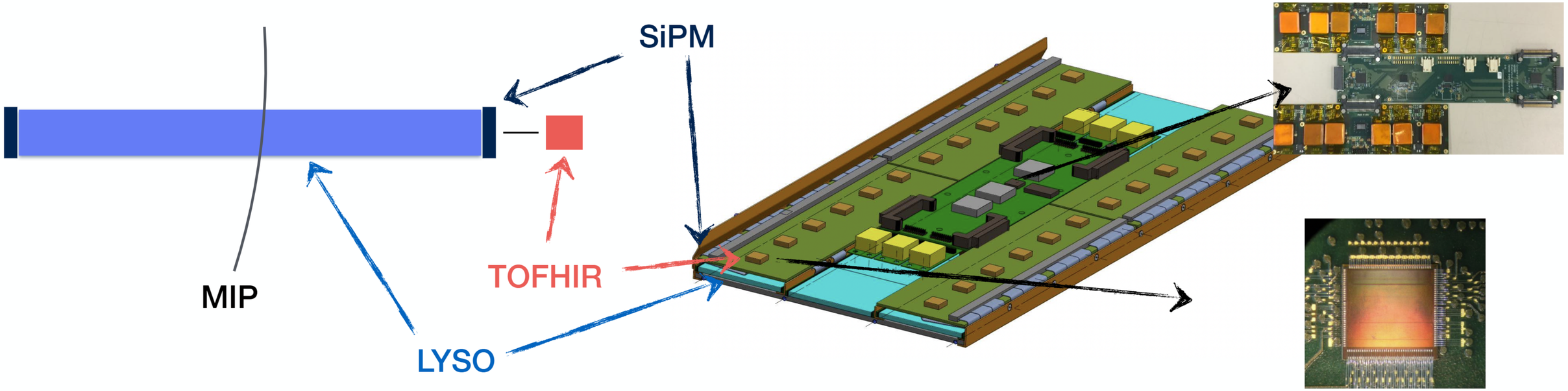




MTD

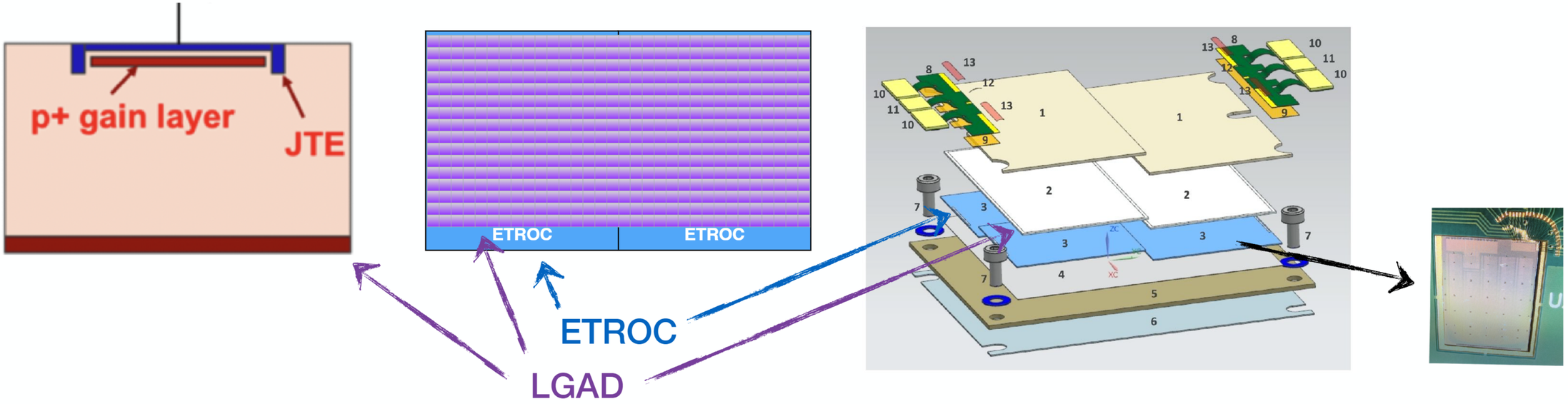
- The **MIP timing detector (MTD)** will have **35 ps resolution** at the beginning of its lifetime.
- It will have an hermetic **coverage up to η=3**.
- Why two different technologies?
- Radiation hardness and cost!

MTD - Barrel timing layer readout



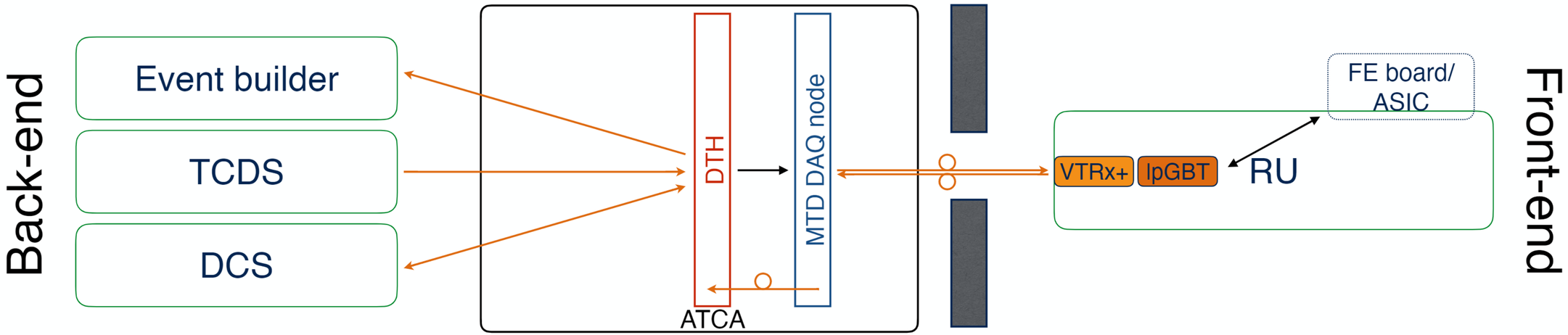
- The readout is performed by silicon photo multipliers (SiPM) and the readout ASIC (TOFHIR).
  - Small cell size SiPM: fast readout, robust against magnetic field and radiation, low power consumption.
  - LYSO crystal bars read out on two sides - improved resolution and response insensitive to position.
- The TOFHIR ASIC has 32 independent channels (can readout 16 crystals), each containing independent amplifiers, discriminators, time-to-digital converters and charge-to-digital converters.

MTD - Endcaps timing layer readout



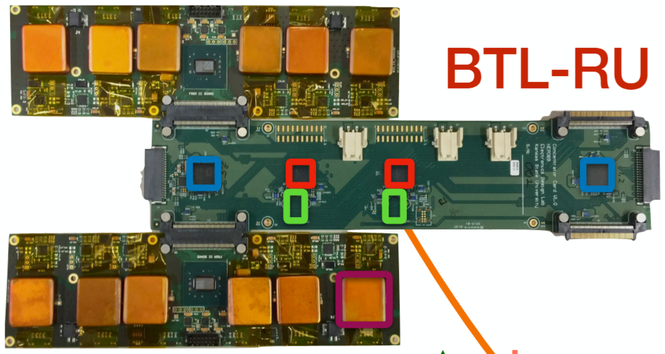
- The Ultra Fast Silicon Detectors can be achieved with an additional gain layer (LGAD) and are optimized for timing.
  - Common CMS & ATLAS development.
- The **ETL readout ASIC (ETROC)** is designed to handle a **16×16 pixel cell matrix**
  - Each channel consists of a preamplifier, a discriminator, a TDC used to digitize the TOA (time of arrival) and TOT (time over threshold) measurements
  - H-tree clock distribution.

MTD DAQ overview



- CMS Phase II DAQ systems are based on the Versatile Link + framework and lpGBT ASIC.
- The number of lpGBTs required for MTD:
  - **BTL: 864 (432 concentrator cards)**
  - **ETL: 1600 links (800 per endcap detector)**
- Serialization of the links: the control, Trigger Timing Control (TTC) and DAQ paths in the same fashion!
- All lpGBTs will operate in the transceiver mode (so no simplex transmitter lpGBTs) at 10 Gb/s.
  - Slow control, fast control and trigger signals are sent via the DAQ links. Therefore, **all links are bidirectional**.
  - In some of the subsystems they operate in simplex transmitter mode as well (just moving data to backend).

MTD DAQ components



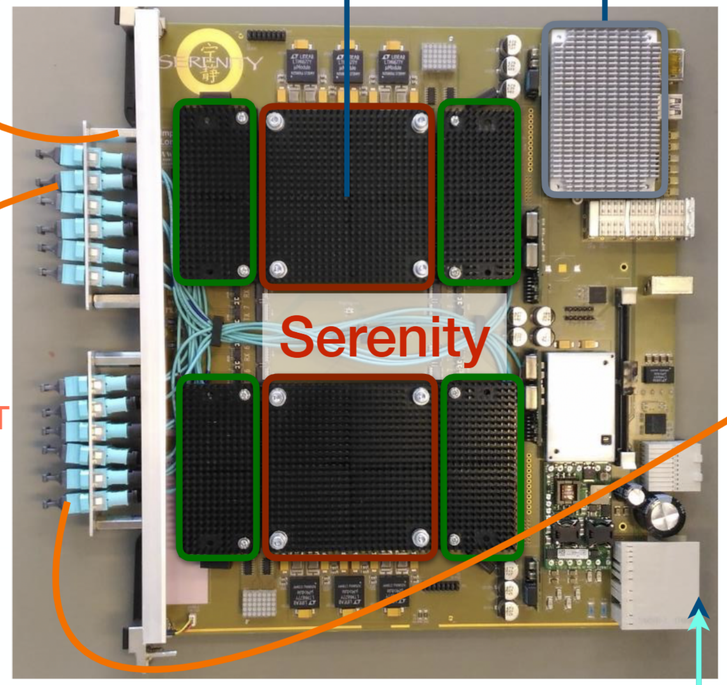
BTL-RU

2.5 Gb/s lpGBT

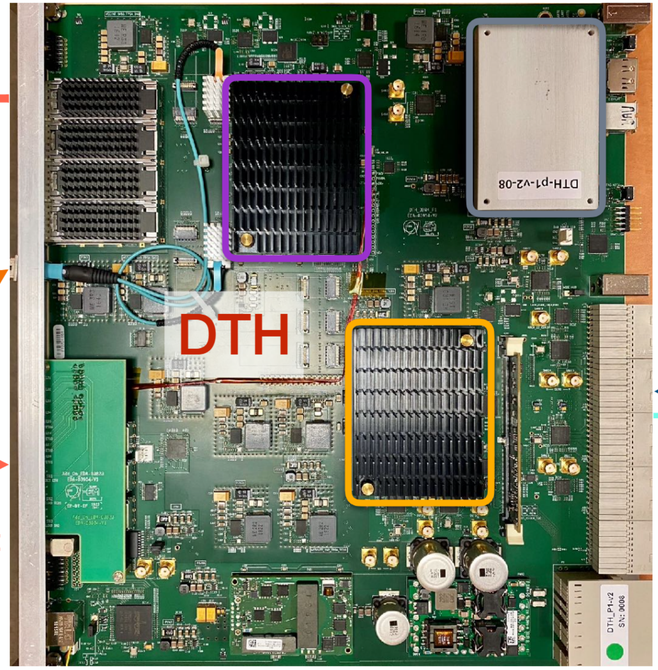
10 Gb/s lpGBT

RU	Serenity	DTH400
lpGBT	CPU	CPU
GBT-SCA	VU9P FPGA	DAQ FPGA
VTRx+	SAMTEC FF	TCDS FPGA
TOFHIR		
ETROC		

1Gb/s IPBUS

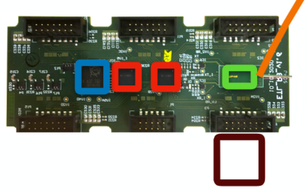


100 Gb/s d2s



2.5 Gb/s lpGBT

10 Gb/s lpGBT



ETL-RU

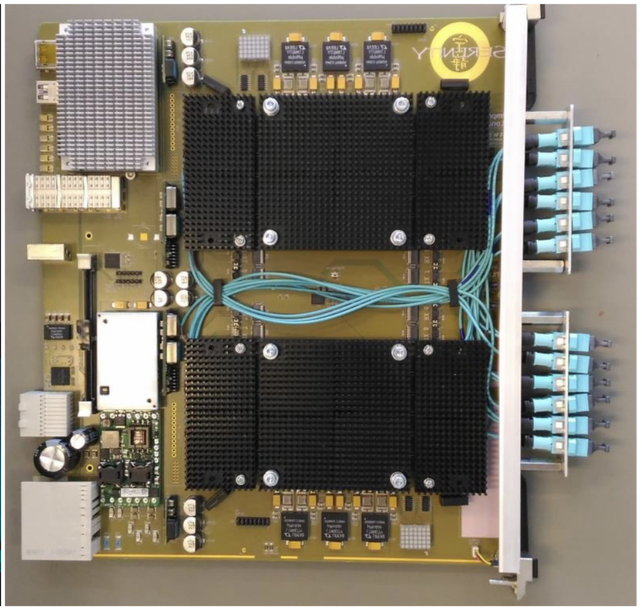
10 Gb/s Ethernet

25 Gb/s slink

1Gb/s IPBUS

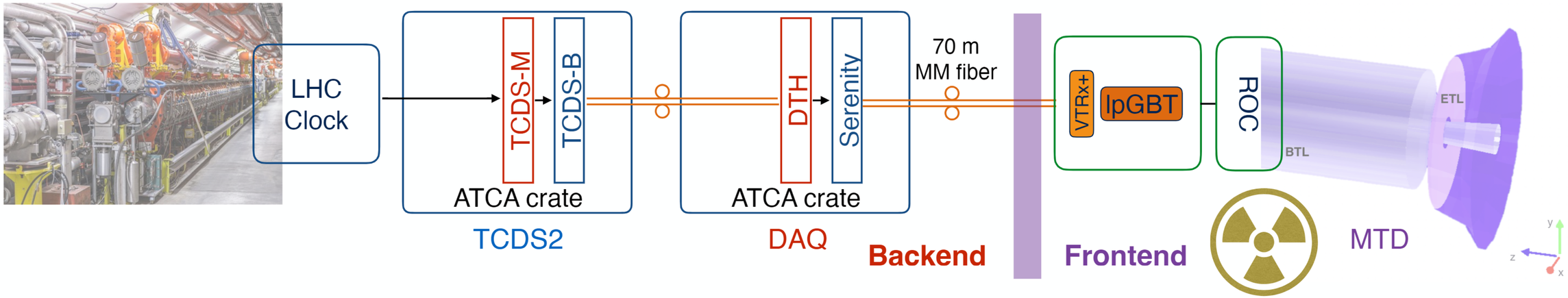
10 Gb/s TTC + Precision clock

Serenity



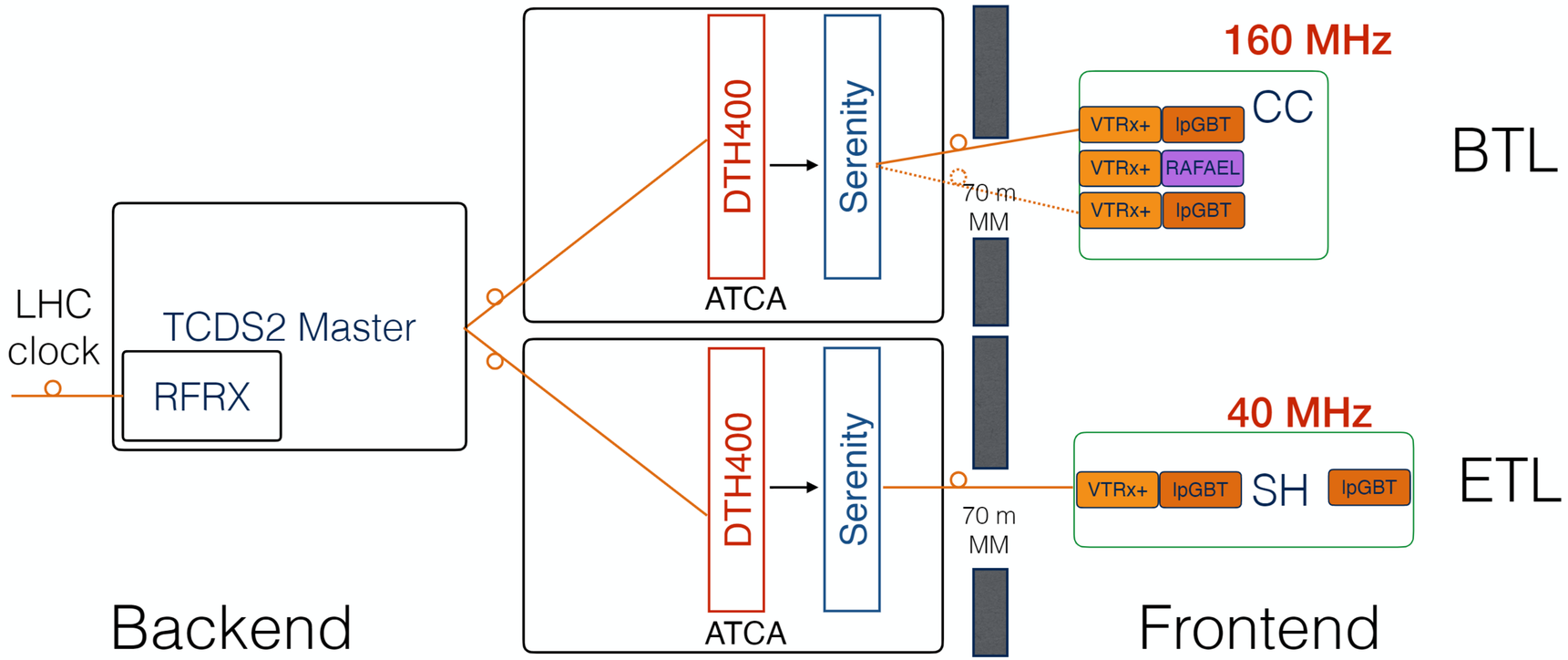
- An ATCA form factor board built by the **Serenity Consortium**
  - IRFU is a part of the Serenity consortium
  - It is used by **HGCAL, MTD, Tracker (partially), L1Trigger (partially) and Muon (partially) systems**.
  - For the development systems **FPGAs are replaceable** (daughter cards with SAMTEC Z ray interposer technology),
  - Can drive more than **144 bidirectional links per board (25 G and 16 G links)**
  - The current FPGA choice for the MTD is **Xilinx VU15P**.

Timing distribution



- 40.0788 MHz LHC clock (synced with the bunch crossing) are distributed from RF system to the experiments (via a system based on WR).
- The experiment (Trigger Control Distribution System) then distribute this clock in an encoded data stream to the subsystem backends.
- The clock is decoded in the backend and encoded in a different control stream to the frontend using lpGBT protocol.
- The lpGBT ASIC recovers the clock and multiply to the reference frequency of the ROC.

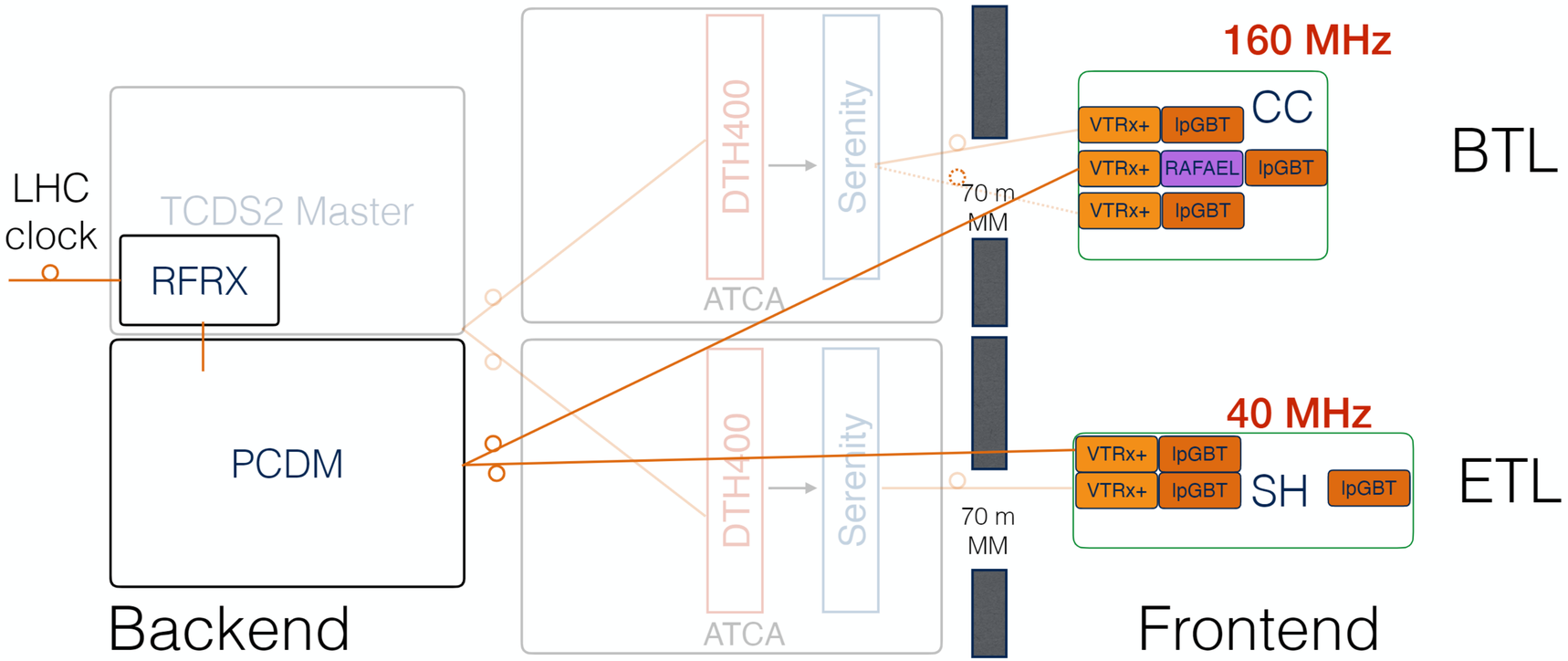
Clock distribution scenario I



Baseline clock distribution:

- The clock distribution should provide a stable clock with less than 15ps RMS jitter (1 Hz to sampling frequency).
- In the baseline distribution the DAQ link is used to distribute the embedded clock.
- (DAQ, control communication and clock distribution can be done with a single bidirectional link.)

Clock distribution scenario II

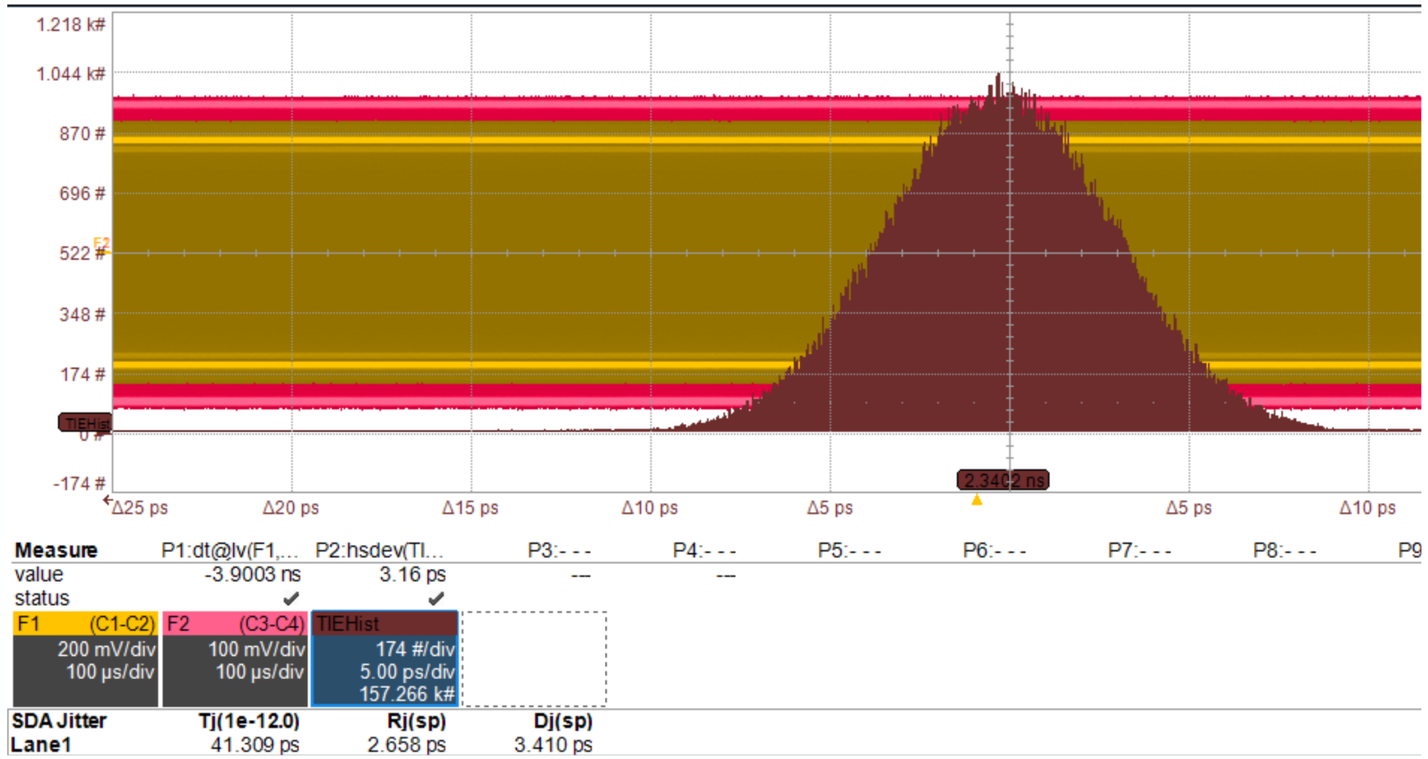


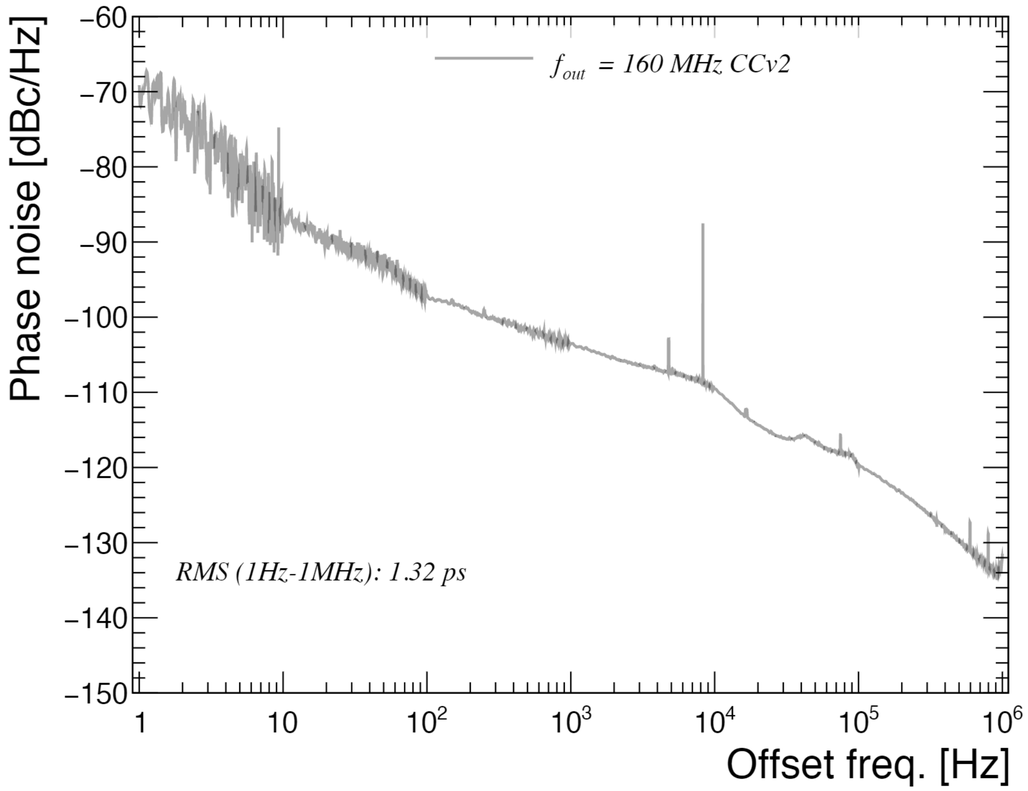
Risk mitigation - pure clock distribution:

- If the **baseline clock distribution fails to meet the performance expectation**, an alternative clock distribution scheme will be used.

- Clock is recovered from RFrx. The clock distributed to the frontend modules without encoding. Requires additional optical fiber and transceivers for each readout unit.

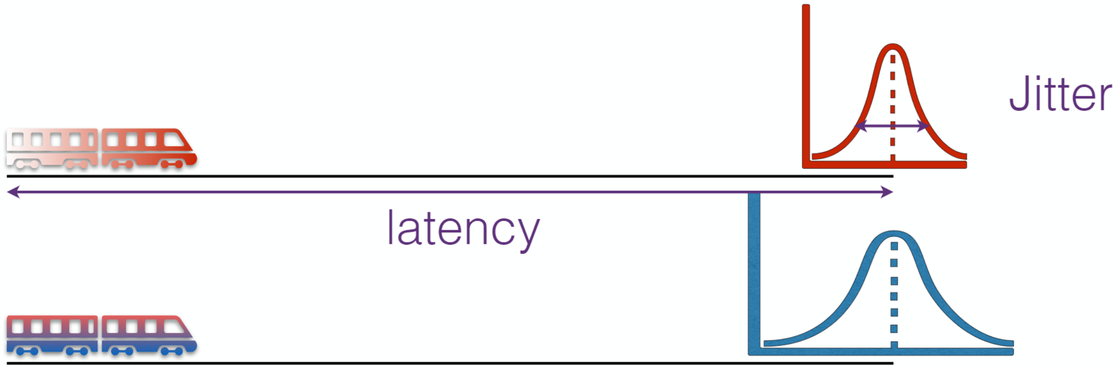
Jitter





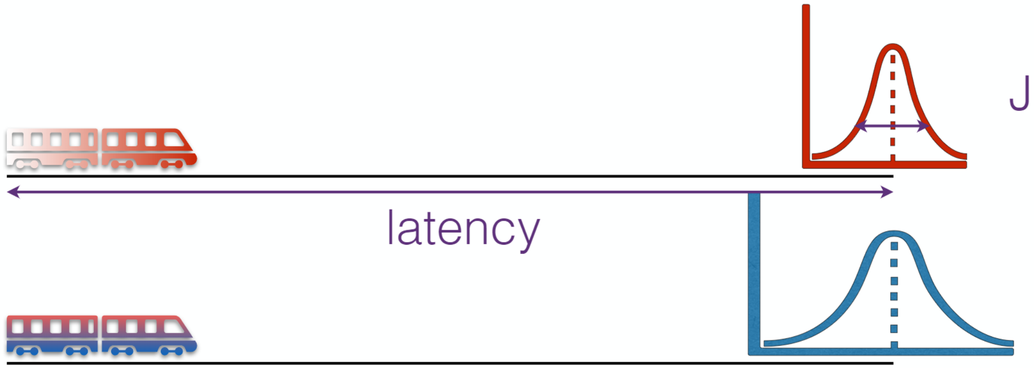
- Jitter: noise in a periodical signal
  - The frequency of the noise is ambiguous!
  - Stating a jitter requirement without a frequency range does not make too much sense…
  - Types of jitter are also important.

Jitter

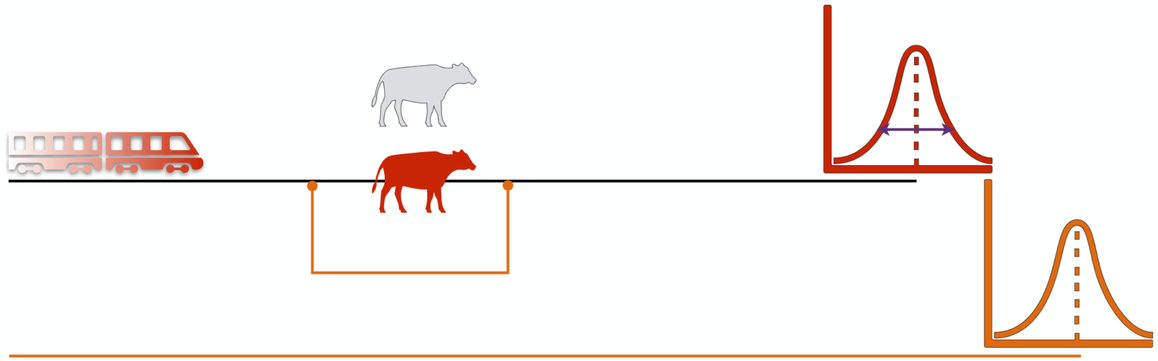


The Random Jitter with a Gaussian distribution.

Jitter

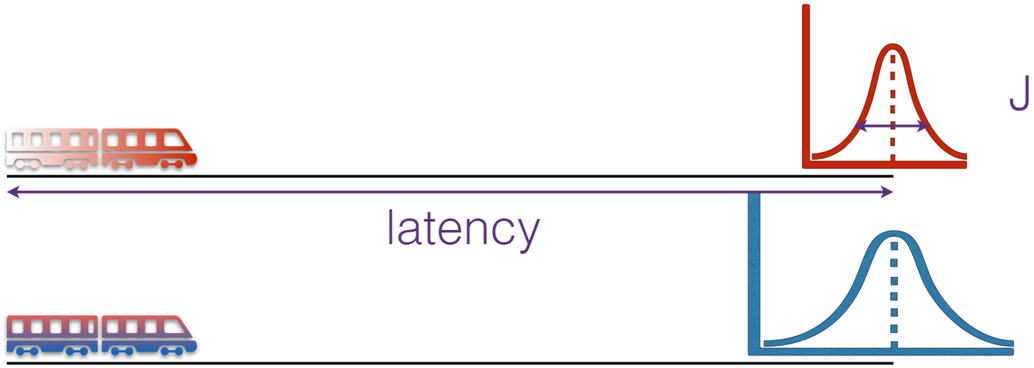


The Random Jitter with a Gaussian distribution.

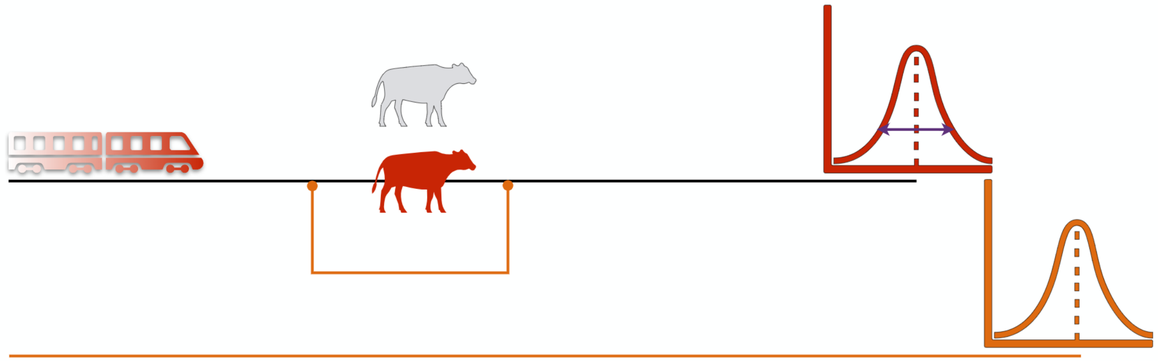


- The Deterministic Jitter with a bimodal Dirac delta distribution.

Jitter

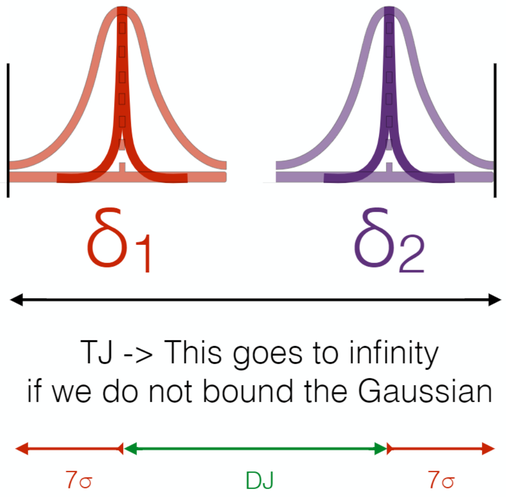


The Random Jitter with a Gaussian distribution.

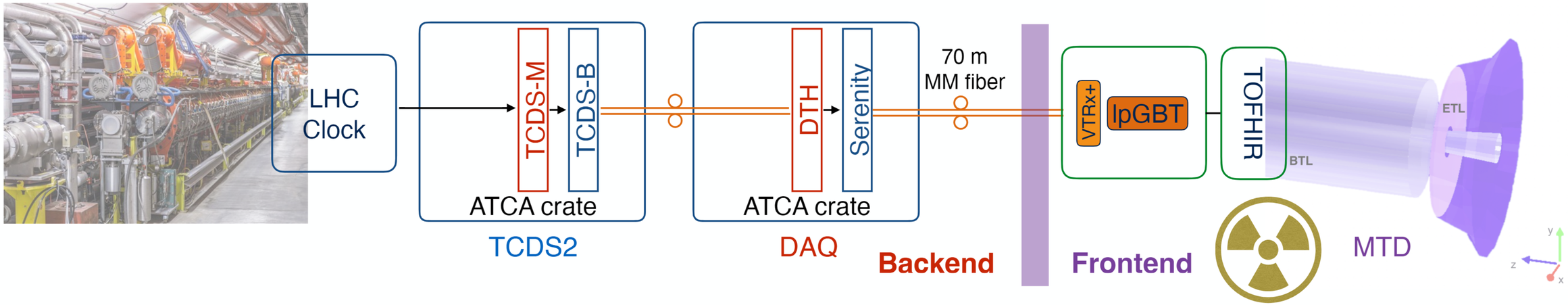


- The Deterministic Jitter with a bimodal Dirac delta distribution.

- Random jitter is unbounded:
  - A typical standard is to estimate the peak-to-peak jitter at 10^{-12} BER (~14 sigma)
  - So Total Jitter (10^{-12} BER) = 14xRJ+DJ
  - DJ is mostly caused by design faults (noisy power supply, trace interference etc)

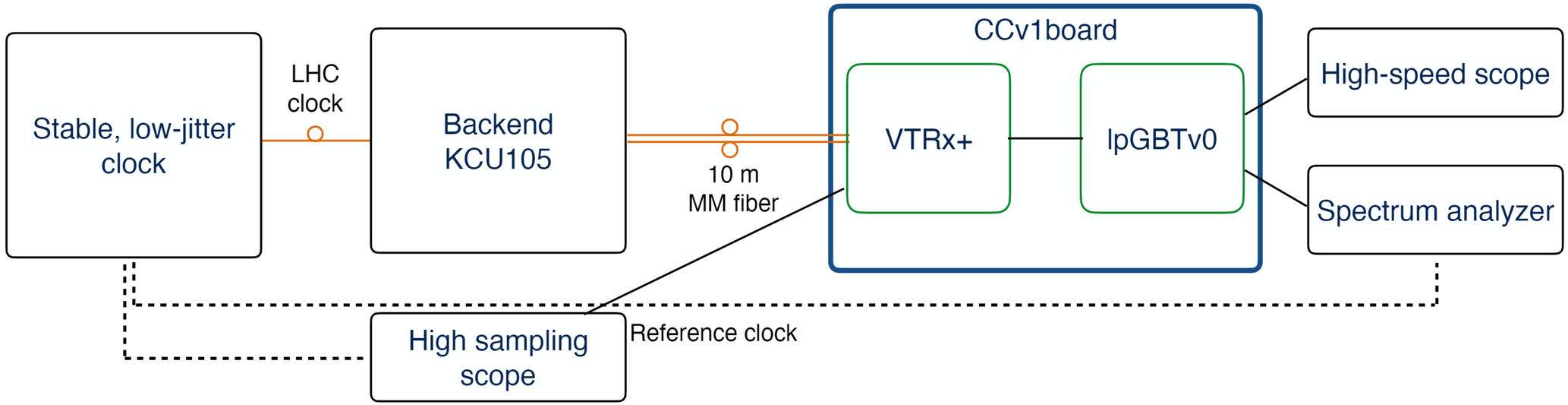


Characterization



- We characterized each component on the clock distribution tree individually:
  - CEA Saclay CMS timing lab, CERN HPTD lab, CERN b27
  - High speed scopes with large memory, noise spectrum analyzers!
- Increase test system complexity step by step:
  - Considering various operation conditions

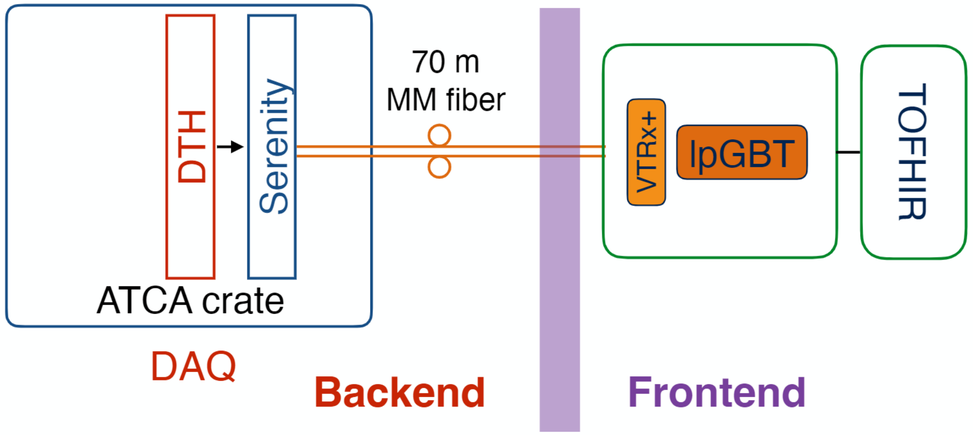
BTL RU (v1) measurements



- Xilinx KCU105 as DAQ backend
- CC board:
  - Single link similar to **lpGBTv0** CB ~ 6 ps
  - Link-to-link ~ 9 ps
  - Data activity: 2 ps impact on DJ, minor effect on RMS

eClock (MHz)	RMS (ps)		RJ (ps)		DJ (ps)	
	Direct	PoI inverted	Direct	PoI inverted	Direct	PoI inverted
40	2.8	2.8	2.6	2.6	1.8	1.7
160	6.1	9.0	2.5	2.3	14	23

What is if we have a more complex backend?

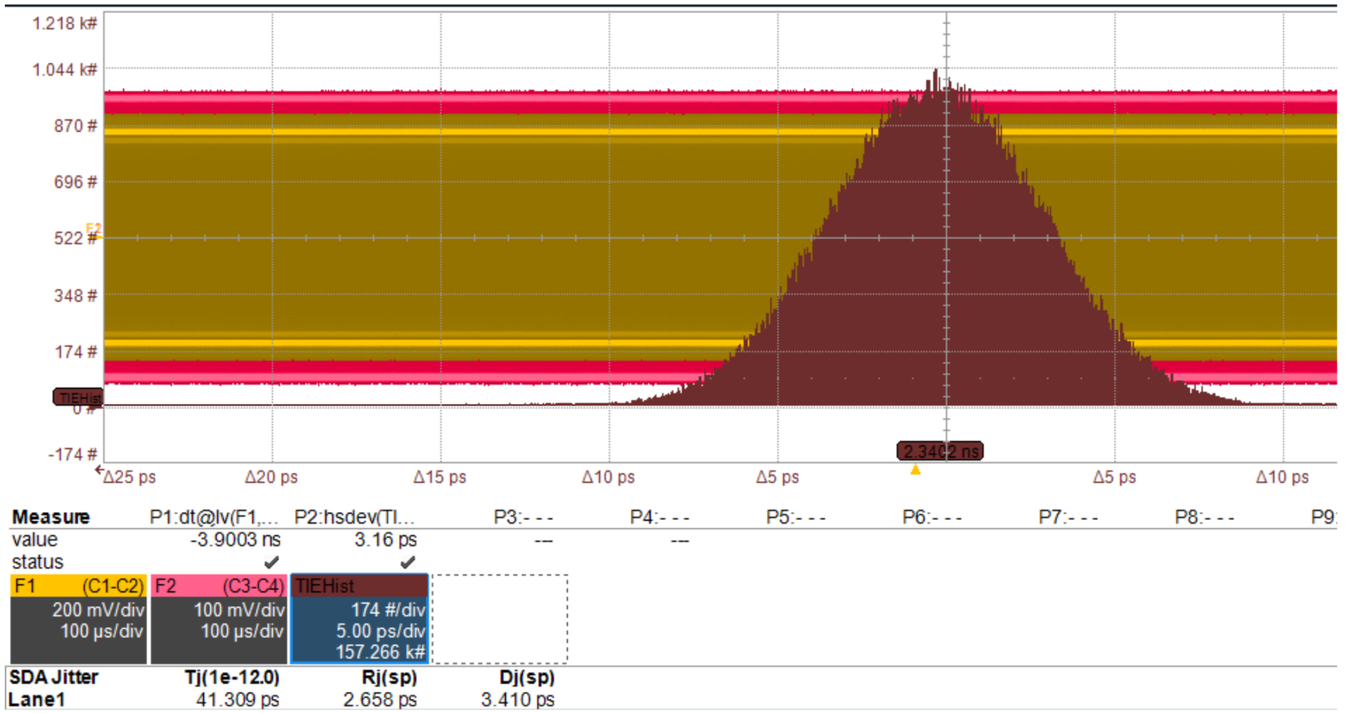


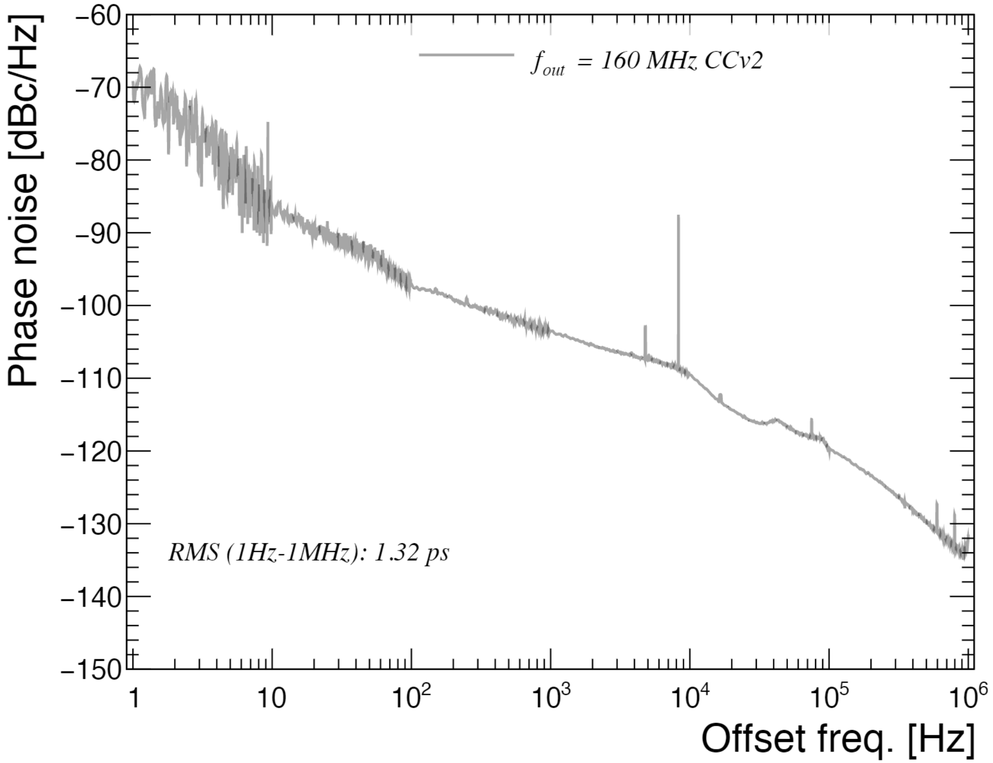
eClock (MHz)	RMS (ps)			
	Reference KCU105	1 link	40 links	40 links (80C<T)
160	(6.1)	5.8	5.9	6.5

Baseline clock distribution:

- Serenity and DTH boards within ATCA crate performs better than KCU105 with a single lpGBT link
  - Overall well within the specifications

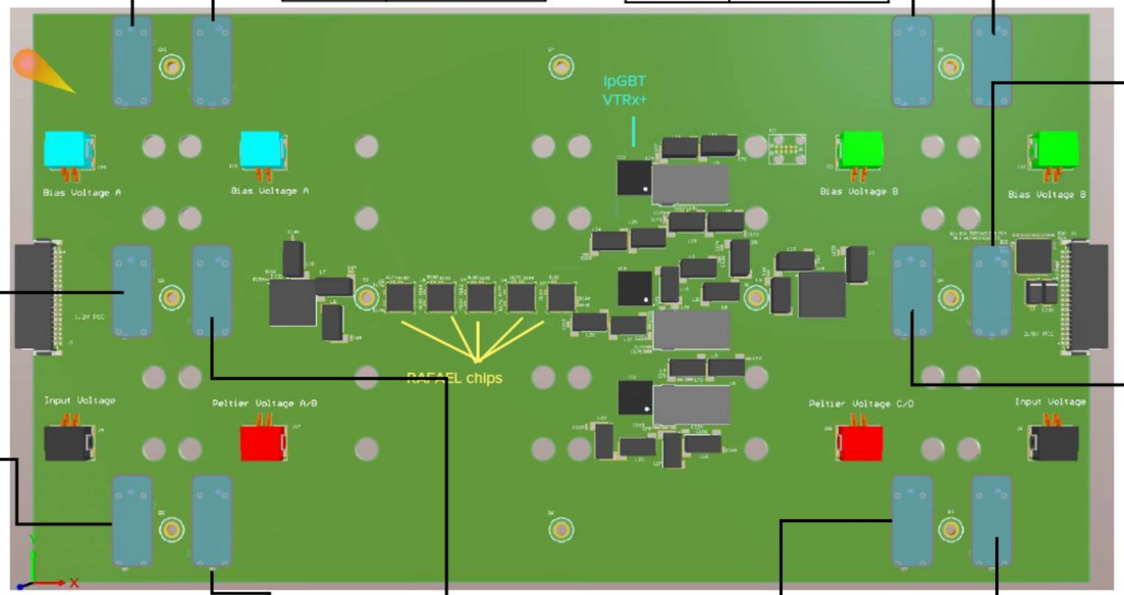
BTL RU (v2) measurements





- In the second version of the boards we decided to use a second lpGBT as a PLL!
- 3.2 ps RMS jitter
  - **Significant improvement wrt CCv1**

Validation of all clock channels



sdev	3.23 ps
Tj	42.40 ps
Rj	2.71 ps
Dj	3.62 ps

sdev	3.24 ps
Tj	41.70 ps
Rj	2.66 ps
Dj	3.70 ps

sdev	3.02 ps
Tj	40.46 ps
Rj	2.60 ps
Dj	3.34 ps

sdev	3.20 ps
Tj	41.14 ps
Rj	2.64 ps
Dj	3.43 ps

sdev	3.40 ps
Tj	41.79 ps
Rj	2.57 ps
Dj	5.13 ps

sdev	3.26 ps
Tj	41.37 ps
Rj	2.61 ps
Dj	4.12 ps

sdev	3.31 ps
Tj	40.74 ps
Rj	2.51 ps
Dj	4.91 ps

sdev	3.29 ps
Tj	42.30 ps
Rj	2.70 ps
Dj	3.73 ps

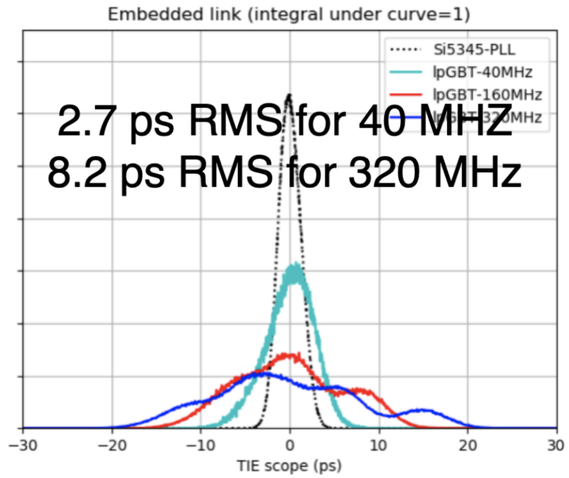
sdev	3.29 ps
Tj	42.45 ps
Rj	2.71 ps
Dj	3.82 ps

sdev	3.32 ps
Tj	40.99 ps
Rj	2.7 ps
Dj	4.34 ps

sdev	3.20 ps
Tj	40.55 ps
Rj	2.58 ps
Dj	3.81 ps

sdev	3.31 ps
Tj	42.78 ps
Rj	2.76 ps
Dj	3.60 ps

Why was the second lpGBT PLL useful?



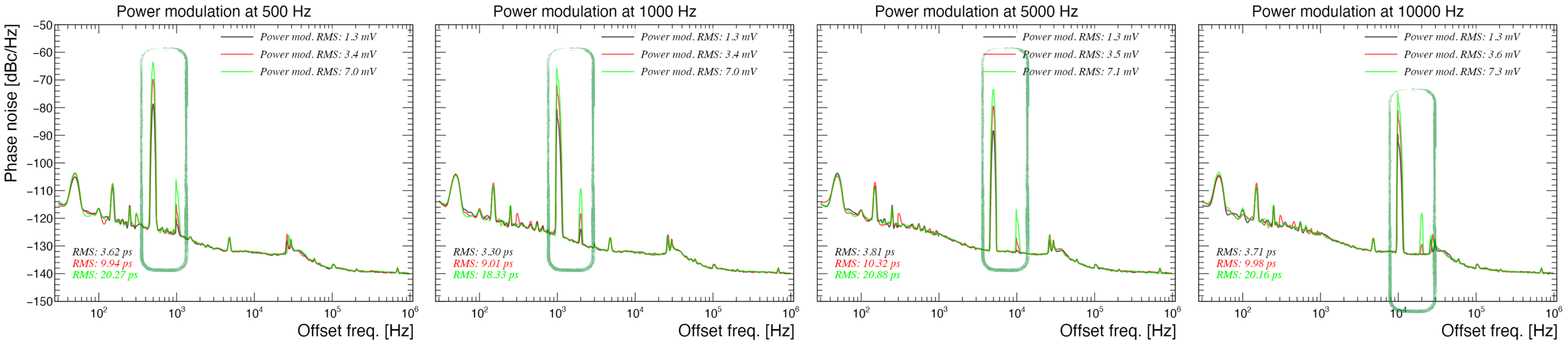
- lpGBTv0 introduced a Nx40 MHz jitter in transceiver mode.
  - The second lpGBT was operating in the simplex transmitter mode.
  - It cleaned the jitter of the first ASIC.

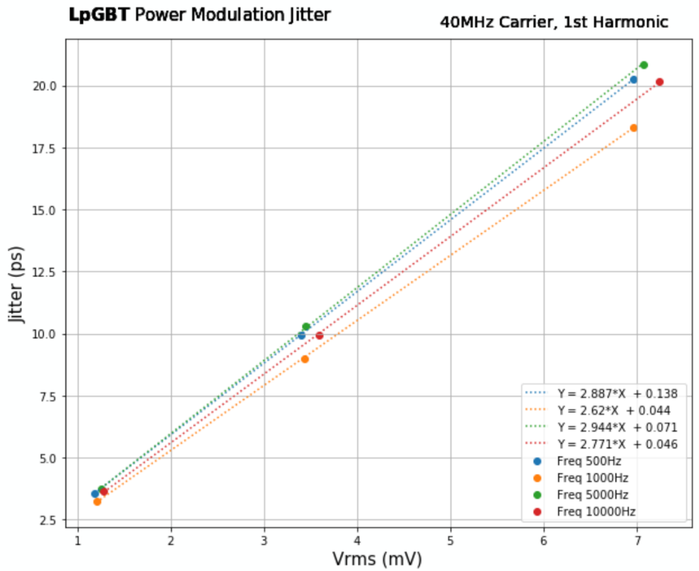
With the lpGBTv1 this issue is significantly reduced so we do not need any additional lpGBT in the front-end for the clock distribution.

So are we done?

- Well not really:
  - All is good in the lab under stable external conditions.
  - However we know that temperature and power fluctuations have huge impact in the timing performance!

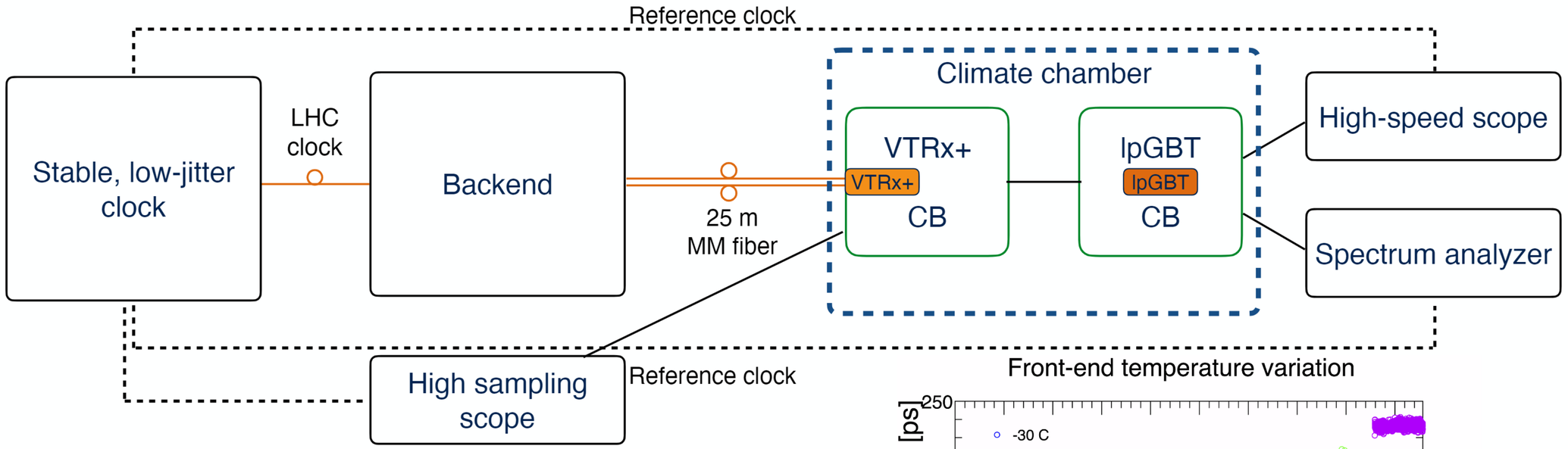
Power modulation tests



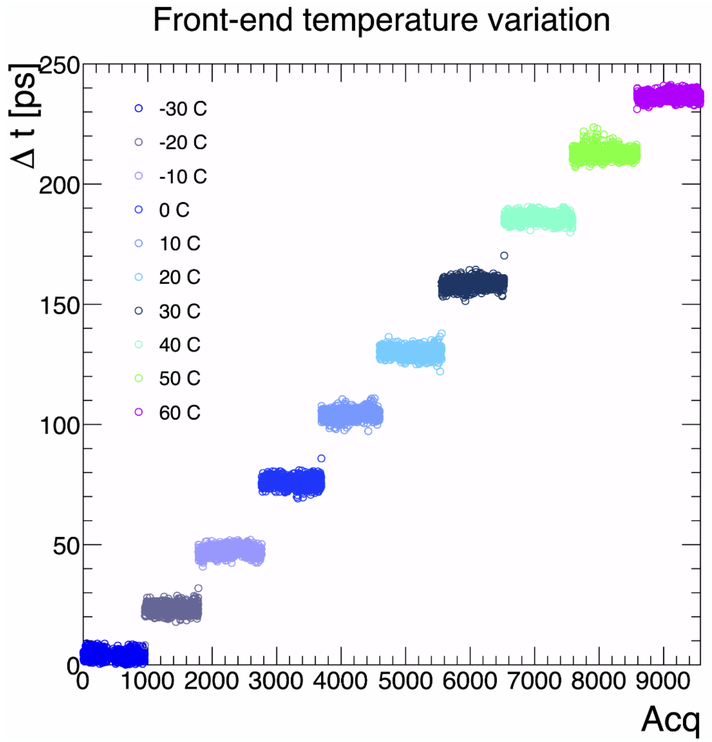


- The phase noise is measured within the range of 30 Hz to 1 MHz.
  - The corresponding RMS jitter is quoted on the graphs. The jitter scales linearly with the injected noise.
  - **2.8 ps RMS jitter per mV RMS modulation is observed.**

Temperature tests



- lpGBT is measured to have 3 ps/C and 3 ps/mV variation.
- FE (lpGBT + VTRx+) temperature variation:
  - Scope measurement:
    3.1 ps/C for clock



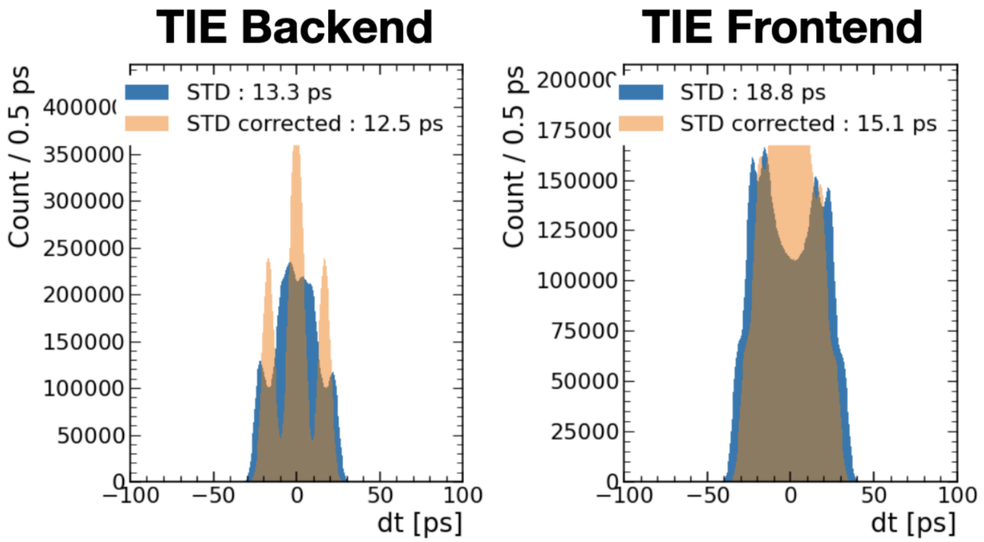
So are we done?

- So actually we are not there yet:
  - **The detectors are colossal and intricate!**
    - **Operating under extreme conditions**
  - We cannot control all these external factors stable!

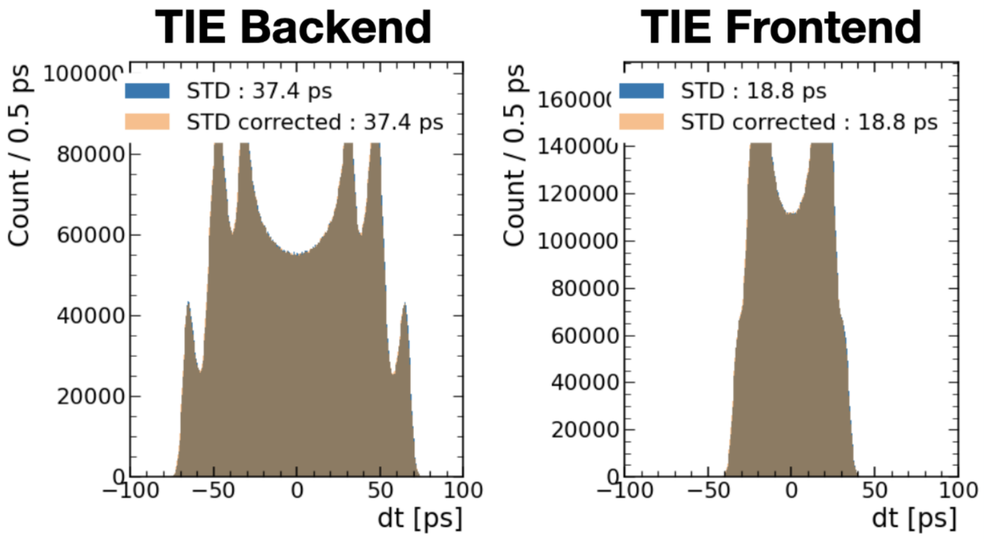
Advanced monitoring tools are only solution!

DDMTD

So are we done?



DJ at 100 Hz and N = 8192



DJ at 100 kHz and N = 8192

We at CEA Saclay working on extensive simulation tools where these techniques can be tested (not just in hardware but in software as well)

But maybe that is a topic for a second discussion!