Proposed (eRD109) readout R&D for pECAL with on-detector waveform digitizing

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9/26/2022 EPIC Calor. Meeting

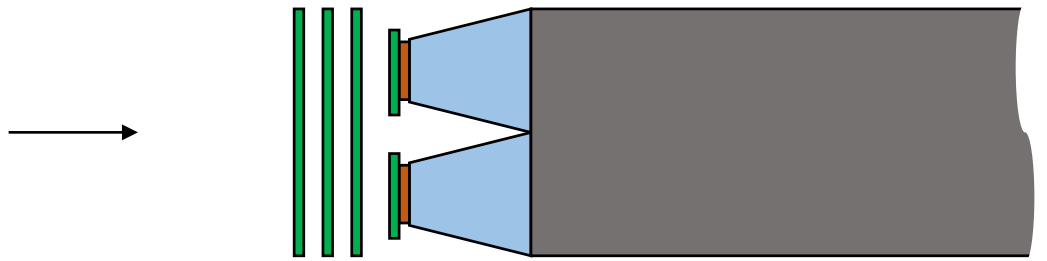
eRD109 proposal

- a 3 year plan to design and prototype readout for pECAL
- on-detector digitizing, **with emphasis on minimizing cables & services**
- to be used with a (possibly 'generic') Frontend Processor (FEP) to aggregate data to DAQ fiber links
  - not in scope of this proposal
  - but a simple test DAQ is
- readout scheme:
  - continuous waveform digitizer (14 or 12 bit at 49.25 or 98.5 MHz, or async 50 – 80 MHz)
  - detect hits in waveform data, form hit-waveform records w/ timestamp
  - push out streaming data in timestamp order
- implementation:
  - stack of several PCB's, interconnect to SiPM carriers TBD but certainly design for easy replacement of readout
  - first version based on COTS ADC & FPGA
  - final version *may* replace with ASIC

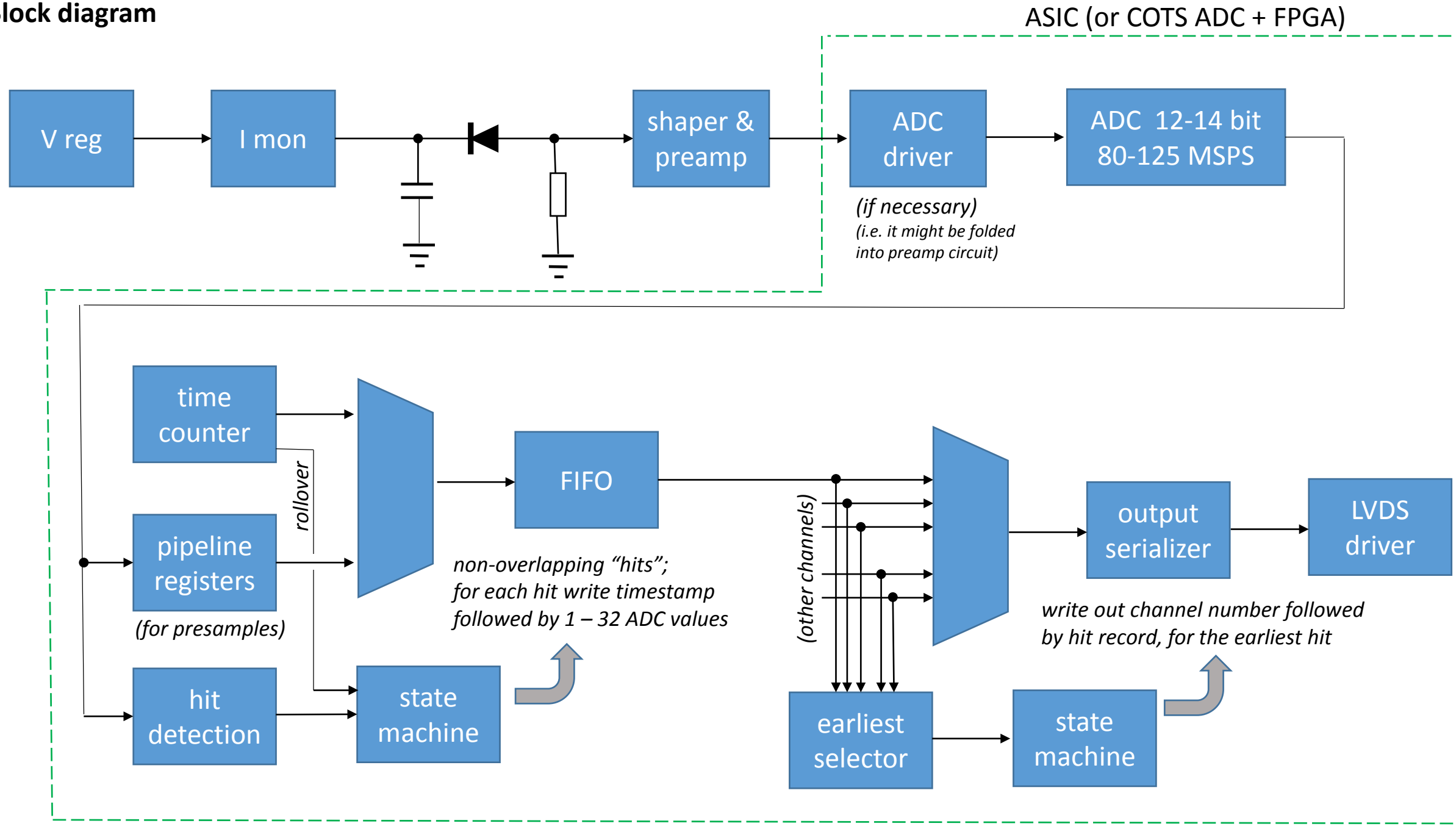
Schedule

The rough schedule for this effort over 3 years is shown in Fig. 2:

	FY23				FY24				FY25			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Select ADC & FPGA												
Develop frontend specifications												
Improve STAR FCS bias & preamp												
Firmware development												
ASIC evaluation (TBD)												
Power design												
PCB design and fabrication												
Bench tests												
Cosmic ray tests												
FNAL beam tests												
Tests at STAR												
Revise PCB (tbd w/ ASIC)												



Block diagram



requirements and characteristics – for discussion

- 16 channel assembly
- dimensions: 9.9 × 9.9 × 3 cm^3
- further 4 cm space for cables and cooling (7 cm overall thickness)
- power: 120 mW/ch (16k ch: 1.9 kW)
- peaking time: 80 ns
- ADC: 14 bit, 49.25 MSPS
- samples on hit waveform: 8
- SiPM capacitance: 8 nF
- SiPM gain: TBD, *function of radius*
- full scale signal: 60-100k pixels ?? (seems too high, we have only 57324 pixels in 4x S14160-6050HS!)
- pECAL light yield: 1000 pixels/GeV (goal)
- SiPM DCR (after irrad.): TBD, *function of radius*
- dark counts in pulse: TBD (roughly 80 ns × DCR)
- minimum working signal: TBD, *function of radius*
- linearity (electronics only): 0.1%
- rate capability: **firm >50 kHz** per channel
- hit data size: 18 bytes
- max output (to FEP) data rate: 14.4 MB/s @ 50 kHz
- output bandwidth: 16 MB/s
- timestamp size: 24 bit (340 ms rollover)
- rollovers marked in datastream
- SiPM bias control: per channel DAC
- SiPM bias compensation: per channel thermistor, common slope DAC
- SiPM bias current monitor
- input supply monitor
- on-board supply voltage regulation
- slow controls: multidrop I^2C

Data format, size, rates

Output data format (per hit)

1. Timestamp 24 bits
2. Channel number 4 bits
3. Flags 4 bits (rollover, overrun, …)
4. ADC data N*14 bits (N*12), 1≤N≤32 (N≤8 for physics running)

Hit is fixed (N-dependent) length, say 144 bits or less for physics running

If no hit to send, send a suitable variable-length idle sequence on output link to be dropped by receiver; idle format designed so that next hit data start is identifiable.

Having the timestamp first simplifies (IMHO) merging data downstream in time-ordered way.

Hit rate up to 50 kHz average on all channels simultaneously.
→ Output data rate up to 14.4 MB/s.

No buffer is needed on output of FEE, it *never* waits to send.
Per-channel buffers (depth O(100) hits) only need to handle peak fluctuations in rates. Will be sized to drop less than 10^{-7} of the hits, for instance.
If (rarely!) any hits are dropped the number dropped will be marked in the datastream.

Some key questions…

1. How many samples should be used? (What's the experience from FCS analysis, other experiments?)
2. Should the sampling clock be related to bunch crossing clock 98.5 MHz (e.g. /2 is perhaps nice)?
    - Probably not essential. But *using a related clock avoids having to cross-reference timestamps* downstream, though that should be feasible.
3. What linearity (of the electronics, neglecting inherent SiPM nonlinearity) is really needed?
4. Minimum energy threshold for hits may have to be higher near the beampipe, due to radiation damage. Need to work out details on that.
5. Does 4 cm space for SiPM + FEE + cables sound good enough?

FEP questions (far future):

1. How many FEB per FEP? I think we can assume 16 but it may depend on connector choices/sizes.
2. How many bits of timestamp need to be sent from FEE to DAQ (i.e. on the fiber link)?
3. Would we do feature extraction on the (future) FEP board? (Sending hit time and amplitude instead of all the raw samples.)

Testing goals (FY24/25)

- Demonstrate readout performance, with measured power and temperature rises
- Provide readout for test beam for detector R&D
- Check for operational issues or damage from radiation in STAR
    - Possibly conduct other radiation damage studies on the readout
- Check rates due to SiPM dark counts with irradiated SiPM
- Demonstrate reliable and simple connections and mechanical interfaces

BACKUP SLIDES

Realization with standard COTS ADC + FPGA – leading contenders

$10 per channel, 10.4 mm^2 PCB area per channel
same chip as on STAR DEP

ANALOG DEVICES

Octal, 12-Bit, 40/80 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9637**

FEATURES 60 mW/ch 71.5 dB SNR

- Low power: 60 mW per channel at 80 MSPS with scalable power options
- SNR = 71.5 dBFS (to Nyquist)
- SFDR = 92 dBc (to Nyquist)
- DNL = ±0.4 LSB (typical), INL = ±0.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p differential input voltage range
- 1.8 V supply operation

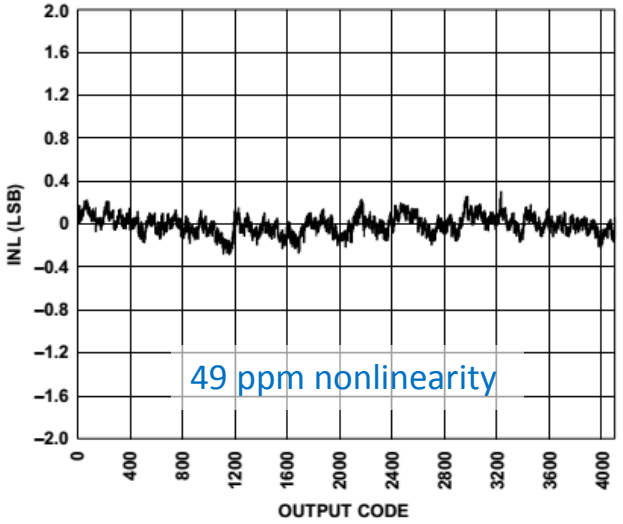
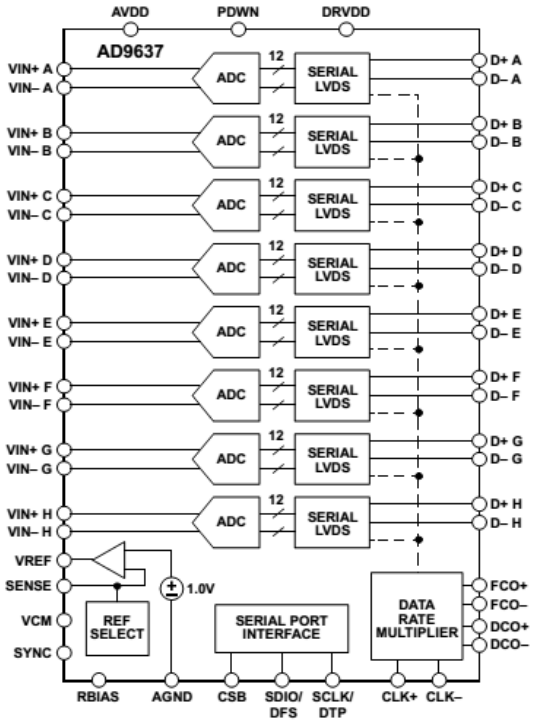


Figure 19. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

FUNCTIONAL BLOCK DIAGRAM



$10 per channel, 6.4 mm^2 PCB area per channel

ANALOG DEVICES

16 Channel, 14-Bit, 65 MSPS, Serial LVDS, 1.8 V ADC

Data Sheet **AD9249**

FEATURES

- Low power 58 mW/ch 75 dB SNR
  - 16 ADC channels integrated into 1 package
  - 58 mW per channel at 65 MSPS with scalable power options
  - 35 mW per channel at 20 MSPS
- SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)
- DNL: ±0.6 LSB (typical); INL: ±0.9 LSB (typical)
- Crosstalk, worst adjacent channel, 10 MHz, –1 dBFS: –90 dB typical
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation

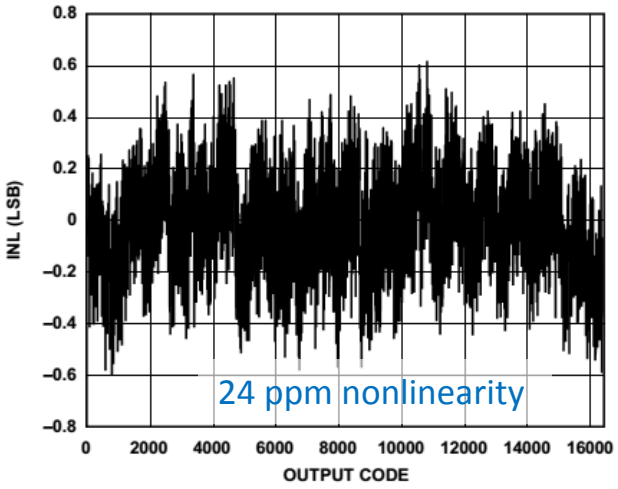


Figure 19. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

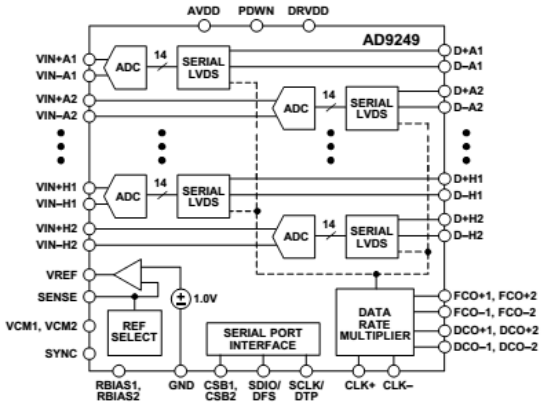


Figure 1.

Could run at ½ bunch crossing clock, 49.25 MHz
50 mW/ch

Realization with ASIC (perhaps)

Pacific MicroCHIP Corp.

A 32 Channel ASIC for X- and Gamma-Ray Energy and Timing Measurement

Keywords: Event building, Streaming readout, X-ray detector readout, Gamma-ray detector readout

Technical Summary

Pacific Microchip Corp. has developed a power efficient 32-channel ASIC (1st generation) for X- and gamma-ray energy and timing measurement with a digital event building back-end.

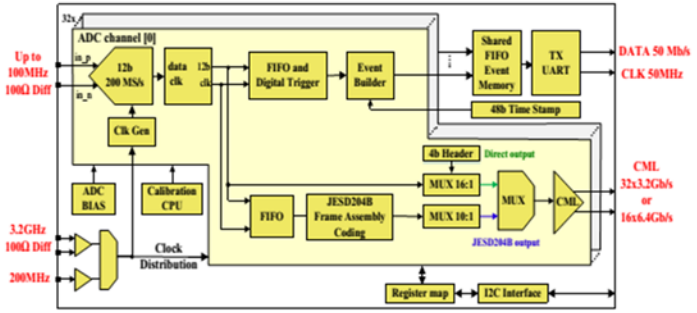


Figure 1. A block diagram of the ASIC.

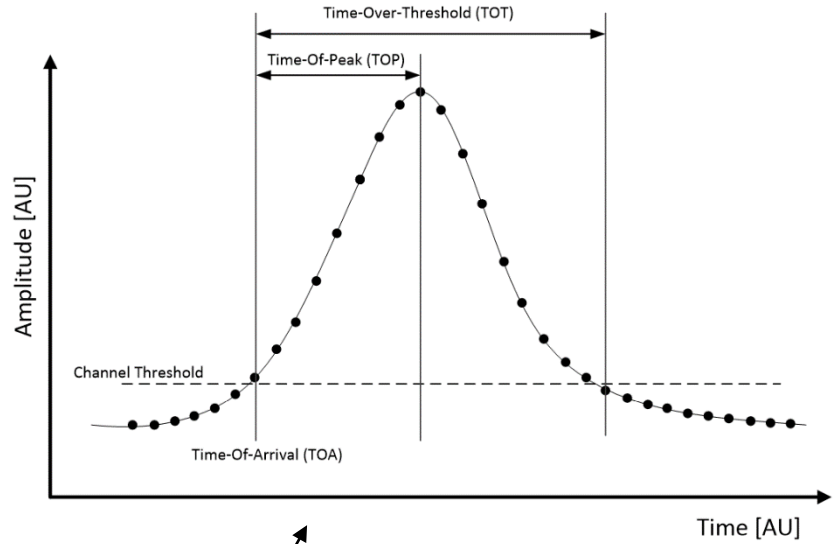
Figure 2. A chip photo (left), BGA package (center) and the

Targeted Operational Capabilities

The ASIC offers low power consumption (4.5mW/ch) combined with complex functionality required for signal digitizing and extracting of event related data (time of arrival, threshold, time of peak, peak value, time over threshold, etc.). This data is assembled into packets and shipped out through an UART interface. Specific parameters/capabilities:

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB > 10-bit
- Input signal bandwidth > 0.2GHz
- Integrated 32ch event-building digital back-end
- Optional direct ADC output through JESD204B interface
- Event data packet output through UART interface
- Power consumption < 4.5mW/channel (JESD204B is off)
- Total power with ADC data interface <880mW.
- I2C interface for ASIC control
- Chip layout footprint 7.8mm^2
- 15mm x 15mm 324 ball BGA package

Development Objectives & Milestones



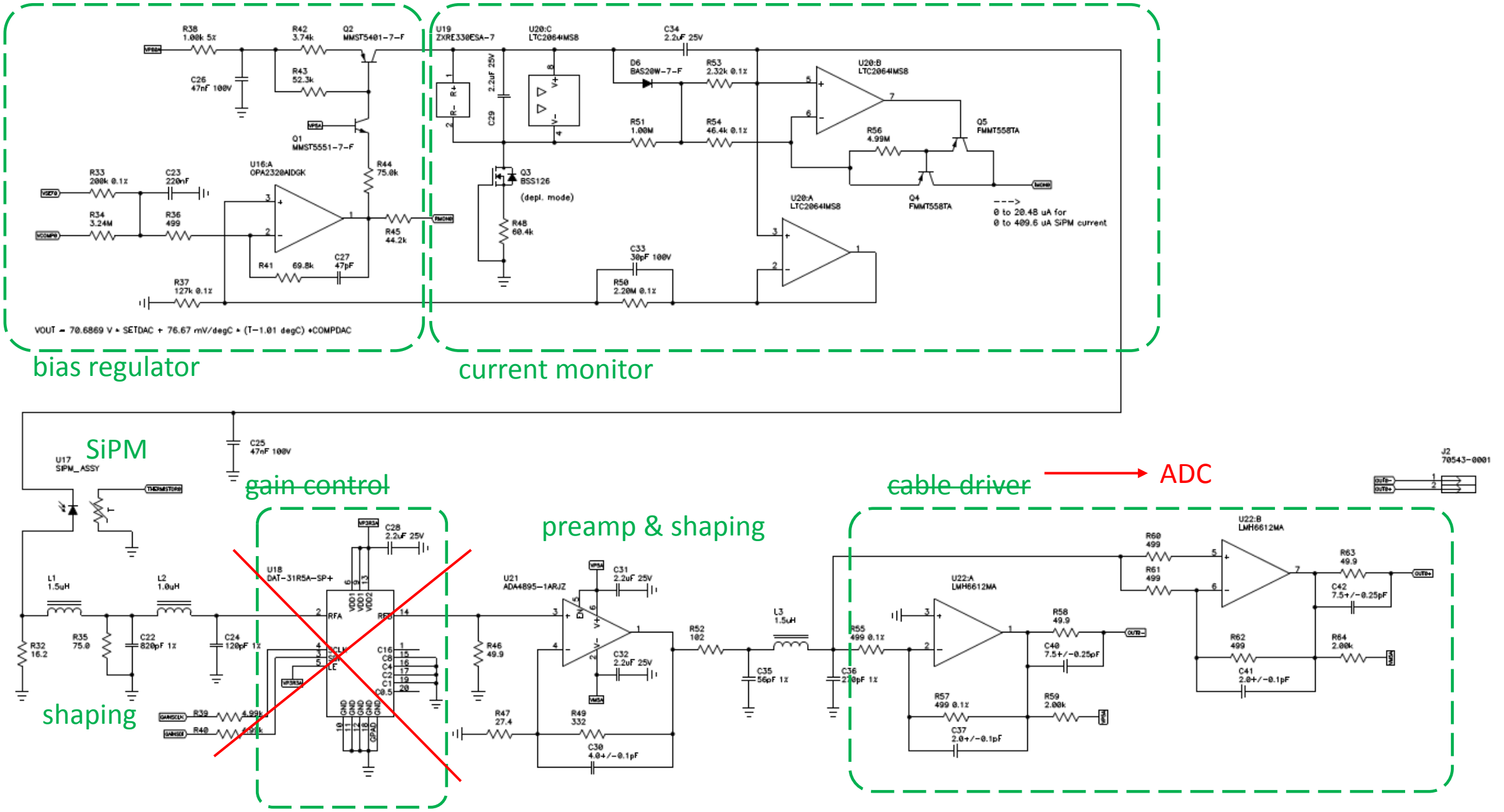
- Price $39 /ch
- Output bandwidth 6.25 MB/s (not enough probably)
- Data clock sent separately (we rather have embedded)
- Hit record (in current design) 126 bits, comparable to our expectations. [Assume → buffering is about right.]
- All controls by I^{2}C – nice!

- In current design, samples are NOT stored except for peak value. They do time, TOT, and peak value/time. This is probably **not** good enough for us.
- There's a 2 month window (i.e. To ~Nov. 1st) to try to influence feature changes for new version of the chip. They are already thinking about BW improvement.

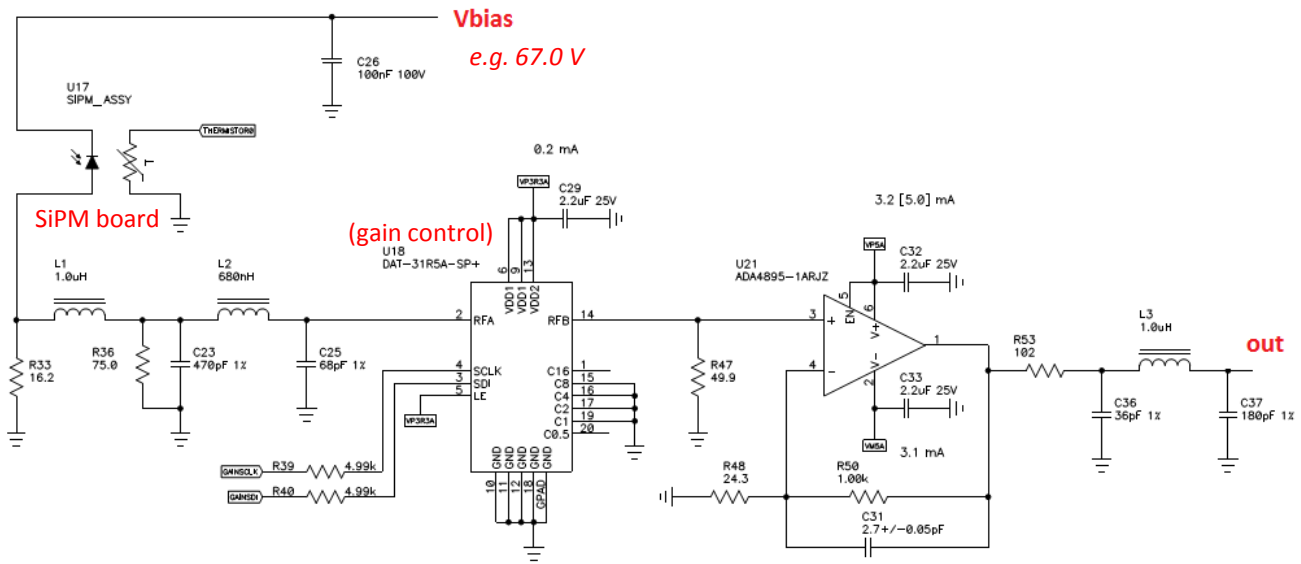
readout essentials, similar to STAR FCS

- Integrated precision SiPM bias and temperature compensation – stable gain
- Low impedance loading of SiPM – stable and linear gain
- Some shaping before amplification – stable and linear gain
- Low noise preamp
- Fully DC coupled – stable baseline
- Continually digitize waveform
- Identify hits, do streaming readout of hit records
- Hardware as simple as possible
- Especially the cables and interfaces on detector as simple as possible
    - Slow controls: Bussed I^2C to multiple FEE

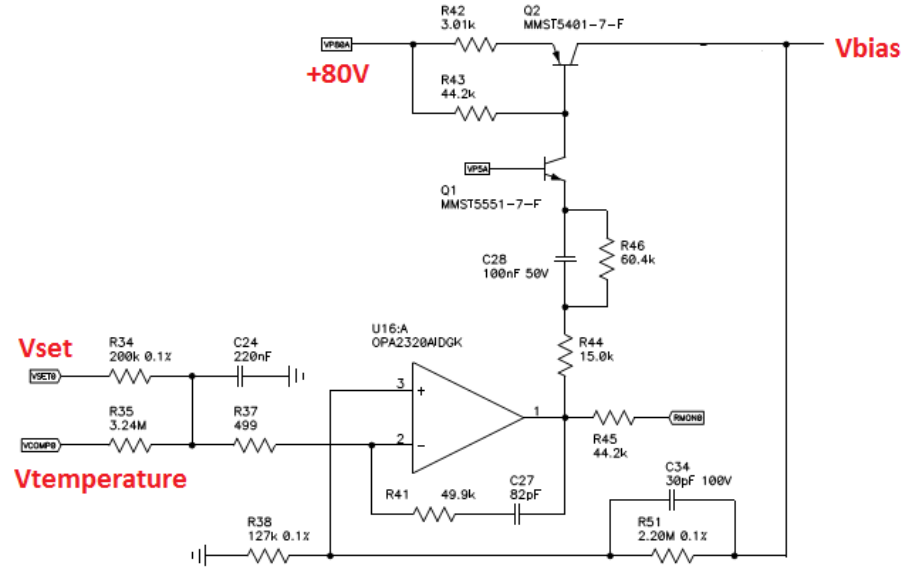
complete bias and signal schematic of one channel STAR FCS FEE, and changes for pECAL



FCS frontend and bias



- ECAL 4×, HCAL 6× 3×3 mm^2 SiPM's
- SiPM with **small** load resistor, followed by voltage amplifier
  - for best possible linearity and gain recovery – *speed and linearity of the amplifier are not involved in sweeping charge out of SiPM*
- some shaping before amplification – so that amplifier *does not have to linearly follow pulse as fast as SiPM produces*
- more shaping after the amplifier – for noise limiting
- fully DC coupled through to ADC – *stable pedestals*
- for STAR we included gain control for better cosmic ray calibration; this could be omitted…



- simple but precise, low noise bias voltage regulator
- inherent current limiting – *no series resistor needed to protect SiPM*
  - more stable bias voltage → more stable gain
- fast recovery 3 µs to 2 mV after full scale signal pulse
- current monitor (not shown above) – optional, but useful!
- Vset and slope of Vtemperature set by DAC's