FY22 Report and FY23 Proposal on EIC AC-LGAD R&D

eRD112

October 2, 2022

Executive Summary

In FY22, we advanced the development of AC-LGAD sensors and frontend readout ASICs for EIC applications. Sensors designed and fabricated by BNL IO for EIC have shown promising timing and spatial resolutions with beam. Design and submission of the first version of frontend ASICs dedicated to read AC-LGAD sensors have been completed with encouraging initial results from beta sources.

In FY23, we propose to continue the sensor and frontend ASIC development, and start looking into sensor/ASIC integration, frontend electronics, and light-weight mechanical structures. We will continue the sensor development and design optimization with BNL IO to utilize its great flexibility and fast turnaround time, and engage commercial vendors to produce large area sensors to understand their yield/cost and quality. We will design and submit the second version of frontend ASICs, while completing the testing of the first version ones in the lab and with beam. The proposed work on sensor/ASIC integration, frontend electronics and mechanical structure will be important to have a complete and validated design of AC-LGAD detector systems for the upcoming DOE CD2/3a review.

To carry all these works in FY23, we request 462k$ funds for sensor, sensor/ASIC integration, and light-weight mechanical structure R&D. In addition, we request 267k$ for frontend readout ASIC and electronics development. The latter is also presented in a separated document submitted via eRD109 dedicated to ASIC and electronics R&D.

Contents

1 Introduction

In March 2021, Brookhaven National Laboratory (BNL) and Thomas Jefferson National Accelerator Facility (JLab) together issued a call for Collaboration Proposals for Detectors at the EIC [1]. Three proto-collaborations (ATHENA, CORE and ECCE) formed and submitted three proposals. All the proposals utilize the AC-coupled Low Gain Avalache Detector (AC-LGAD) technology for Time-of-Flight (TOF) particle identification (PID) and tracking in the central detector, and timing measurement and tracking in the far-forward direction. In March 2022, the EIC Detector Proposal Advisory Panel announced its recommendation to choose the ECCE proposal to be the reference design for the EIC project detector. Since then, a new collaboration (EPIC) has been formed to work on the technical design of the detectors in preparation for the DOE CD2/3a review anticipated in October 2023. Specifications of the AC-LGAD detectors for EPIC are summarized in Tab. 1 and discussed below. Note that the requirements on the timing and spatial resolutions and material budget are still being evaluated and are subject to changes as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

	Area (m^2)	Time resolution	Spatial resolution	Material budget
Barrel Timing Tracking Layer	11	30 ps	30 μm in $r \cdot \phi$	0.01 X_0
Endcap Timing Tracking Layers	1.2+2.2	25 ps	30 μm in x and y	0.08 X_0
B0 Tracker	0.07	30 ps	$500/\sqrt{12}$ μm	0.01 X_0
Roman Pots	0.14	30 ps	$500/\sqrt{12}$ μm	no strict req.
Off-Momentum Detectors	0.08	30 ps	$500/\sqrt{12}$ μm	no strict req.

Table 1: Specifications of AC-LGAD detectors for EPIC, the EIC project detector. The timing and spatial resolutions are given for single hits, while the material budgets are given per detector layer.

1.1 AC-LGAD for the Central Detector

The central EPIC detector includes the following AC-LGAD detectors (see Fig. 1):

- Electron Timing and Tracking Layer (ETTL) with a single layer of pixel sensors at $-171 < z < -161$ cm, with an inner radius of 12 cm and outer radius of 64 cm.
- Central Timing and Tracking Layer (CTTL) with a single layer of strip sensors at $62.5 < R < 65.5$ cm with a total length of 270 cm.
- Forward Timing and Tracking Layer (FTTL) with a single layer of pixel sensors at $155.5 < z < 170.5$ cm, with an inner radius of 12 cm and outer radius of 85 cm.

The layouts of these detectors are shown in Fig. 2. The CTTL follows the STAR Intermediate Silicon Tracker design [2], while the ETTL/FTTL follow the CMS Endcap Timing Layer design [3]. The CTTL consists of 288 tilted staves, each of which is 135 cm long. AC-LGAD strip sensors are mounted on low mass Kapton flexible circuit boards (hybrids), and are wire-bonded with front-end ASICs. The hybrids are glued onto mechanical structures made from low density Carbon-Fiber (CF) materials, and bring power and input/output signals to the sensors and ASICs. The heat generated by the frontend ASICs are removed by an embedded Aluminium cooling tube in the CF structure. The ETTL/FTTL consist of detector modules made from AC-LGAD pixel sensors bump-bonded with front-end ASICs. These detector modules are mounted from both sides onto a thermal-conductive supporting disk with embedded liquid cooling lines. Since the irradiation flux at the EIC is much smaller than that at the LHC, it is assumed that the radiation damage will not be a concern and the AC-LGAD sensors can be operated at room temperature.

With single hit timing resolution of 25 ps, the CTTL and ETTL/FTTL can separate pions and kaons at the 3σ level for $p_T < 1.2$, and $p < 2.5$ GeV/c, respectively. By combining the PID information from the AC-LGAD detectors and Cherenkov detectors, EPIC will have excellent PID capability over a wide momentum range in a nearly 4π acceptance, which is crucial to achieve the goals of the EIC physics program. Besides precise timing resolution, AC-LGAD sensors can also provide precise spatial

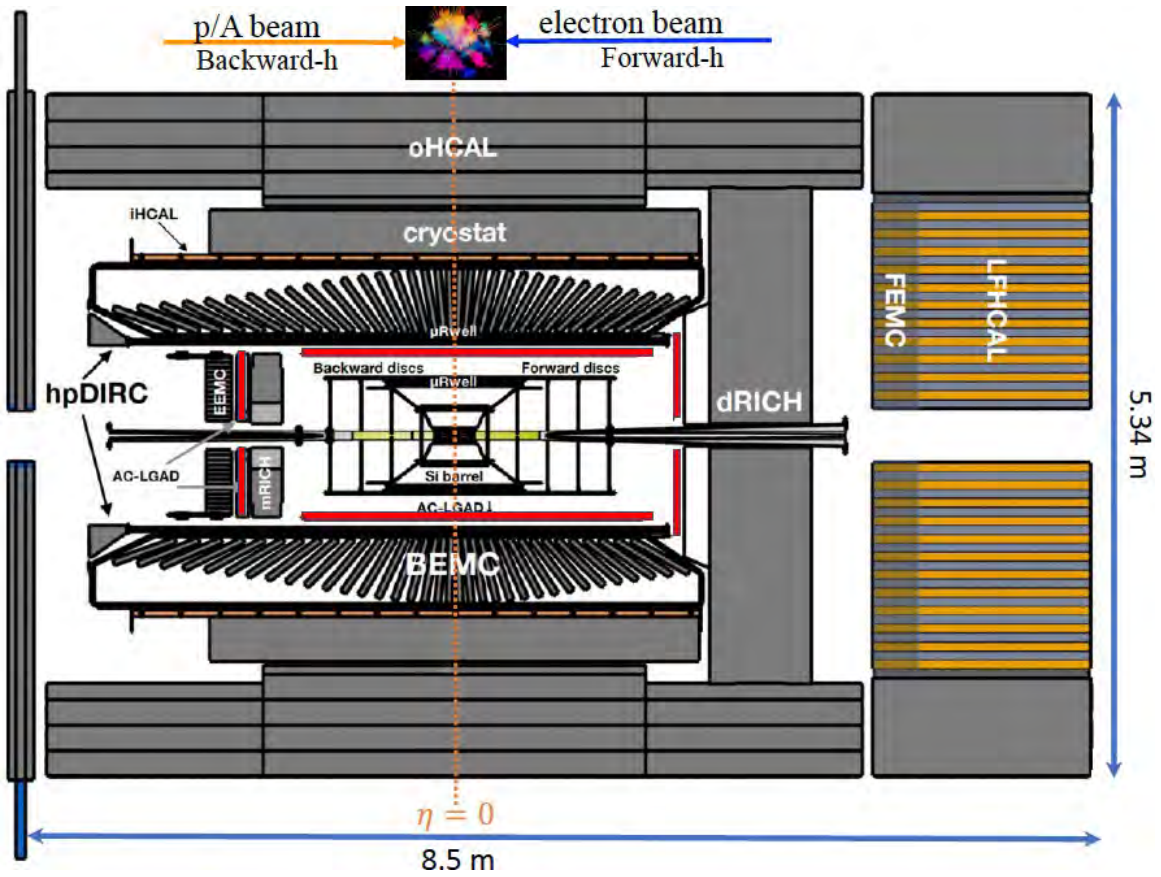


Figure 1: Layout of the central detector of the EPIC detector reference design, which includes a AC-LGAD Timing and Tracking Layer detectors (in red) in the backward, central, and forward directions.

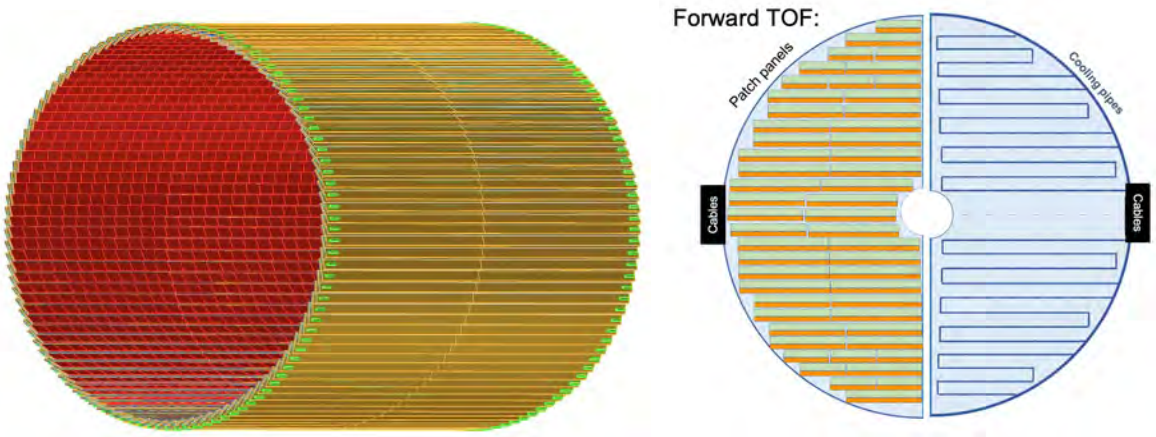


Figure 2: Layout of the EPIC AC-LGAD TTL detectors in the barrel (left) and endcap regions (right).

resolution, and thus aid track reconstruction and momentum determination. The requirements on the timing and spatial resolutions, as well as the material budgets of the TTL detectors are being evaluated in EPIC MC simulation to find the optimal configuration without over-designing these detectors.

1.2 AC-LGAD for Far-Forward Detectors

The EIC physics program includes a strong emphasis on exclusive and diffractive final states, which produce charged and neutral particles at $\eta > 4.5$, outside of the main detector fiducial acceptance. In

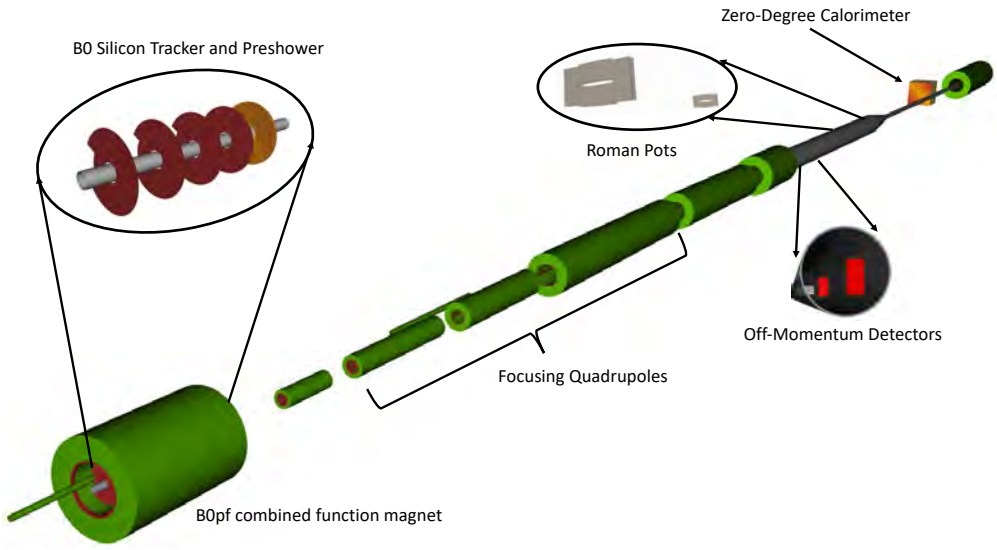


Figure 3: Layout of the EPIC far-forward detector systems, which include a tracking spectrometer and a silicon pre-shower embedded in an accelerator dipole magnet (the so-called "B0 detector"), silicon tracking detectors directly in the machine vacuum (Roman Pots and Off-Momentum Detectors), and a Zero-Degree Calorimeter with both hadronic and electromagnetic calorimetry capabilities.

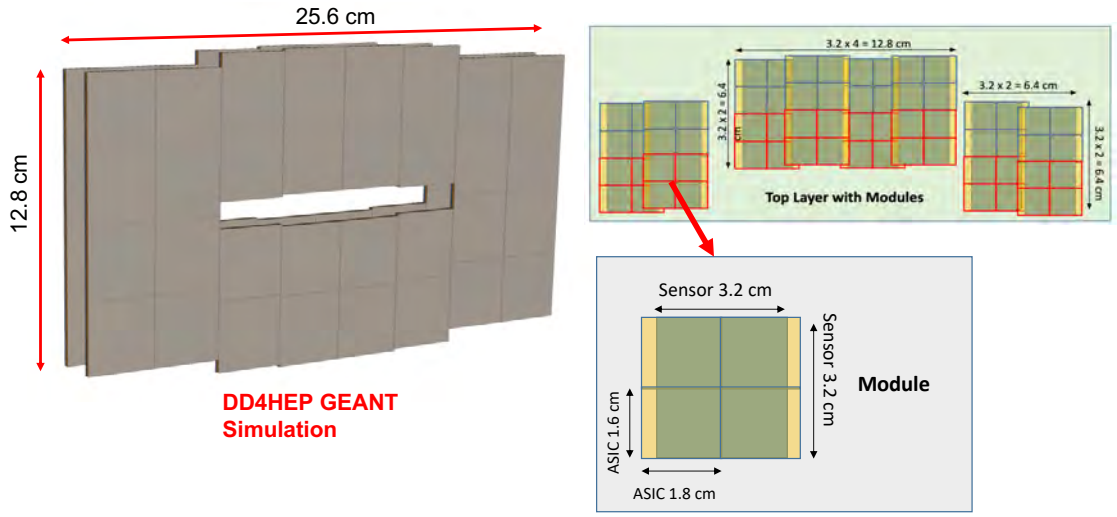


Figure 4: Layout Roman Pots far-forward detector subsystem. The current layout has been implemented in the GEANT4 simulations, and includes the sensor and ASIC package, as well as material estimates for the cooling and shielding layers of the detector.

order to tag and fully reconstruct these "far-forward" final states, a suite of detectors integrated with the hadron beam-line at interaction point (IP) 6 (the project IP) are required. The layout of this suite of far-forward detectors is shown in Fig. 3.

All four far-forward sub-systems require silicon detection components with spatial resolutions between 5 and 145 μm, and timing resolution ~30ps to achieve the required performance to reconstruct charged particle momenta at $\eta > 4.5$. In particular, the timing requirement is important for background rejection from both beam+machine component and beam+gas events, but also for disentangling the transverse momentum kick provided to the bunch particles by the EIC crab cavities. These devices account for the 25mrad crossing angle at IP6 by rotating the bunches via transverse momentum kicks, which vary longitudinally along the bunch, and cause an effective vertex smearing when performing reconstruction of the final-state particles. Given these requirements, AC-LGADs provide the unique

benefit of enabling accurate measurement of spatial and timing information, making them perfect for many applications in the far-forward region. Below, the subsystems for which use of AC-LGAD technology is planned are summarized.

In the case of the B0 Detector, AC-LGADs are planned to be used as a timing layer in the main tracking system, while also providing an additional spatial point for tracks, and perhaps also in the silicon pre-shower detector. The AC-LGAD sensor was also considered for the main technology for the entire subsystem, but it was determined that even with the incredible improvement in spatial resolution provided by signal-sharing in the sensor, the highly demanding specification ($\sim$5-10μm) for the B0 tracking was more-readily met with a different technology.

In the case of both the Roman Pots (RP) and the Off-Momentum Detectors (OMD), the spatial resolution requirements are less-stringent ($\sigma_{x,y} \sim 140\mu m$), enabling use of the AC-LGAD technology as a primary choice for implementation of the detector. This option allows for 4D information to be extracted from a single technology, which enables the Roman Pots and OMD subsystems to be efficiently realized in a very limited space inside the beam vacuum system. The current layout of the Roman Pots sensor and readout ASIC packages are shown in Fig. 4. The RP and OMD subsystems do not have stringent requirements on material budget since the particles being detected are all at energies $>$ 41 GeV (most above 100 GeV), and therefore not greatly affected by multiple scattering. However, in the timing layer of the B0 tracking system, we will need a material budget more-consistent with the forward tracking disks ($< 1\%$).

The size of the sub-systems are based on the spatial extent of the scattered beam particles which are produced from the various EIC beam energy/species configurations. The largest scattered proton envelope occurs for the 5x41 GeV beam energy configuration, and requires the 26cm x 13cm plane size for the Roman Pots detector systems. The Off-Momentum Detectors require smaller planes of 10cm x 20cm. In total, the combined active (sensor) area of the RP and OMD subsystems is $2152cm^2$. Since these detectors are operated close to the beam, and within vacuum, spatial care needs to be taken in cooling and shielding the detectors. Work is underway to better understand these requirements as both the ASIC and machine design matures, but current estimates place the expected detector occupancy at least two orders of magnitude lower than what is seen at the LHC for systems employing DC-LGAD technology for timing measurements.

For all applications in the far-forward area, a pixelated AC-LGAD with a minimum of 500 μm pixels is required, not just for accurate spatial reconstruction, but also for background rejection, and separation of multi-particle final states containing charged spectators with small angular separation (e.g. in the case He-3 breakup with the neutron as the active nucleon). Additionally, using pixelated detectors requires less overall layers in subsystems for the Roman Pots and OMD, which will be very important for engineering solutions required to minimize impedance on the hadron beams from the presence of these detectors in the beam vacuum.

2 FY22 Report

While working with the EPIC collaboration in defining the layouts and requirements of the AC-LGAD detectors, we have advanced the development of AC-LGAD sensors and frontend readout ASICs in order to meet such requirements, as planned in our FY22 proposal [4]. The highlights of AC-LGAD sensor development in FY22 include: 1) fabrication and testing of strip sensors with 500 μm pitch and 0.5-2.5 cm strip length with BNL Instrumentation Division (IO), 2) fabrication and initial testing of sensors with 20-50 μm active layer thickness with BNL IO. The development of frontend ASICs includes: 1) submission, receiving and initial testing of custom-designed EICROC0, 2) submission, receiving and initial testing of custom-designed FCFDv0, 3) investigation of alternative ASICs from third party institutions. Below we present these progresses.

2.1 AC-LGAD sensor

Prior to eRD112, small sizes $O(mm^2)$ of AC-LGAD sensors were fabricated by BNL, Hamamatsu Photonics (KPK) and Fondazione Bruno Kessle (FBK). Their timing and spatial resolutions from test beam studies were consistent with expectation from these sensors. For example [7], the timing and spatial resolutions of 2×2 pixel sensors from HPK with a active layer thickness of 50 μm and a pixel size of 500$\times$500 μm^2 were found to be around 30 ps and 25 μm, respectively, while those of 2×2 or

3×3 mm^2 strip sensors from BNL with a pitch size of 100-200 μm and length of 1.7-2.5 mm were around 30 ps and 5-10 μm. In order to meet the low material budget requirement for CTTL, we have designed, fabricated and tested long strip sensors with greatly reduced number of channels per unit area. Moreover, we are working on fabricating sensors with 20 or 30 μm thick active layer, which are expected to have smaller intrinsic timing resolution than the abovementioned sensors with 50 μm thick active layer. These results are described below.

2.1.1 Sensor fabrication by BNL IO

In fall/winter 2021, the first batch of AC-LGAD sensors for EIC applications was completed on 4", p-type epitaxial wafers in the class-100 clean room at BNL. The epitaxial layer consists of high-resistivity silicon 50-μm thick. The substrate is a low-resistivity, 300-μm thick wafer, serving as mechanical support, and its back is unpatterned. A picture of a wafer fabricated in this batch is shown in Fig. 5 (left). The wafer was populated with AC-LGAD strip sensors of large area, whose active area is about 0.5 cm $\times$ 0.5, 1.0, and 2.5 cm. Aluminum (about 0.7 μm thick) AC-coupled strips are patterned on top of $\sim$ 150 nm of PECVD silicon oxide, which has been deposited over an uniform low-dose (and therefore high resistivity) implant of phosphorus. At the border of the resistive n-layer, a Junction-Termination Edge (JTE) is created by a deep phosphorus implantation. Embedded into the JTE, which runs all around the device, a high dose phosphorus implant is contacted by a metal frame, grounded during biasing of the sensor. The gain layer, a deep low-dose boron implant, is uniformly ion-implanted below the n-resistive layer and 20 μm distant from the JTE. The termination region, including guard rings, is the same for every device. The wafers have been passivated with polymide while the full length of the metallized strip is exposed and available for wire-bonding. For each strip length, a few variations in the pitch and the width of the metal strips have been introduced:

- 0.5-cm long strips: pitch/gap 500/300 μm or a multi-pitch structure of pitch/gap 300/150, 200/100 and 100/50 μm into the same device;
- 1-cm long strips: pitch/gap 500/200 or 500/300 or 500/400 μm, and the same multi-pitch series as the 0.5-cm long strips;
- 2.5-cm long strips: pitch/gap 500/200 μm or and the same multi-pitch series as the 0.5-cm long strips.
- elongated pixels at a pitch of 2.6 mm in one direction and pitch/width as the above structures in the other dimension. However, these structures are outside of the scope of this report.

A few 0.5, 1 and 2.5 cm long strip sensors from this batch (see Tab. 2) have been tested in the beam. Test results can be found in section 2.1.3.

Name Unit	Pitch μm	Metal Width μm	Length mm	Thickness μm	Bias Voltage V
BNL 5–200	500	200	5	50	245
BNL 10–100	500	100	10	50	220
BNL 10–200	500	200	10	50	255
BNL 10–300	500	300	10	50	240
BNL 25–200	500	200	25	50	215

Table 2: Geometry of tested sensors with optimal operating voltage.

In summer 2022, we commenced with the fabrication of 4 new wafers at BNL. These wafers are 4" in size, p-type, with an active layer thickness of either 20 or 50 μm, based on the existing layout of AC-LGAD strips, see Fig 5 (left). We completed two wafers (one 20 and the other 50 μm thick), while the other two wafers (20 and 50 μm) are on hold, waiting inputs from the measurement results of the first two, as detailed below.

For these 4 wafers, we slightly modified the technology used in the previous fabrication of AC-LGAD wafers, leveraging from the knowledge acquired during fabrication of former AC-LGAD batches and their functional measurements. In particular, we changed (slightly) the implantation parameters of the uniform high-resistivity phosphorus layer (n-type implant) and, therefore, of the gain layer. For

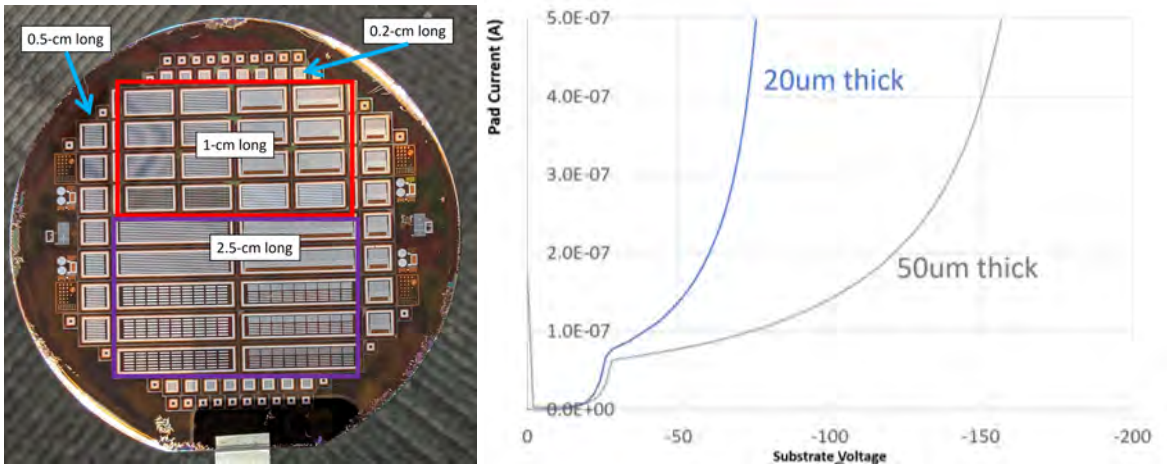


Figure 5: Left: Photograph of one of the 4" BNL wafers fabricated, populated with AC-LGAD strip sensors of different length in fall/winter 2021. 24 devices feature 1-cm long strips, 10 devices have 2.5-cm long strips and, at the sides, 14 devices with 0.5-cm long strips. AC-LGAD with 0.2-cm long strips are also on top and bottom of the wafer placed for test purposes. Right: I-V from two devices belonging to a 20 μm (blue) and 50μm (grey) thick wafers in 2022.

the latter, while the implantation energy is fixed at 380 keV – the maximum allowed by our vendor – the dose must be recalibrated to take into account the different doping profile of the n-type implant. For all the 4 wafers we used a n-type dose of $2e^{13}$ cm^{-2}, while a dose of $2.4e^{12}$ cm^{-2} for the gain layer has been used, notably, for both 20 and 50 μm thick substrates. The choice of the doses resulted by careful consideration of previously fabricated wafers and by TCAD simulations conducted in parallel. Preliminary current-voltage (I-V) characteristics of devices coming from the two finished wafers are shown in Fig. 5 (right), showing a breakdown voltage of 180 V for the 50 μm thick devices and of 80 V for the 20 μm devices. As the I-V graph shows, the gain layers depletes at about 25 V, therefore an electric field is generated in the substrate of about 3 V/μm, for both types of devices with different thicknesses. In the eRD112 discussions, it was proposed to attempt to obtain a larger electric field in the substrate to increase the gain, thus, for the two wafers that are still to be produced, we plan to implant the gain layer at a slighter lower dose, to bring the breakdown up in voltage. To tackle another problem that was find during laser tests in lab tests and test beams at FNAL, namely the non-uniformity in the gain over the wafer, observed in a previous BNL production, we worked with the ion-implantation vendor to increase the uniformity of the gain implant. A different implantation strategy has been applied for the first time to the two finished wafers, and it will be also applied to the two planned wafers of this batch. If the measurements show an increase in the gain uniformity, any other future LGAD wafer will be implanted in this way. The wafers in this batch used most of the masks of our previous batches, however the mask for the metal layer has been slightly changed to reflect the operational experience acquired in the tests conducted in the labs (laser tests) and at test beams. More specifically, in addition to strip devices, devices with zig-zag electrodes have been inserted. A summary of the geometrical characteristics and multiplicity per wafer of the devices in this batch is given in Tab. 3.

A third batch is also planned to be fabricated at BNL. This will be dedicated to small-area devices to test the EICROC0 chip. A design of the wafer layout is shown in Fig. 6. Half of the wafer consists of two layouts mating the 4x4 EICROC pixels (i.e. bump-bond compatible). The rest replicates large area devices of the previous batch for consistency in testing. As of now, all photolithographic masks have been ordered to the manufacturer (Photronics) except for the metal one (and therefore the passivation openings). The design of the metal layer will be discussed with the collaborators when the times comes to pattern it. More time is granted to implement the latest developments. Notice also that, due to the large number of EICROC0 compatible pixel sensors, a huge variety of electrode geometries is possible. This batch has already started with the p-spray implantation of a few 20, 30, and 50 μm thick epitaxial wafers. In this batch we also process 30 μm thick substrates to continue the study of different thicknesses.

multiplicity	strip length (mm)	pitch (μm)	gap (μm)
7	0.5	500	400
7	0.5	500	450
4	10	500	400
4	10	500	450
4	10	700	600
4	10	zig	zag
5	25	500	400 or 450
5	25	500	400

Table 3: List of AC-LGAD strip geometries in a wafer of the second batch.

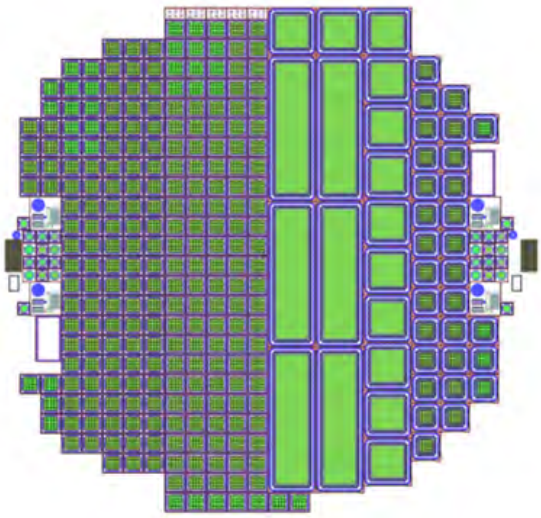


Figure 6: Wafer layout of the new batch that is dedicated to EICROC-compatible AC-LGAD sensors.

2.1.2 Sensor production by HPK

Prior to eRD112, there has been a US-Japan collaborative effort to advance the LGAD sensor technology focusing on high energy particle physics experiments. We have joined the effort to share knowledge and experience in AC-LGAD sensor development. Moreover, we have been working together with Univ. Tsukuba/KEK to prepare a AC-LGAD sensor production by HPK with shared cost and wafer area since June 2022. We expect to receive some strip and pixel AC-LGAD sensors with different pitch/length, electrode width, active layer thickness and n-restive layer dose by March 2023. We plan to test these sensors to understand the performance of sensors from HPK, which will be one of the candidate vendors for sensor production when the construction starts.

2.1.3 Sensor characterization with beam by UIC/FNAL

Characterization of AC-LGAD sensors was carried by the University of Illinois at Chicago (UIC) and Fermi National Accelerator Laboratory (FNAL) teams in the labs using infrared laser and beta sources, and at Fermilab Test Beam Facility (FTBF) using 120 GeV proton beam in order to validate sensor design and extract optimal parameters for EIC applications. Below we present the results with beam on AC-LGAD strip sensors from the first batch of BNL production listed in Tab. 2.

Data were collected at FTBF using the LGAD characterization setup developed by the Fermilab team as described in [6, 7]. This setup is based on a facility-provided silicon tracking telescope that measures the impact position of each proton, and a fast microchannel plate detector (MCP-PMT), which serves as a time reference with 10 ps resolution. The AC-LGAD and MCP-PMT waveforms were recorded using an eight channel Lecroy Waverunner 8208HD oscilloscope with a bandwidth of 2 GHz and a sampling rate of 10 GS/s per channel. The AC-LGAD sensors were mounted on the fast analog amplifier boards with 16 channels and 1 GHz of bandwidth designed at Fermilab [8] and

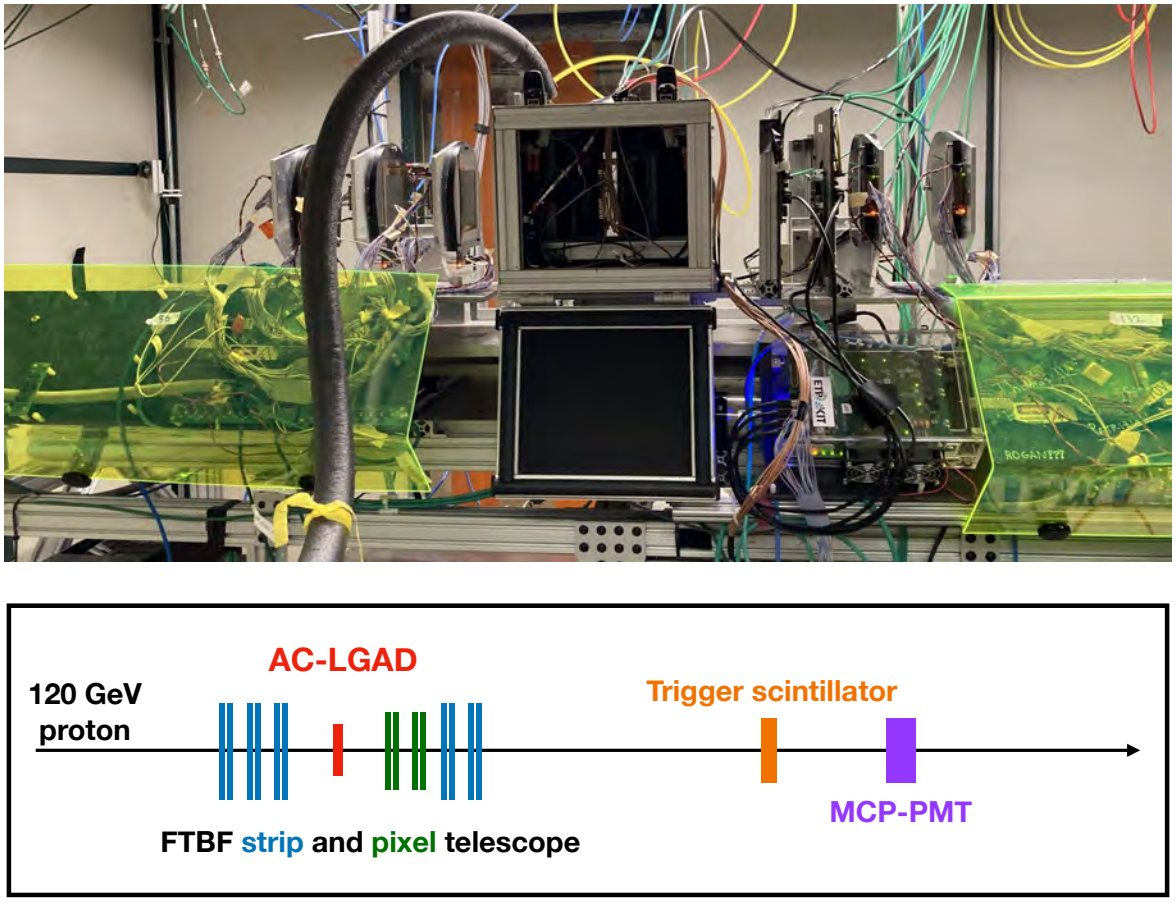


Figure 7: Picture (top) and diagram (bottom) of the FTBF silicon telescope and reference instruments used to characterize AC-LGAD performance. The telescope comprises five pairs of orthogonal strip layers and two pairs of pixel layers, for a total of up to 14 hits per track.

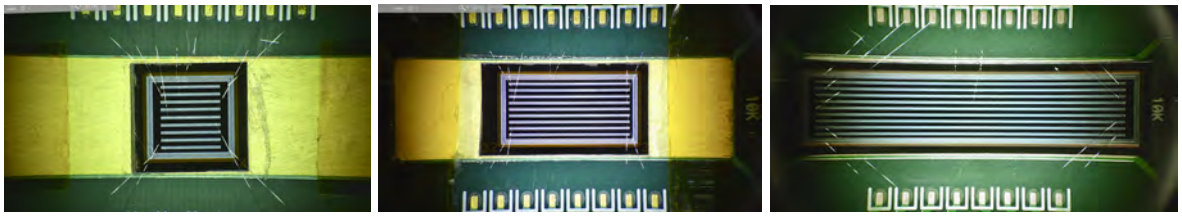


Figure 8: Three AC-LGAD strip sensors wire-bonded on Fermilab test board and tested at FTBF: BNL 5-200 (left), BNL 10-200 (middle) and BNL 25-200 (right). See text for details.

optimized for LGAD sensors, capable of accommodating 16 channels. The trigger signal is generated by a scintillator detector located downstream from the AC-LGADs and distributed to the tracker and the oscilloscope. Major improvements and upgrades to the experimental setup were made in FY22 to improve the position resolution of the reference telescope tracker down to ~ 5 μm, and upgrades to the DAQ system yielding increased operational robustness and enabling data-quality monitoring and event reconstruction in real time. Figure 7 shows a diagram of the setup along with an image of the environmental chamber that houses the AC-LGADs inside the telescope.

Multiple large-area sensors were systematically studied in our most recent campaign in March 2022, and some of the sensors are shown in Fig. 8. Signal wave-forms from up to seven channels of each LGAD are recorded by the oscilloscope. The waveforms are analyzed event-by-event to extract the amplitude, risetime, slew rate, and other relevant signal properties. The longest sensors exhibit larger duration pulses with a slower risetime for a given total charge or integral, which can result in

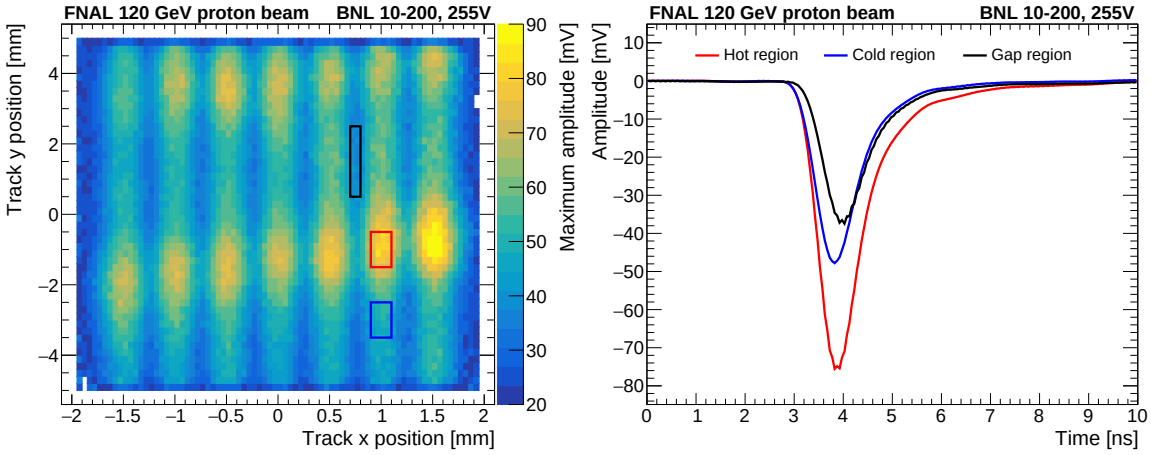


Figure 9: Amplitude map (left) of BNL 10-200 sensor. The different colored box represents hot, cold, and gap region. Averaged waveform (right) for the three different regions.

compromised timing performance.

A critical characteristics required to construct a large-area detector is the uniformity of the sensors properties across their surface. A detailed characterization of all these properties requires precise knowledge of the coordinates of the passage of the particles, and the FTBF telescope provides a unique facility to perform these studies, which were the focus of the March 2022 experiments. It was observed that sensors from this production show a significant non-uniformity in the signal amplitude across the sensor surface, with characteristic band patterns as shown in Fig. 9. These patterns are believed to arise due to a non-uniformity in the gain implant, and will be corrected in the next round of BNL sensor production (see section 2.1.1). The ratio of amplitudes between high and low gain regions reaches roughly a factor of two when the sensors are operated at high voltage near breakdown. Since the highest gain regions enter breakdown at lower voltages, they determine the maximum attainable bias voltage for each sensor. As result, the lower gain regions remain somewhat under-biased, and in some cases, these regions represent the majority of the surface, since the high gain structures can be highly localized. Many important performance metrics are strongly dependent on gain, and therefore can vary significantly across the surface.

Since uniform large-area LGADs are produced routinely by large commercial vendors (e.g. HPK/FBK for the CMS and ATLAS timing detectors), it is expected that future large-area AC-LGADs productions by BNL or other foundries will also demonstrate good uniformity. To isolate the effects of the design and geometry choices from the effects of the non-uniformity in this BNL production, we define regions within each sensor to characterize the high and low gain regions separately. Since the response also varies between direct strip hits and hits to gaps between strips, we also define regions to separately quantify the gap performance. Examples of these regions of interest are overlaid in Fig. 9, as well as the corresponding average pulse shapes in each region. We take the performance in the high gain regions as indicative of what would be attained in a uniform sensor, where all regions would reach high gain at similar bias voltage.

In Tab. 4, we summarize the beam test results for AC-LGAD strip sensors from the first BNL production after correcting for a time delay contribution to the time resolution due to finite length of strips. As one can see, the timing resolution degrades as the strip length increases due to slower rise time and lower signal amplitude. Nevertheless, the 10 mm length strip sensors achieve a timing resolution between 32-36 ps in the "hot region", which is comparable to previous BNL strip sensor production with much shorter length (1.7-2.5 mm). The 10 mm strip sensor with 500 μm pitch and 100 μm metal electrode width achieve 21 μm spatial resolution by taking the weighted average of single-strip and two-strip clusters. These results show that AC-LGAD strip sensors with $O(cm)$ strip length represent a good candidate for EPIC AC-LGAD detectors providing both excellent spatial and timing resolutions with relatively low number of channels.

Name	Time resolution		Exactly one strip		Two strip	
	Overall	Hot region	Resolution	Fraction	Resolution	Fraction
Unit	ps	ps	μm	-	μm	-
BNL 5–200	35 ± 1	30 ± 1	52 ± 1	35%	12 ± 1	65%
BNL 10–100	42 ± 1	35 ± 1	28 ± 1	23%	19 ± 1	77%
BNL 10–200	42 ± 1	32 ± 1	55 ± 1	43%	18 ± 1	57%
BNL 10–300	40 ± 1	36 ± 1	78 ± 1	51%	16 ± 1	49%
BNL 25–200	72 ± 1	51 ± 1	71 ± 1	82%	31 ± 1	18%

Table 4: Test beam results of AC-LGAD strip sensors from the first batch of BNL production.

2.1.4 Sensor studies at SCIPP

In the area of sensor development, in FY22 the Santa Cruz Institute for Particle Physics (SCIPP) at UC Santa Cruz (UCSC) contributed studies geared towards the understanding of charge sharing and position resolution for AC LGADs, and on the effects of strip length on these characteristics. The group made use of several techniques to provide feedback to labs developing and fabricating AC LGADs, including lab-bench measurements of electronic characteristics (CV, IV) and sensor response (making use of a highly-focused, fast pulsed laser system) and test-beam data from the FNAL test beam facility. The SCIPP group also organized a neutron irradiation campaign of AC-LGADs at the TRIGA reactor in Ljubljana (IV of a pre-rad and post-rad AC-LGAD shown in Fig. 10 (left)). Finally, the group also developed 2D and 3D sensor simulations in two proprietary TCAD frameworks (SILVACO and Sentaurus) that are showing promise to be able to guide further optimization of sensor parameters for EIC applications.

The SCIPP group performed measurements on AC-LGAD strip and pixel sensors produced at BNL, HPK and FBK. The electrical characterization was performed on a probe station using a power supply and LCR meter. The measurements were done on AC-LGADs with the following configurations:

- IV (current over voltage): done by connecting the HV to the back of the sensor and the power supply ground to the N+ ring DC connection. This measurement is to check the current level and the breakdown voltage of the sensor. An example IV for BNL sensors before and after neutron irradiation is shown in Fig. 10 (left).

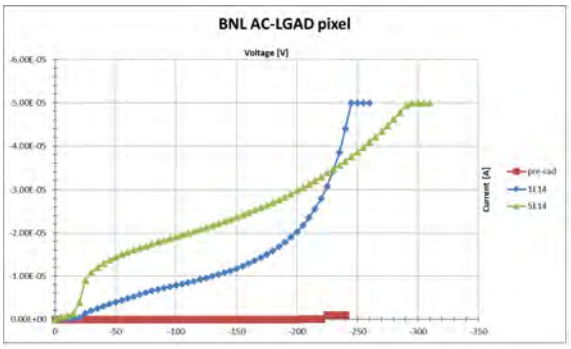
- DC capacitance over voltage (CV): capacitance of the entire sensor, done by connecting the low LCR meter connection with HV to the back of the sensor and the LCR meter probe to the N+ ring DC connection.

- AC CV: capacitance of one of the AC pixels or strips, done by connecting the low LCR meter connection with HV to the back of the sensor and the LCR meter probe to one of the AC connection. The N+ connection in this configuration is connected to ground. The AC capacitance is the most important parameter since it corresponds to the input capacitance to the readout ASIC. An example AC capacitance for three different electrode sizes is shown in Fig. 10 (right).

- Inter pixel/strip capacitance: capacitance in between two metal pixels or strips, done by connecting the HV to the back of the sensor, the LCR meter high and low with probes to two of the AC connection. The N+ connection in this configuration is connected to ground.

For all of these measurements the measured capacitance is registered after the full depletion of the devices. The measurements were done with several frequencies on the LCR meter to ensure measurement stability as seen in Fig. 10 (right). Multiple sensors from BNL, HPK and FBK were characterized in this manner.

For the laser Transient Current Techinique (TCT) testing sensors are mounted on Fermilab testing boards [8] and read out by a fast oscilloscope (2 GHz, 20 Gs). The goal of the measurement is to emulate the signals from charged particles but in a more convenient laboratory setting with a faster turnaround. The downside is that the laser cannot penetrate the metal electrodes, therefore the sensors can only be studied in between the metal. Sensors mounted on boards are excited with an infrared (IR) 1064 nm pulsed laser with a pulse temporal width of 400 ps. The laser beam is focused by a lens system that can produce a laser spot of 10-20 μm on the surface of the sensor. The analog board is



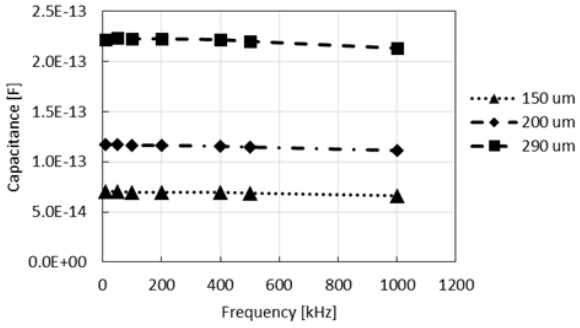
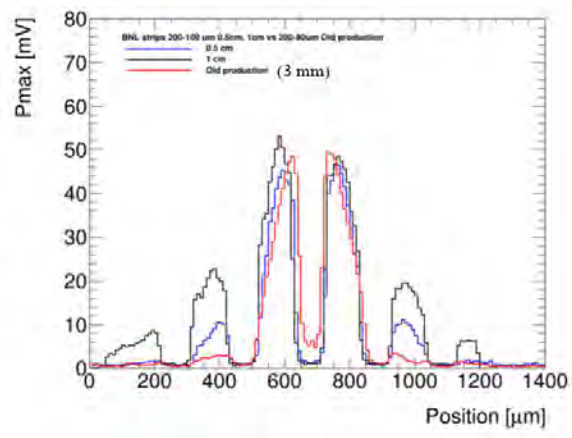


Figure 10: Left: IV of a BNL AC-LGAD before and after neutron irradiation. Fluences are quoted in 1 MeV neutron equivalent. Right: AC capacitance of a 2×2 pixel sensor from FBK with pitch of 300 μm and different metal electrode sizes.



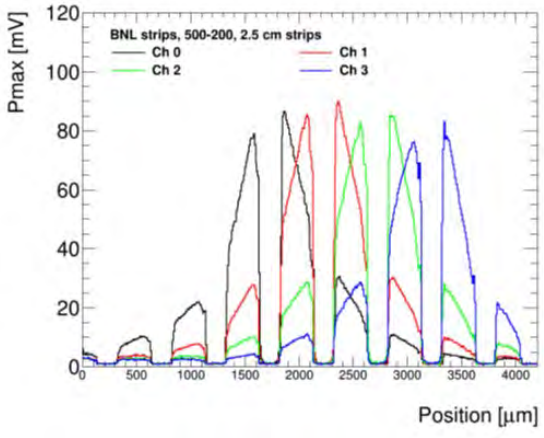


Figure 11: Left: Single strip laser TCT scan of 200 μm pitch BNL strip AC-LGADs with three different lengths of 3 mm, 5 mm and 10 mm. Right: Laser TCT scan of four strips of a 500 μm pitch BNL AC-LGAD strip sensor with length of 25 mm. In both plots the signal under the metal strip is zero because the laser cannot penetrate the metal, the signal is only visible in between strips.

mounted on X-Y moving stages so the response of the sensor as a function of laser illumination position can be evaluated. X-Y 1D/2D scans of the sensors are taken with the system: for each position in the position grid an average waveform is registered for each readout channel. The characteristic charge sharing proprieties of AC-LGADs was probed for strips of different width, pitch and length. As an example the effect of the strip length is shown in Fig. 11.

Pixel sensors were also tested with the laser TCT system, a 2D scan around a 100×100 μm^2 electrode in a FBK AC-LGAD sensor with 500 μm pitch is shown in Fig. 12 (left). The estimated position resolution in the Y direction is shown in Fig. 12 (right), in this case the position resolution is between 5-10 μm in the inter-pixel region. To evaluate the distribution a very precise average scan between the four pixels and the relative fractions for the four pixels is computed for each point. Then several events are taken and the position is reconstructed by comparing the fractions with the reference scan and the resolution is calculated with a Gaussian fit to the reconstruction-true position distribution.

The key points for the reported studies is that AC-LGAD can provide very good position (down to pitch/10-100) and time resolution. The position reconstruction can be done using the charge sharing proprieties of AC-LGADs. Furthermore the combination of time of arrival can be used to improve time resolution. However many parameters, geometry and doping, have to be optimized to achieve the perfect performance, A range of strip geometries show good results, however sensors with very small pitch (50 microns or less) or long strips (2.5 cm) have shown too much charge sharing and degraded performance (large charge sharing means smaller amplitude per electrode and less Signal/Noise ratio).

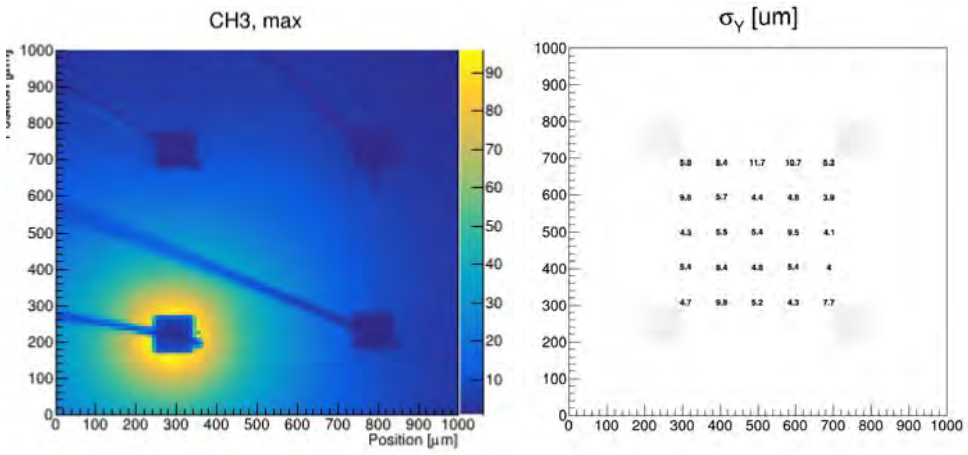


Figure 12: Left: 2D laser TCT scan of one pixel of a FBK pixel sensor with pitch of 500 μm and pixel size of 100 μm. Right: reconstructed position resolution in Y in between the four pixels (grey squares).

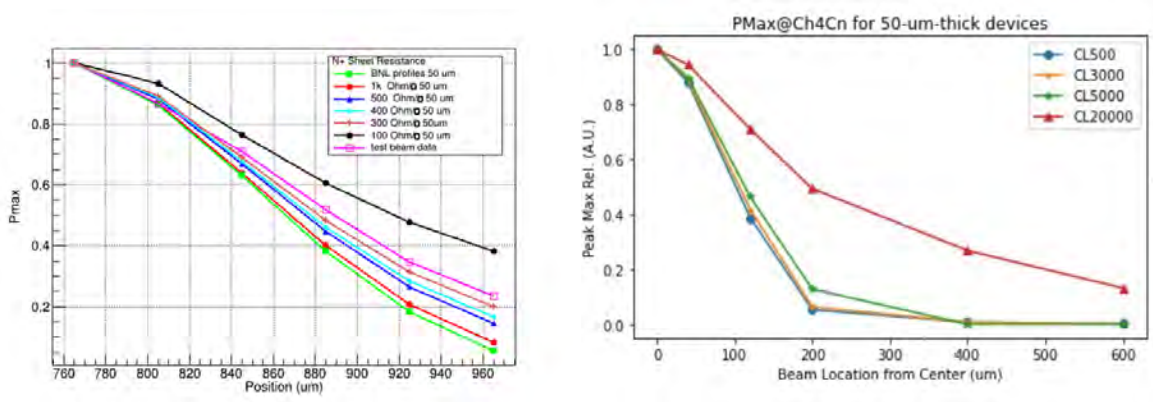


Figure 13: Left: 2D Silvaco simulation for a 200 μm pitch strip AC-LGAD showing the effect of the N+ resistivity. Right: 3D Sentaurus simulation of a 200 μm pitch strip AC-LGAD showing the effect of the strip length.

Small pixels with large pitch show good reconstruction properties and low input capacitance. The pixel geometry (pitch, electrode size, shape) can be optimized.

TCAD Silvaco and Sentaurus simulation have been run to study the effects of AC-LGADs parameters to the charge sharing profile. Studies shown with Silvaco are done with a 2D approximation, while studies in Sentaurus are for a full 3D simulation. In Fig. 13 (left) the effect of the N+ resistivity on charge sharing is shown for a 200 μm pitch strip sensor. In this plot the Pmax of the studied strip when the charge injection is under the strip (position 760 μm) is normalized to one and the relative response is shown as the injection is moving away from the strip. In the same plot the charge sharing profile taken from the test beam data mentioned in the previous paragraph is shown in pink. In Fig. 13 (right) the 3D Sentaurus simulation of a strip AC-LGAD with pitch 200 μm and different lengths is shown. The Pmax of the studied strip when the charge injection is under the strip is at position 0 μm and the response is shown as the injection is moving away from the strip. The effect of the strip length on the charge sharing profile can be clearly seen. Note that this effect is not observed in the standard 2D Sentaurus simulation, a full 3D simulation is necessary. The conclusion is that TCAD simulations are invaluable to provide guidance for detector parameters in future prototype runs: pitch, metal width, strip length, sensor thickness.

2.1.5 Sensor studies at LANL

The Los Alamos National Laboratory (LANL) team has carried out a series of LGAD and AC-LGAD prototype sensor characterizations. With the LANL LDRD support, a ^{90}Sr source test bench has been setup at LANL, which includes the low and high power supply modules, a 2.5 GHZ Keysight oscilloscope, CAEN 1730s digitizers and a DAQ computer. Figure 14 presents the ^{90}Sr source test bench setup at LANL. Four different types of LGAD prototype sensors have been characterized at LANL: HBK-1.2, HBK-2, HBK-3.1 and HBK1.1. The bias voltage dependent amplitude for these LGAD sensors have been studied with this ^{90}Sr test bench. The bias voltage dependent digitized amplitudes for these four LGAD prototype sensors are shown in Figs. 15-16. The results are consistent with the laser tests on the raw prototype sensors carried out at SCIPP. These tests will be continued for new AC-LGAD prototype sensors.

Irradiation tests have been performed at LANL LANSCE with 500 MeV proton beams. In total 8 groups have been setup to validate the LGAD and AC-LGAD prototype sensor radiation hardness. The radiation doses vary from 10^{13} $n_{eq}cm^{-2}$ to 10^{16} $n_{eq}cm^{-2}$. The associated work activities include the following items:

- LANSCE beam user proposal preparation and submission.
- LANSCE beam test setup.
- Sensor characterization before the irradiation tests.

We plan to work on the sensor characterization after the irradiation tests and arrange storage and shipping of these test samples.

2.2 Frontend Readout ASICs

The current design of far-forward AC-LGAD detectors feature pixelated sensors, while the CTTL detector uses strip sensors to have reduced number of channels and power consumption. These require different frontend readout ASICs optimized for pixel sensors and for strip sensors. Therefore, we have pursued more than one frontend ASIC development effort, including 1) EICROC0 design and submission 2) FCFDv0 design, submission and initial testing, and 3) investigation into ASICs developed by third party institutions.

2.2.1 EICROC0 design and submission

While specific ASICs have been designed to readout DC-LGADs of ATLAS HGTD and CMS ETL, namely ALTIROC [9, 10] and ETROC [5], the development of a dedicated ASIC optimized to readout

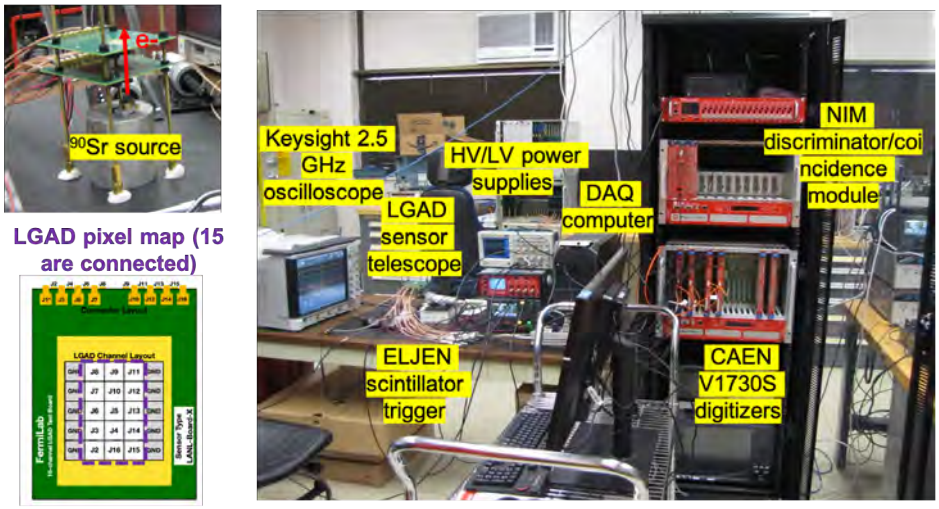


Figure 14: The LGAD and AC-LGAD prototype sensor bench test configuration at LANL. A $90^{S}r$ source has been used for the sensor characterization.

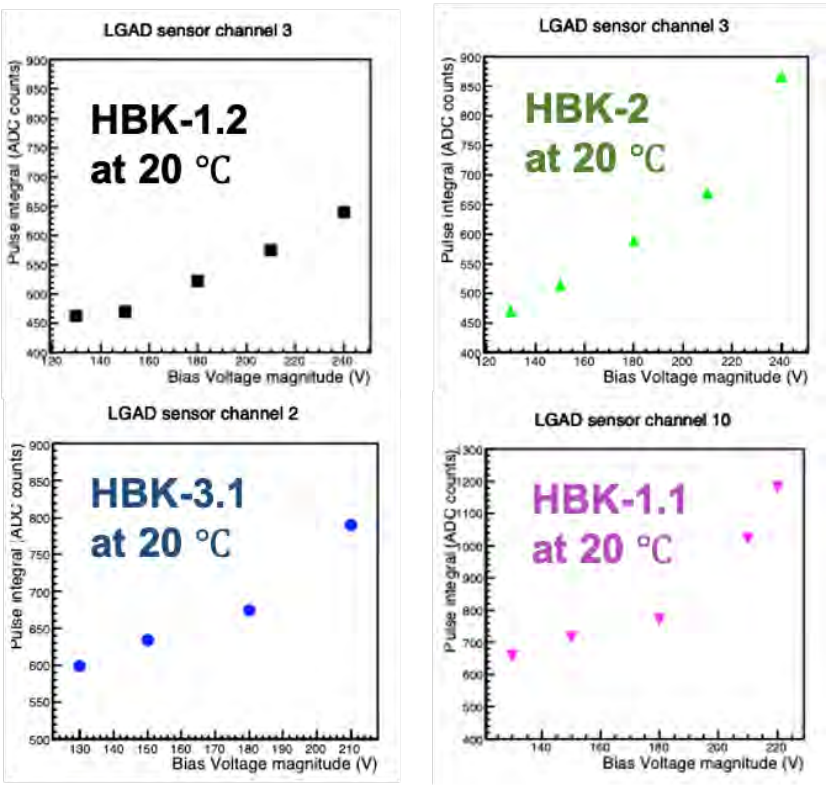


Figure 15: The bias voltage dependent amplitude of LGAD

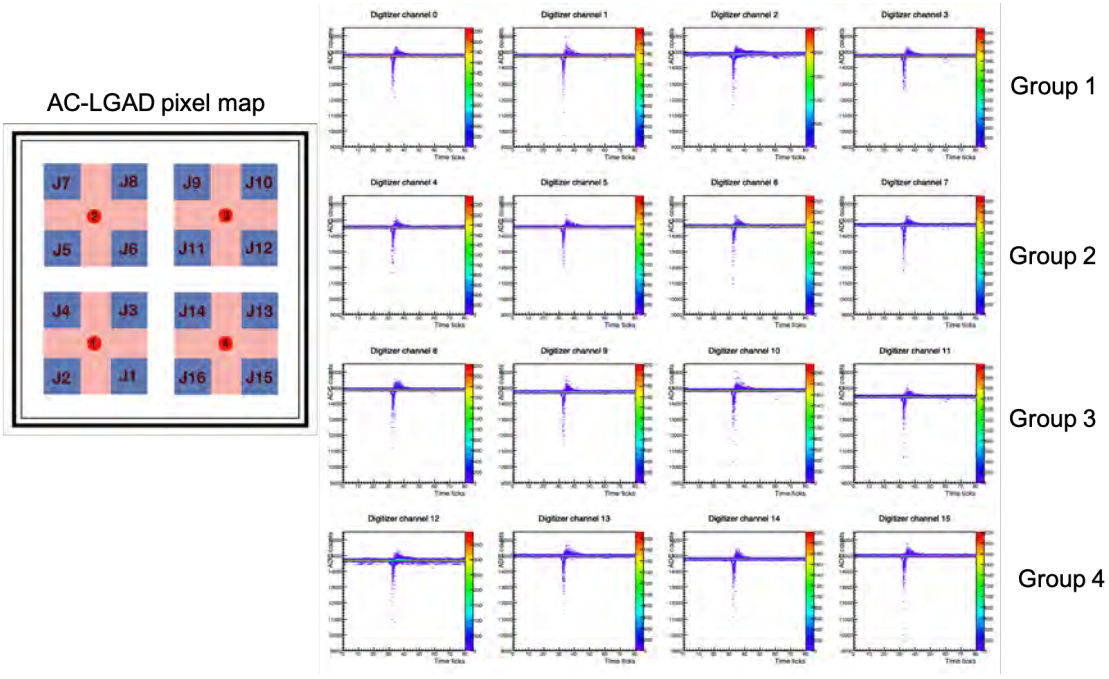


Figure 16: Digitized signals of all 16 pixels from a AC-LGAD sensor with the ^{90}Sr tests at LANL.

novel fine pixelated AC-LGAD sensors is mandatory to fully exploit their potential in terms of time and spatial resolutions, taking into account their intrinsic properties (lower capacitance) and the signal sharing (sensitivity to small charges). The goal of the EICROC team is to develop an ASIC with a pitch size of 0.5 $\times$ 0.5 mm^2 to readout AC-LGAD sensors and to characterize the integrated sensor+ASIC

detector system in an environment close to the experimental conditions.

The needs for fast timing performance and finer granularity pose significant challenges to the readout electronics and specifically to the ASIC readout chips. Present ASIC chips designed for ATLAS and CMS timing detectors have a jitter on the order of 20–30 ps, and a pixel granularity of 1.3 × 1.3 mm^2. Reduced granularity and better timing resolution requirement will make it more challenging to fit all the circuit components within the available space, and also likely lead to significantly increased power consumption due to increased total number of channels.

The EICROC project relies on complementary teams with expertise in micro-electronics, instrumentation and semi-conductor detector characterization from French institutes (IJCLab, CEA-Saclay/Irfu/DEDIP and OMEGA) and from Brookhaven National Laboratory (BNL) also involved in the design and the production of AC-LGAD sensors for EIC. In 2022, in close collaboration within the consortium (periodic meetings), the electronics activity was many folds:

- Measurements and data analysis by the BNL team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC0** chip using a Beta source (^{90}Sr) and exploiting an infrared laser test bench,
- Measurements and data analysis by the IJCLab team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC1_v2** chip using a Beta source (^{90}Sr). Based on the BNL IR laser test bench, all equipment have been ordered to set-up an IR laser test bench at IJCLab,
- Relying on simulations developed at IJCLab and OMEGA, an ASIC prototype has been designed involving the CEA-Saclay/Irfu team for the TDC and collaborators from AGH University of Science and Technology (Krakow, Poland) for the 8-bit ADC (Analogical to Digital Converter). The chip design has been submitted for fabrication at the end of March 2022 and EICROC0 chips have been received at the end of July 2022.
- The dedicated printed circuit board (PCB) which holds the EICROC0 and the AC-LGAD sensor has been designed by the OMEGA team, fabricated and 10 pieces were received at the end of July 2022. The PCBs have been cabled at IJCLab. PCBs and EICROC0 chips have been shipped to BNL for the wire-bonding.
- A ZC706 Xilinx board acting as the interface board to control EICROC0 parameters has been provided and the associated firmware has been developed by IJCLab team.

All the FY22 costs have been covered by funds granted by the LabEx P2IO [12] (Université Paris-Saclay, France) for the period 2020-2022 within the call "Projets Emergents" (AC-LGAD Project), French institutions has thus provided in-kind labor and material contributions during 2022. Below we present these works.

Studies based on (HGTD) ALTIROC1_v2 chip (IJCLab):

ALTIROC1_v2 is a 5 × 5 pixelated ASIC designed by OMEGA in 130 nm node technology for ATLAS HGTD [11]. It holds 2 kinds of Pre-Amplifiers, 15 Voltage Pre-Amplifiers (VPA) and 10 Trans-Impedance Pre-Amplifiers (TZ). Each channel uses two Time Digital Converters (TDCs), one measuring the Time-Of-Arrival and the other the Time-Over-Threshold (TOT) as an estimate of the signal amplitude to correct for time-walk effect. This ASIC which was designed to read out HGTD DC-LGAD sensors with 1.3×1.3 mm^2 pixels is used as a stepping stone to read out AC-LGAD sensors and to constrain the design of a proper ASIC prototype.

After each individual ALTIROC1_v2 channel on the printed circuit board #19 (B19) has been characterized using HGTD test bench at IJCLab to identify best working channels (TOA and TOT), the circuit has been shipped to BNL where 8 channels of a 3 × 3 pixelated AC-LGAD sensor have been wire-bonded to the ASIC and sent back to IJCLab in July 2021 where a characterization of each connected channel of the system ALTIROC1_v2 + AC-LGAD sensor has been performed.

Figure 17 shows on the left the observed pre-amplifier signal amplitudes from each AC-LGAD connected channels corresponding to an input charge of ∼8 fC when the sensor is biased at -160 V. The other plots concern channel 1, as an illustration, and have been obtained after scanning the threshold, the delay (TOA), the charge (TOA and TOT). From the delay scan (TOA), the corrected Least Significant Bit (LSB) is found to be of the order of 30 ps for each connected TDC channel showing a uniformity among all channels (see Fig. 18). For TOT, while scanning the injected charge,

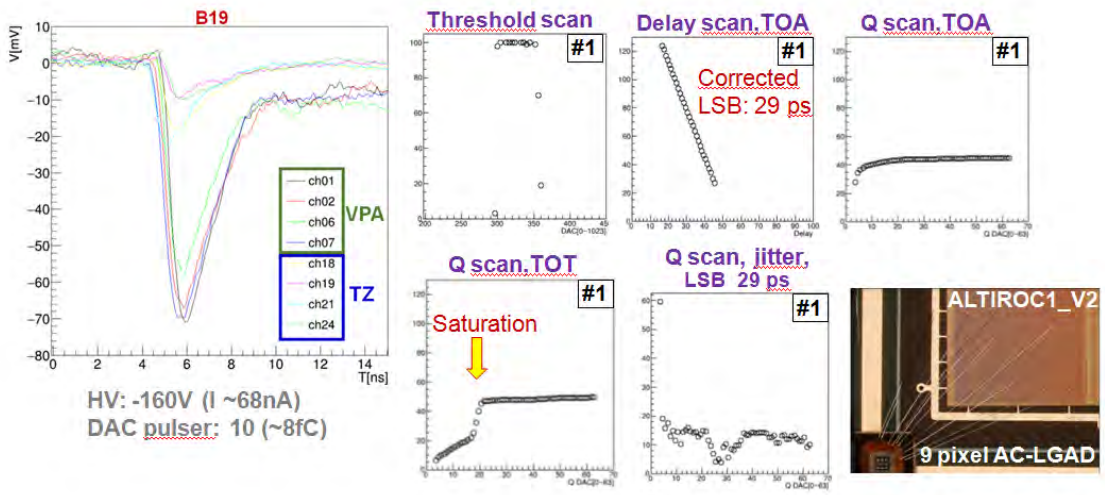


Figure 17: Left: observed ALTIROC1_v2 pre-amplifier signal amplitudes corresponding to a $\sim$ 8 fC input charge for each channel connected to a pixelated 3×3 AC-LGAD sensor biased at -160 V. Right: results from threshold scan, delay scan, and injected charge scan (TOA and TOT). The picture on the bottom right shows a 3×3 AC-LGAD sensor wire-bonded to an ALTIROC1_v2 chip.

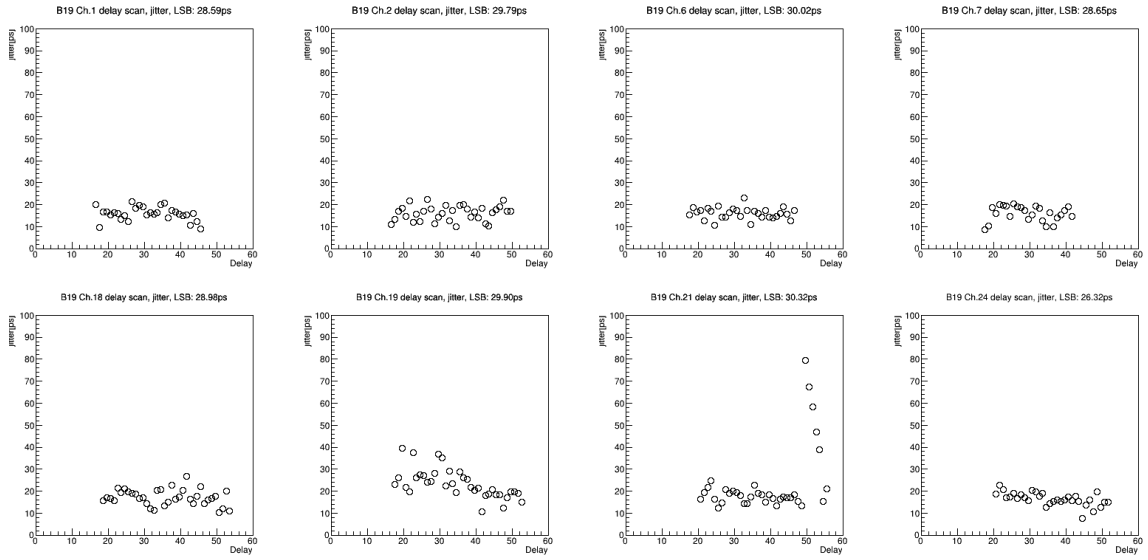


Figure 18: Measured jitter as a function of the delay in arbitrary units for each channel connected to the AC-LGAD sensor.

an effect looking like a saturation is observed for most channels above an injected charge of 21 fC. After investigation, this "saturation" effect, already mentioned in [10] is due to afterpulses observed on the discriminator falling edge signal.

The threshold of each channel has been measured and the lowest detectable charge being about 2.5 fC makes us confident that the goal of 2 fC for EICROC can be achieved. The average jitter for each channel is of the order of 20 ps for an injected charge higher than 5 fC, which is in agreement with measurements and simulations performed earlier by ATLAS HGTD team, see Fig. 19 and [11].

The charge sharing between pads/pixels has been studied exploiting ALTIROC (self) charge injection, using a beta source (^{90}Sr) and through simulations.

Using the ATLAS HGTD electronic test-bench, a study has consisted in injecting a 8 fC charge in one ALTIROC1_v2 channel and measuring pre-amplifier output signal amplitude in the neighboring pads placing the whole system in a black box. The resulting sharing was found to be of the order of

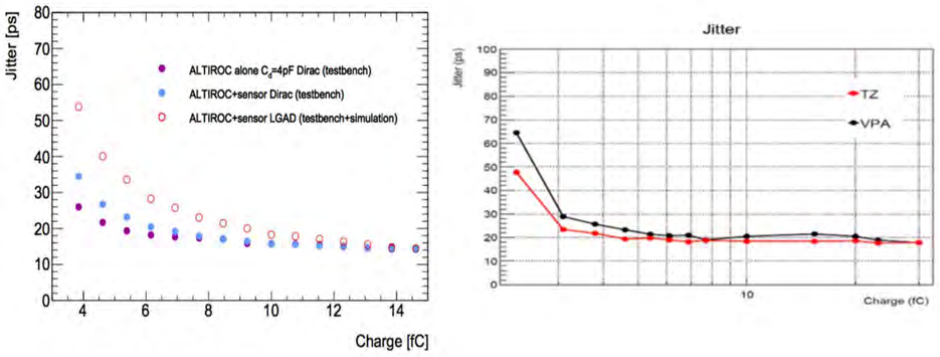


Figure 19: Left: ALTIROC1 measured and simulation-extrapolated total hit jitter for increasing input charges [11]. Right: jitter measured from VPA and TZ pre-amplifier AC-LGAD wire-bonded channels (HV -190 V) as a function of the injected charge.

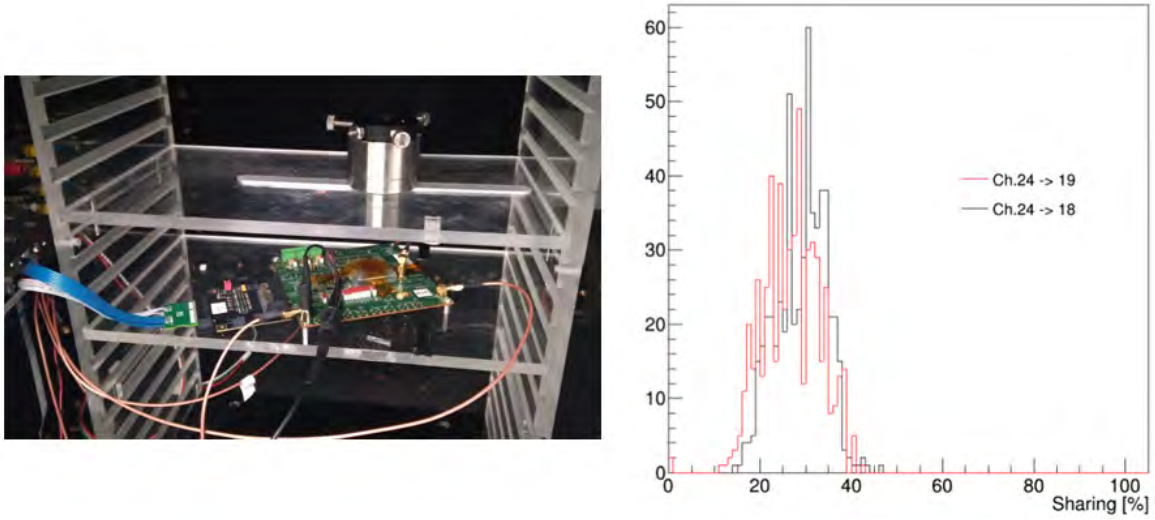


Figure 20: Left: experimental Beta source set-up. Right: amplitude distributions of channels #18 and #19 versus the charge sharing selecting #24 as the highest measured amplitude.

15% of the injected channel for 2 clusters: one involving VPA channels and one involving TZ channels.

A beta source (^{90}Sr, 37 MBq) has been used to acquire data with the system (ALTIROC1_v2 + 3 × 3 AC-LGAD sensor 8 channels wire-bonded) placed in a black box to screen from light. The experimental set-up is presented on Fig. 20 (left). Considering TZ connected neighboring channels (#18, #19 and #24), AC-LGAD biased at -170 V, the charge sharing was found to be of the order 30% for neighboring channels (#18 and #19) with respect to #24 selected as the highest measured amplitude (see Fig. 20 (right)). This result includes the TOT issue due to afterpulses observed at the falling edge of discriminators signals.

To study the charge sharing among pads, an electronics simulation modeling the charge injection has been developed considering a matrix of 12 pads and TZ pre-amplifiers, as illustrated on Fig. 21 (left). The study consisted of comparing pre-amplifier signal amplitudes obtained at each pad after injecting a 19 fC charge at a distance ratio between pads between 0 and 1 (a ratio of 0.5 meaning that the charge is injected at equal distance between 2 pads, pads #6 and # 7). As an example, the pre-amplifier signal amplitudes corresponding to a distance ratio of 0.25 and considering a LGAD sheet resistance of 1kΩ are presented on Fig. 21 (right). In the simulation different values of LGAD resistance sheet have been taken into account: 0.1, 1, 2.5, 5 and 10 kΩ. The optimization of the

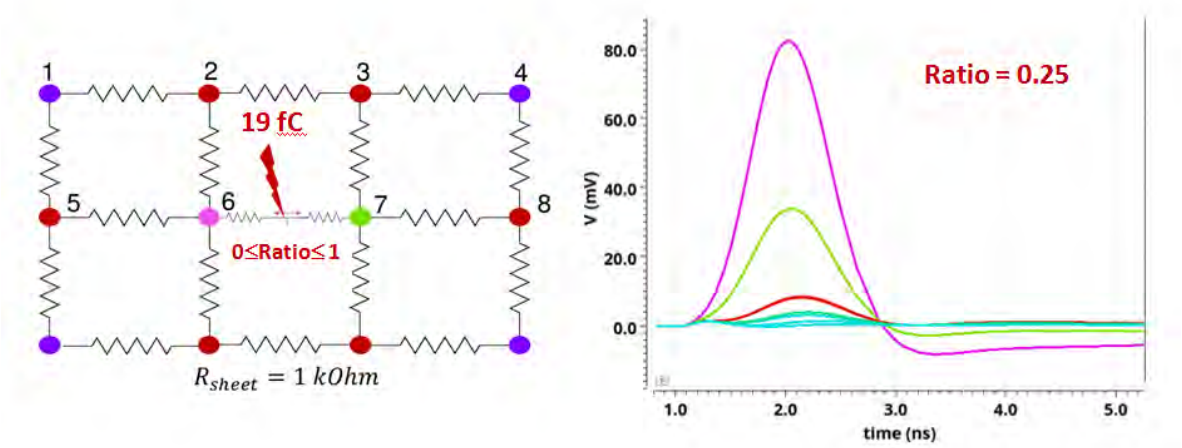


Figure 21: Left: schematic model of 12 pads on which rely the electronics simulation that has been developed to study charge sharing among pads. Right: pre-amplifier signal amplitudes corresponding to each pad according to the pad matrix model for a distance ratio of 0.25 and considering a LGAD sheet resistance (R_{sheet} of 1 kΩ.

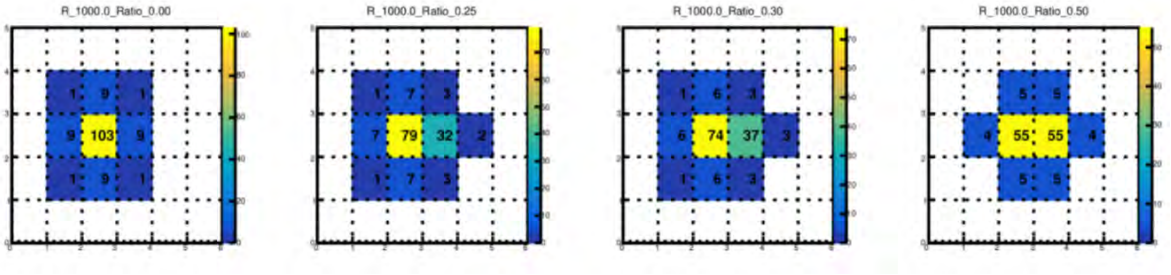


Figure 22: A 2D-representation of pre-amplifier signal amplitudes in mV obtained in each neighboring pad for a distance ratio of 0, 0.25, 0.30 and 0.50 (from left to right) considering a LGAD resistance sheet of 1 kΩ.

sheet resistance layer is a trade-off between the best time resolution in the central pixel (requiring the largest amplitude, thus a large sheet resistance value) and the position measurement (requiring enough amplitude sharing in the neighbours, thus a small sheet resistance value). A few kΩ will satisfy both requirements.

The results of this electronics simulation have been exploited as inputs of another simulation which provides a 2D representation of the results obtained by the electronics simulation which is shown in Fig. 22 for distance ratios of 0, 0.25, 0.30 and 0.50 and a 1 kΩ AC-LGAD sheet resistance. In the context of the design of a specific ASIC prototype to readout AC-LGAD, due to the need of a threshold for precise position determination and the strongly nonlinear behaviour of the TOT, the goal of this simulation was to determine the position resolution which could be achieved relying on the barycenter method as a function of the dynamic range of the ADC to be used to measure the amplitude. This second simulation including the Landau(1,0.3)-distributed (smearing) deposition and a 1 mV gaussian noise has shown that a 8-bit ADC was sufficient to achieved a position resolution < 50 μm. On Fig. 23, one can see that 8 and 10-bit ADC are leading to an equivalent position resolution of the order of 4% (RMS) of the pixel size which corresponds to 20 μm when considering a 500 μm pixel size.

These studies have been presented at the 2022 EIC User Group Early Carreer [13] and allowed us to develop analysis tools which will be exploited in the next step consisting of the characterization of the system (EIROC0 + AC-LGAD sensor).

EICROC0 Design

Based on the expertise in mircro-electronics of OMEGA (responsible for the design of HGCROC

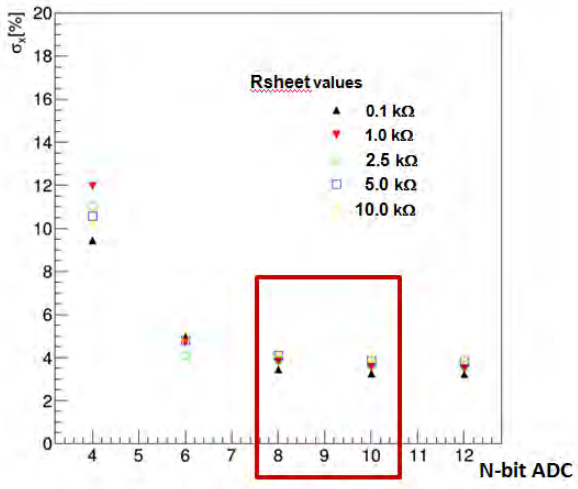


Figure 23: Position resolution in % of the pixel size as a function of the ADC dynamic range for several AC-LGAD sheet resistance.

[14, 15] readout chip for the CMS High Granularity Calorimeter and the ATLAS ALTIROC ASIC) and from CEA/Irfu/DEPIP (responsible for the design of the TDC of HGCROC), the goal is to design a novel ASIC in 130 nm CMOS technology, EICROC, with a pitch size of 0.5 × 0.5 mm^2 that meets the requirements set by EIC providing a precise time measurement with a TDC combined with an Analog Digital Converter (ADC) for the amplitude measurement based on the simulations undertaken at OMEGA and IJClab.

For the EICROC ASIC associated to the EIC Roman Pots detector, due its location (in vacuum) and its proximity to the beam (limited space), one challenge is to reduce the power per channel to a fraction of mW, while ensuring GHz bandwidth, ultra-low noise (< 1mV) for the front–end, picosecond accuracy in the TDCs and good signal-to-noise ratio at the ADC level. Most common architectures dissipate only when the TDC is converting but the large currents drawn during conversion limit drastically the number of TDCs that can be placed on a chip and the voltage drop for large ASIC. In addition, fitting the current electronic blocks, such as the HGCROC-like TDC, in a smaller pixel area represents a second challenge while maintaining their performance. Therefore, the development of a pixel-like ASIC with a few picoseconds timing accuracy represents a technological challenge and requires several iterations that have to be characterized. Table 5 summarizes the specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities as well as the EICROC0, the first EICROC iteration, that has been designed and delivered in July 2022.

	HGCROC	ALTIROC/ETROC	EICROC0
Sensor type	Si	LGAD	AC-LGAD
Pixel size [mm^2]	5 × 5	1.3 × 1.3	0.5 × 0.5
Pixel thickness [μm]	100-300	50	50
Pixel capacitance [pF]	50	4	0.5
MIP equivalent charge [fC]	4	5-20	10
Power per channel [mW]	20	5	1
TDC Least Significant Bit (LSB) [ps]	20	20	12
Threshold [fC]	12	4	2
Band width [MHz]	200	800	800
TDC (Time-Over-Threshold)		8 bits/10 bits	
ADC	10 bits@40 MHz		8 bits@40 MHz

Table 5: Comparison of specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities. ALTIROC and ETROC are similar but in different technologies: 130 nm CMOS for ALTIROC and 65 nm CMOS for ETROC.

EICROC0 is a 4×4 pixelated prototype ASIC with a pitch size of 0.5×0.5 mm^2 based on ALTIROC front-end (TZ pre-amplifiers) and HGCROC ADC/TDC. Collaborators from AGH University of Science and Technology (Krakow) who designed the HGCROC 10-bit ADC provided an 8-bit version of the ADC for EICROC0. The purpose of EICROC0 is to evaluate the readout of AC-LGAD sensors with a dedicated ASIC. The schematic and the design corresponding to one EICROC0 pixel are represented on Fig. 24 and 25. The main components in a EICROC0 channel are:

- TZ Pre-amplifiers and discriminators taken from ALTIROC,
- I2C slow control taken from HGCROC,
- TOA TDC adapted by CEA/Irfu from HGCROC to EICROC0,
- ADC taken from HGCROC adapted to 8-bits by AGH Krakow,
- digital readout: FIFO depth 8 (200 ns),
- 5 slow control bytes per pixel:
  - 6 bits local threshold,
  - 6 bits ADC pedestal,
  - 16 TDC calibration bits,
  - several on/off and probes

The TDC developed by CEA/Irfu/DEDIP and included in HGCROC has been fully characterized. It used an architecture inspired by [16], based on time residual amplification but with extended dynamic range and improved robustness against PVT (Process, Voltage, Temperature) variations. Its orientation for low power consumption is also a key point in a pixelated environment. Indeed, the power consumption of this TDC is only present during the conversion of an event. Therefore, the consumption of this part is directly proportional to the rate of events arriving on the pixels. This multichannel architecture is presented in Fig. 26. The TDC is driven by a 160 MHz clock (CLK). This clock sequences an 8-bit Gray counter which outputs are broadcasted to all the channels. When a hit occurs on a channel, the counter output is captured on an 8-bit register. To refine the measurement, a coarse TDC (CTDC) based on a 32- step Delay Line (CDL) provides 5 more bits. To extract the less significant bits, the time residue between the hit and the next step of the CDL is multiplied by 8 (optionally by 16) by a time amplifier (TA) before being coded by a fine DL (FDL) over 3 (optionally 4) bits. Then, a digital block decodes and combines the data from the counter, the CDL and the FDL to form the TDC data coded in the nominal TOA mode of operation and 10 bits are kept. In order to keep these performances stable in time and with the environment, a common block (called MASTER DLL) is used which allows to make a permanent calibration on all the TDC channels. There is therefore no dead time relative to the calibration. In addition, a fine calibration system per channel is added. Even if the common calibration is essential, a fine calibration is necessary to compensate for the mismatch effects of the channels. This calibration is currently included in the chip and is adjustable by channel. As an illustration of the performance of this TDC, Fig. 27 shows that the Integral Non Linearity (INL) is close to $\pm$ 2 LSB (Least Significant Bit) and the LSB is as low as 13 ps. Such a performance fulfills EIC requirements. This existing TDC (1 mm $\times$ 120 μm) needed to be adapted in terms of dynamic range and resolution as well as spatially optimized to fit within a pad of 500 $\times$ 500 μm^2. On the other hand, the trigger-less architecture of EIC allows some simplification of the digital part of the ASIC compared to ALTIROC, giving a larger available area for the TDC. To achieve an excellent time resolution, any coupling between the sensor input and the digital electronics activity in the ASIC or the bias voltage connection (inductance) needed to be carefully controlled, which implied constraints on the module design.

The printed circuit board (testboard) associated to EICROC0 has been designed by OMEGA, was received and cabled at IJCLab in July 2022. Main components are level translators (1.2V and 2.5V), on-board regulators for low voltage, 4 SMA connectors for pre-amplifier signal output. Space have been left near the chip location to accomodate for AC-LGAD sensor wire-bonding. Pictures of an EICROCO chip placed on the bare printed circuit board are shown on Fig. 28.

As a first step, in September 2022, an EICROC0 has been wire-bonded by BNL. PCBs holding an EICROC0 are available at BNL and IJCLab. In order to control the parameters of the system, a Xilinx

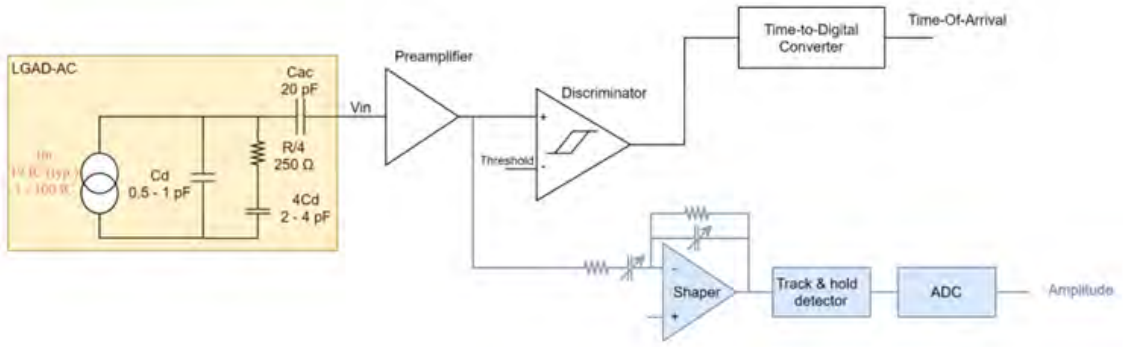


Figure 24: Schematic architecture of one channel of the EICROC0 ASIC prototype dedicated to the readout of an AC-LGAD sensor. A TDC is used to measure the time of arrival (TOA) of the charge and an 8-bit ADC measures the amplitude of the charge filtered by a shaper step.

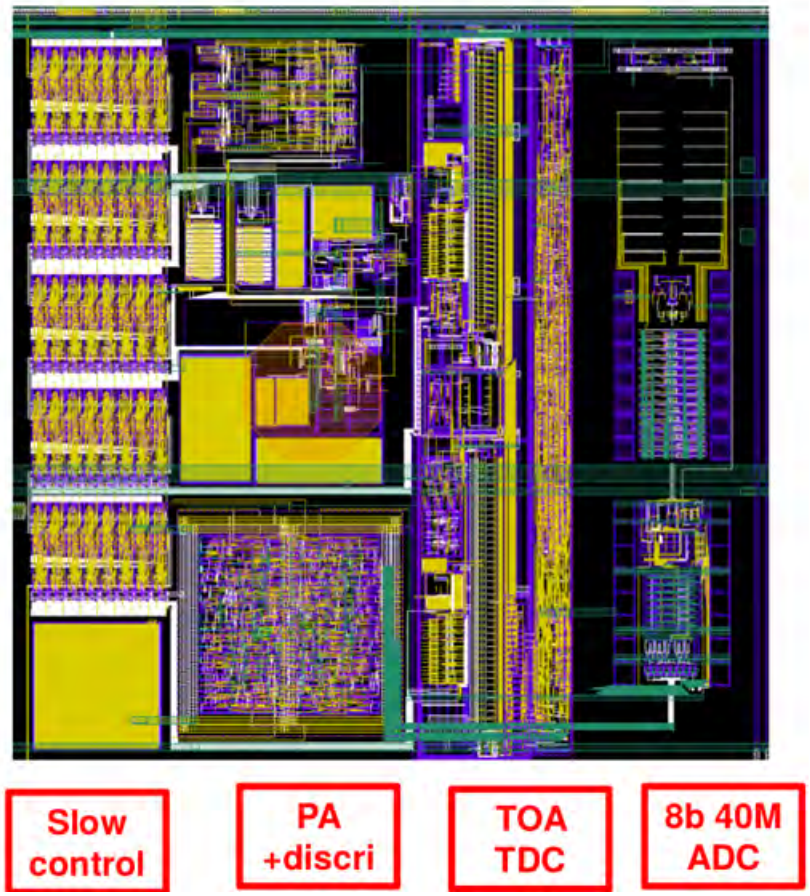


Figure 25: Design of one channel of the EICROC0 chip.

ZC706 (interface board) was purchased and the dedicated firmware has been developed at IJCLab. The connection between the interface board and the test board is made through a FMC connector. A picture representing a bare printed circuit board connected to the Xilinx ZC706 is shown on Fig. 29.

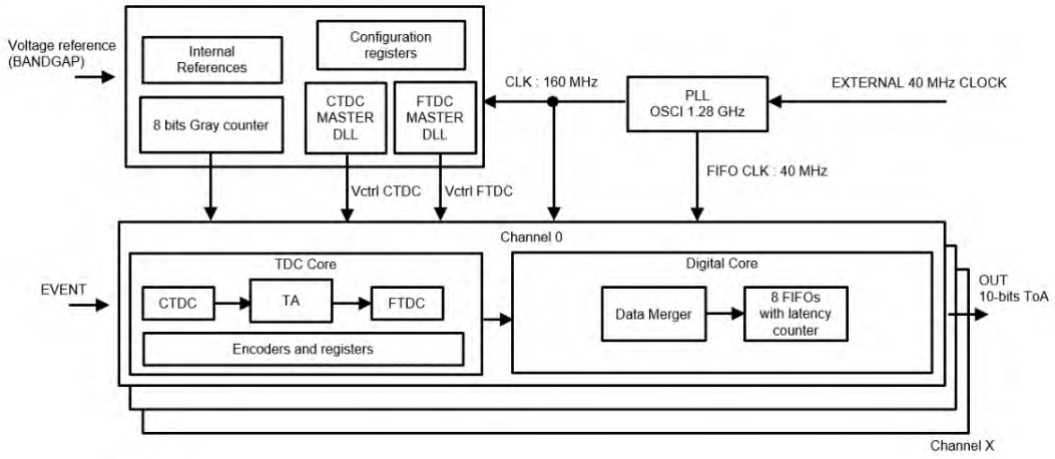


Figure 26: Block-diagram of the improved 3-steps multi-channel TDC.

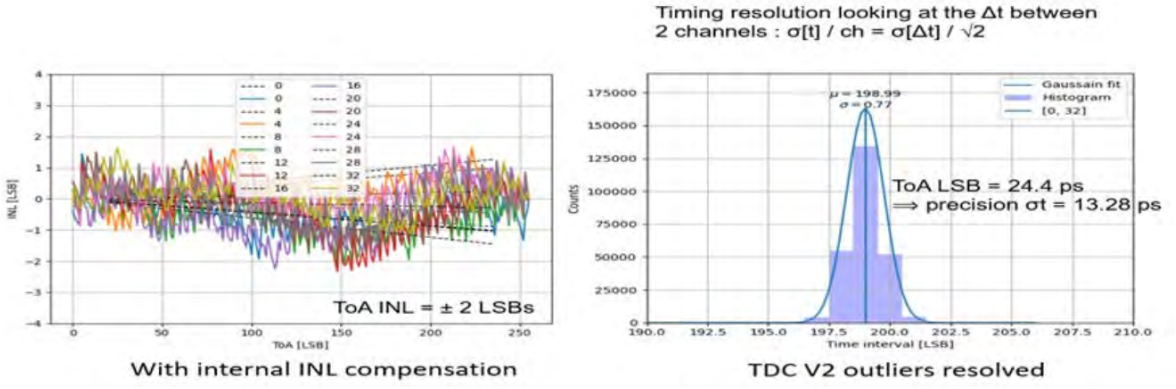


Figure 27: TOA channel INLs with internal compensation (left) and timing resolution histogram by difference between two channels (right). An individual temporal precision of 13 ps is extracted.

2.2.2 FCFDv0 design, submission and initial testing by FNAL

Design of the front-end electronics capable to extract precision timing information from LGAD sensors presents many challenges but plays a key role in the applications of the LGAD technology. The Fermilab and UIC team has been studying optimal methods for extraction of timing information from LGADs, using either Leading Edge (LE) or Constant Fraction Discriminator (CFD). Timestamping using the LE requires time-of-walk correction for optimal time resolution of the reconstructed signal, due to the dependence of the threshold-crossing on the signal amplitude. The CFD discriminant does not require such a correction and is therefore much simpler to operate and implement in large systems, without a need to derive and monitor signal dependence as the detector ages. Additionally, our studies in [5] showed that CFD outperforms LE for smaller signals, making it a preferred choice for AC-LGAD sensors which have smaller signals in non-primary channels due to signal sharing.

Following the studies presented in [5] the Fermilab team designed and produced the single-channel version an ASIC based on the CFD concept using TSMC 65nm technology (Fermilab CFD version 0, or FCFDv0). The FCFDv0 uses several new techniques to achieve low power, area, jitter, time walk. This enables a simple and robust timing measurement (30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required. The FCFDv0 is a single-channel ASIC that only contains analog blocks, i.e. the amplifier and discriminator. Another critical feature in the design and implementation of the ASIC was complete testability with simple bench-top equipment, to properly characterize and adjust the settings on the chip for optimal operation.

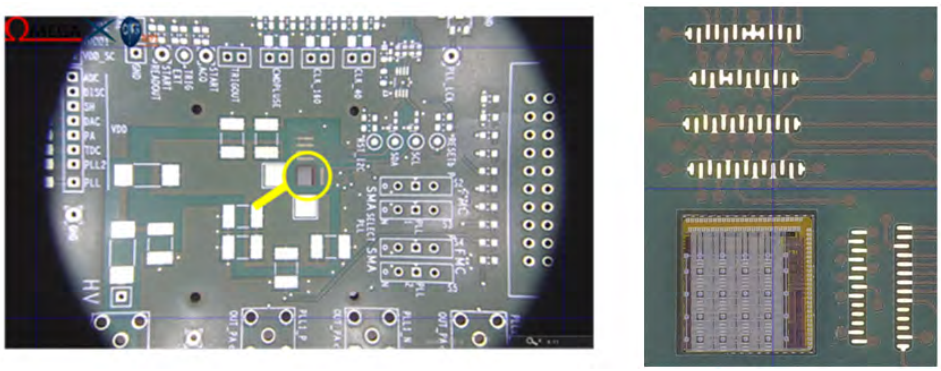


Figure 28: Pictures of an EICROC0 placed at its location on the bare printed circuit board. The picture on the right represents a zoom on EICROC0.

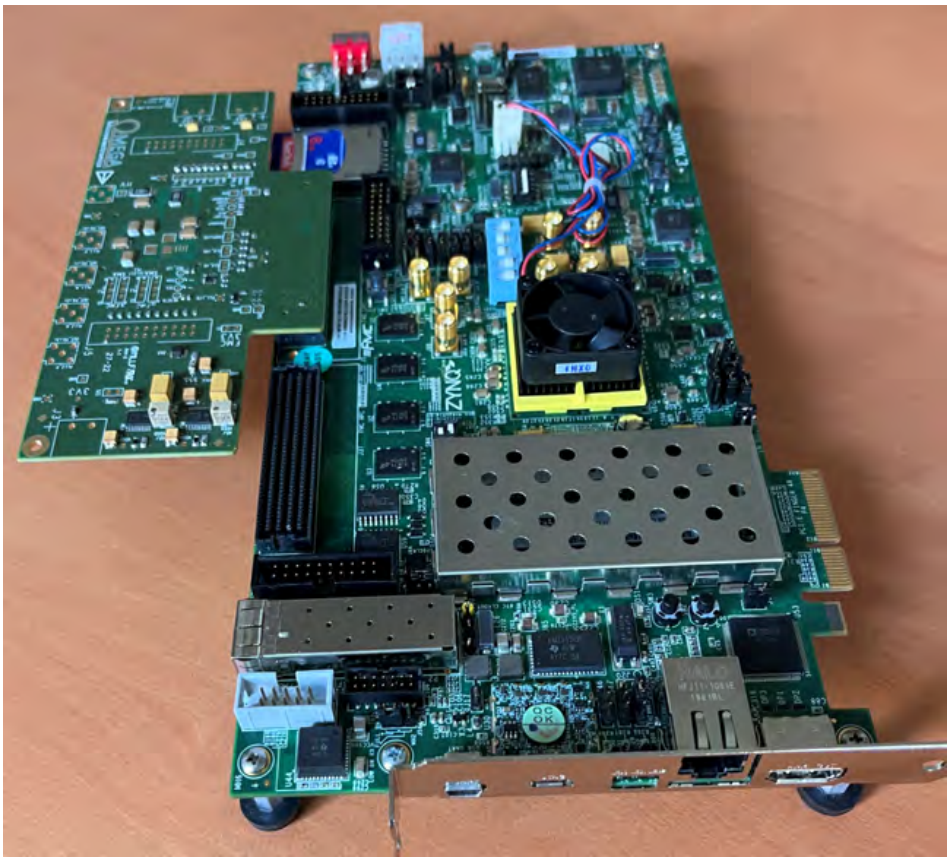


Figure 29: Picture of a bare printed circuit board connected trough FMC connector to a Xilinx ZC706.

The FCFDv0 forms both an attenuated and a delayed version of the amplified input pulse. The input stage is an integrator with a feedback capacitor and a parallel feedback resistor to provide "slow" continuous reset. The attenuated signal is derived very efficiently by splitting the integration capacitance into two series capacitors and buffering the midpoint node. The delayed signal is formed by a programmable RC delay on the integrator output, followed by a buffer. These two buffered signals then directly feed a fast differential amplifier. The single-ended output of the differential amplifier feeds a very simple output comparator that compares it to an internal DC threshold voltage. The biasing of the integrator and differential amplifier chain is critical to achieving the best performance and eliminating the need for any trimming. The integrator capacitor midpoint must have a DC bias

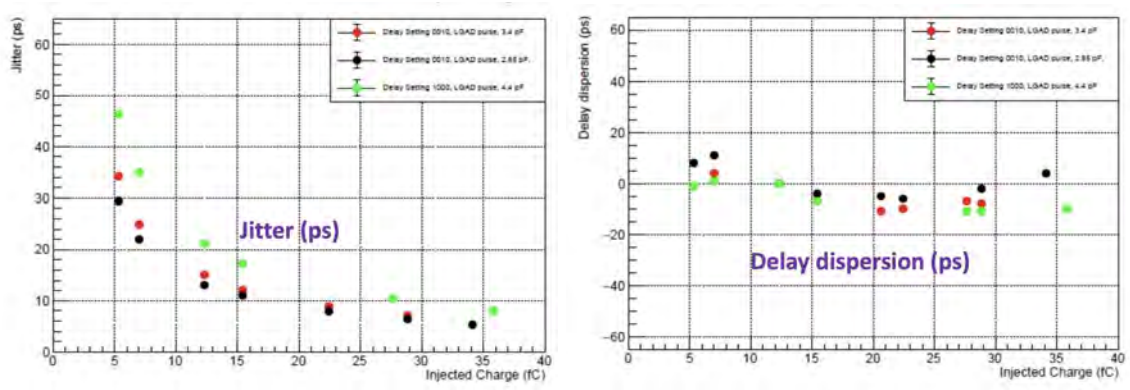


Figure 30: Measured delay jitter (left) and delay dispersion (right) vs. input charge. Red, black, and green points correspond to 3.4, 2.85 and 4.4 pF respectively.

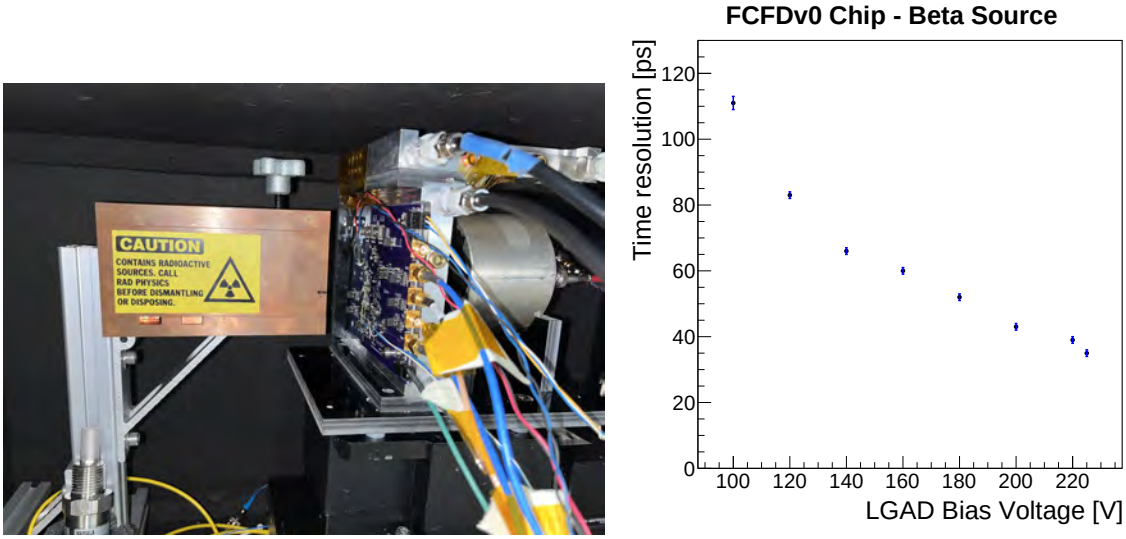


Figure 31: The setup to measure performance of the FCFDv0 with the beta-source (left), and the time resolution vs bias voltage measured using the beta source (right).

established, and the differential amplifier has a significant random input offset. A servo loop is used to establish the differential amplifier output voltage by sensing and filtering it and comparing it to an on-chip DC level setting. The capacitor midpoint is then driven appropriately to establish the desired DC output level of the differential amplifier. In a classical CFD, the output comparator would have its threshold set to the quiescent value of the differential amplifier output. However, large signals have more comparator overdrive than small signals, and thus smaller delays. To compensate for this effect, the differential amplifier output is biased at a critical level away from the comparator threshold.

The FCFDv0 chip has been characterized using internal charge injection circuit [6], and recently using an infrared (IR) laser at SiDet. The performance of the FCFDv0 chip was initially tested using the internal charge injection circuit. The LGAD-like pulse corresponding to a 50 μm thick DC-LGAD with 1.3×1.3 mm^2 pixels (C_{in}=3.4 pF) was injected into the circuit to emulate the realistic signals, and signal size was varied from 2.4 to 25.8 fC. The input transistor current was varied from 520 to 820 μA to study the dependence on the gain of the amplifier. Results are shown in Fig. 30 and demonstrate that the chip can measure the ToA down to about 8 ps with simulated signals. We also studied the delay of signals of various signals, to evaluate whether any residual time-walk correction is still necessary and observe negligible dispersion of the ToA of signals of different sizes, therefore demonstrating no need for time-walk correction.

As a next step we moved to characterize the performance of the FCFDv0 chip using signals from DC-LGAD sensors. A specialized readout board was designed by the Fermilab team for the measurements with source, shown in Fig. 31. For this test, sensors of 1.3×1.3 mm^2 are used. Sensors mounted on the readout board were placed inside an environmental chamber, and the beta source directed at the channel connected to the input of the FCFDv0. The output of the comparator was sent to one of the channels of the Lecroy Waverunner 8208HD oscilloscope, and trigger was generated by the Photek MCP-PMT behind the LGAD sensor. The difference between the time of arrival of two signals was then histogrammed, and the width of the distribution is extracted to evaluate time resolution of the LGAD+FCFDv0 system. The resulting dependence on the bias voltage applied to the LGAD is shown in Fig. 31, demonstrating that we achieve around 30 ps time resolution in a system containing real signals from LGADs, consistent with expectations for this LGAD sensor [8].

2.2.3 ASICs from third party institutions by SCIPP

The development work of LGAD sensors is currently based on high-speed readout boards with discrete components introduced by SCIPP and FNAL. This allowed the crucial characteristics of LGAD signals to be mapped out, however for EIC integrated ASIC has to be developed to allow for high density readout while maintaining a low power dissipation. The readout has to be suitable to the chosen sensor thickness, in Tab. 6 the signal proprieties of 50 μm and 20 μm LGADs are presented with the respective requirements for the ASIC.

LGAD characteristic	50 μm	20 μm
Rise time (10-90%) [ps]	455	182
Input charge [fC]	11	4.6
ASIC characteristic	**50 μm**	**20 μm**
Jitter [ps]	10	5
S/N	>50	>40
Voltage signal [mV]	70	70
Noise RMS [mV]	1.4	1.8
Internal sensor gain	20	20

Table 6: LGAD and ASIC characteristics for 50 μm and 20 μm LGAD sensor thicknesses.

In the area of ASIC development, in FY22 the SCIPP at UC Santa Cruz contributed by collaborating with third party institutions and companies to characterize and fabricate ASICs suitable for the readout of AC-LGADs at EIC. SCIPP role is to guide the chip development, develop of electronic board for chip characterization and testing the chip performance with calibration input and with an LGAD sensor with laser and Sr90 source. The three projects that SCIPP followed in the past year follows. A summary table of the ongoing efforts is in Tab. 7.

- FAST2, developed by INFN Torino: Longer shaping time ($\geq$ 800 ps) not optimized for thin sensors (200–500ps signal rise). Power draw: 1 mW/channel for analog, 1 mW/channel for discriminator/TDC. New design (FAST3) ready soon.
- ASROC: Uses fast SiGeprocess for front end. Promising design but prototype not yet in hand. Front-end power draw good ($\leq$1 mW) but not clear it can be mated to low-power CMOS for back-end. Future funding sources unclear
- HP-SoC: Full, highly flexible "system on chip" (SoC). Both front and back end carefully optimized for timing precision. Integrated 65 nm process promises low power for full readout chain. Ongoing project with DOE recognition and support. Prospective performance characteristic on following page. Power draw: 1.6 mW/chfor analog, 1 mW/ch for digitizer and 1 mW/ch for digital (current goal, still under development).

ASIC results have been reported during eRD112 meetings. In Fig. 32 (left) a photo of the HP-SoC chip mounted on the readout board developed at SCIPP can be seen, in Fig. 32 (right) the output pulse of the analog amplifier of HP-SoC using a 50 μm thick LGAD prototype from FBK. The pulse shows a very fast rise time of about 500 ps.

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

Table 7: Characteristics of ASICs followed by SCIPP.

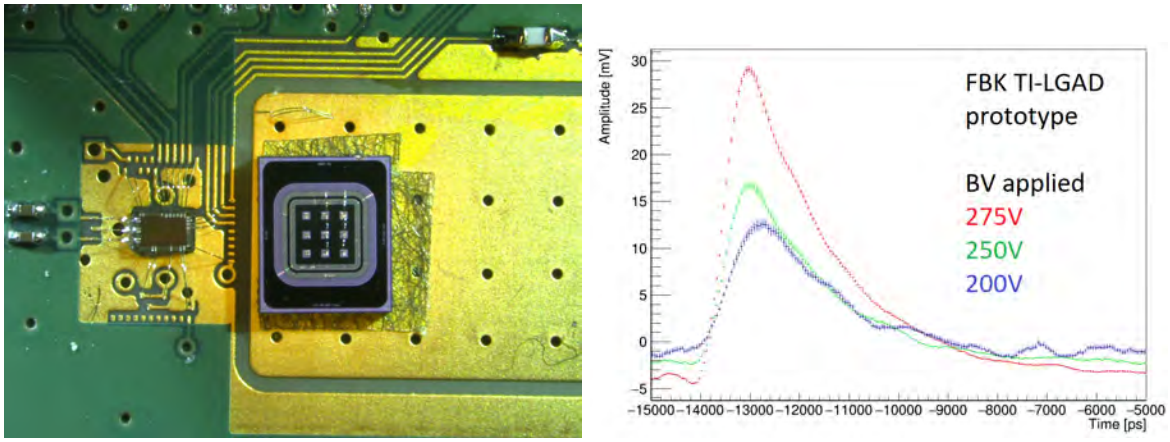


Figure 32: Left: HPSoC prototype by NALU Scientific (left) mounted on the test board developed at SCIPP and wire bonded to an FBK AC-LGAD (right). Right: Measured averaged pulses with HPSoC using an FBK TI-LGAD test sensor, biased at different voltages and irradiated with a Sr90 beta source.

3 FY23 Plan

In FY23, we will continue working with the EPIC collaboration to finalize the detector layout and requirements, exploring the possibility to have common designs where possible in the central and far-forward AC-LGAD detectors. We will also continue working on sensor and frontend ASIC development, and start looking into sensor/ASIC integration, frontend readout electronics, and mechanical supporting structures, as outlined already in the FY22 proposal [4]. Below we describe our plans in these areas.

3.1 AC-LGAD sensor

The first sensor production from BNL IO has shown promising results on both pixel and strip sensors with good timing and spatial resolutions. We will soon receive and test sensors from new BNL IO productions (section 2.1.1) and the first HPK production (section 2.1.2) that feature various pixel sizes, strip lengths and metal electrode widths to find optimal design parameters, and thinner active layer with improved intrinsic timing resolution. In FY23 we will continue the sensor development at BNL IO to utilize its great flexibility and fast turnaround time for sensor design optimization, and engage commercial vendors (e.g., HPK and FBK) to produce large area sensors to understand their yield/cost and quality. We will also investigate into sensor and ASIC integration, and finish the study on the radiation damage effect to the sensor performance. We summarize the proposed work below.

3.1.1 Sensor fabrication at BNL

BNL will fabricate one new batch of AC-LGAD, which will implement the modifications suggested by the test results of the FY22 batches. If the test results indicate good performance of thin sensors, the silicon substrates will be between 20 and 30 μm thick, while some 50 μm thick wafers will still be produced for reference. We foreseen the use of new photolithographic mask sets to accommodate changes in the geometrical layouts that may be prompted by the test results of the previous batches. Some aspects of the technology, such as the resistivity of the n-type layer and the implantation dose of the gain layer (the latter directly related to the breakdown voltage and thus to the operation point) will be addressed following discussions and recommendations from the collaboration. Therefore, in addition to changes and variations in the geometrical layout of the devices and active thickness, some variations in terms of doping concentrations in n-type and gain layer are expected for optimisation purposes. Furthermore, this batch will include devices that are geometrically compatible with the future EICROC ASIC iteration (EICROC1 and EICROC2) layouts.

The yield of the BNL clean-room technology process will be put under test, by means of fabricating large area devices. For this, a second batch of few wafers will be fabricated with new silicon substrates, as the yield may critically depend on the quality and defect density of the starting substrate.

Thanks to the return to BNL of one of our PostDocs who is currently based at CERN, an increased (and in-kind) effort in the characterization of the AC-LGADs will be carried at BNL. This includes not only the static, i.e. current-voltage and capacitance voltage characterization at the probe station required to select good devices to be sent out to the collaborators, but also functional tests with laser beams (TCT scans) and with radioactive sources such as Sr-90 etc.

In addition, the BNL team will assemble test-modules of EICROC (v0, and v1 when available) and AC-LGAD, either bump- or wire-bonded, for testing the readout functionalities of the assembly of the sensor+ASIC. Several of these assemblies will be distributed to collaborators in the consortium and a sufficient number of them will be kept at BNL for in-house testing with pulse generators, lasers and radioactive sources.

In summary, the BNL deliverables in FY23 will include:

- 1 batch of several AC-LGADs with optimised geometrical layouts, active substrate thickness and doping concentrations,
- half a batch of large area sensors to test yield efficiency,
- Several EICROC + AC-LGAD assemblies
- In-house performance characterisation of BNL's produced batches of AC-LGADs and EICROC + AC-LGAD assemblies.

3.1.2 Sensor/ASIC characterization and integration by UIC

In FY22, UIC worked closely with FNAL team on testing strip sensors with 120 GeV proton beams at Fermilab Test Beam Facility (see section 2.1.3). We have assembled a test stand with infrared laser of 3 ps jitter mounted on a precision 3D motor, allowing detailed sensor and frontend ASIC characterization in the lab, and a Xilinx ZC706 Dev Kit for ETROC0 readout using external funds. In FY23, we will continue working on characterization of sensors and frontend ASICs, by collaborating with FNAL team on beam tests of new sensors from BNL and HPK, and with EICROC and FCFD design teams to test these chips with infrared laser in the lab and proton beam at Fermilab.

Strip and pixel sensors with various pitch and electrode sizes are currently being studied to find optimal design. Due to the different requirements on timing/spatial resolutions and material budget by the various AC-LGAD detectors at EPIC, different sensor designs may be needed by different detectors. We propose to look into sensor/ASIC integration that can enable connecting strip sensors and pixelated frontend ASICs, or pixel sensors and pixelated frontend ASIC with different pixel sizes. This will faciliate testing of various sensors with the same ASIC in the current R&D phase, and provide a possible solution for sensor/ASIC integration in the construction phase. We will design and fabricate Silicon- or PCB-based interposers, which will be bump-bonded to pixelated ASICs from one side and then wire- or bump-bonded to strip or pixel sensors with different pitch sizes from the other side.

An important goal of the UIC group in FY23 is to design and assembly of a beam test setup using prototype AC-LGAD sensors and EIC frontend ASICs (EICROC/FCFD). So far the AC-LGAD lab/beam test has been mostly relying on Fermilab 16-channel analog test boards read out by high speed Oscilloscope. In order to fully establish the capability of prototype AC-LGAD sensor+ASIC, we will build a test beam telescope using AC-LGAD sensors read out by frontend ASICs dedicated for EIC (EICROC/FCFD). The mechanical structures of the telescope will be made from a 3D printer by an UIC undergraduate student, who is supported by internal UIC funds, and from UIC machine shop that features high quality work (STAR iTPC insertion tooling and Forward Silicon Tracker assembly jigs) at a very low rate ($7/hour). We will work with the EICROC and FCFD design teams on the data acquisition system.

We will continue providing services to the project to bump-/wire-bond and mount sensors and ASICs onto test boards, and do initial testing before distributing the boards to other groups.

The UIC deliverables in FY23 will include:

- Lab/beam testing results for the new AC-LGAD sensors from BNL and HPK,
- Lab/beam testing results for EICROC0 and FCFDv0
- Interposers that connect strip/pixel sensors with pixelated frontend ASIC with different pitches.
- Beam test setup at FTBF using prototype AC-LGAD sensors and frontend ASICs for EIC.
- Test boards with AC-LGAD sensors and frontend ASICs mounted and wire-/bump-bonded,

3.1.3 Sensor characterization and TCAD simulation by SCIPP

A significant component of the work proposed for SCIPP in FY23 will be a continuation of our program of characterization of new sensor prototypes produced by various vendors, including our direct collaborator BNL. These studies will include timing and position resolution, response uniformity, and radiation damage studies. These studies can be performed over a range of readout systems, including discrete systems readily available at SCIPP (the "SCIPP single-channel board" and the "FNAL 16-channel board"), as well as the developing ASIC systems discussed below.

In addition to our laboratory based capabilities described above (precision IV and CV measurements, and sources making use of beta particles and fast-pulsed lasers), Valuable characterization information comes from high-energy test-beam data, as available. Thus, we propose to contribute to the design, execution and analysis of test beam data acquired from runs at FNAL.

Particularly interesting is the prospect of improved timing resolution achievable with thin (20 μm bulk) sensors, for which the intrinsic timing resolution limit imposed by the statistics of the charge deposition process (the "Landau contribution" is better than for current 35 μm and 50 μm bulk prototypes. These thinner prototypes are currently under production at BNL. During FY23

We expect to be able to determine whether these sensors will provide a significant opportunity for improving LGAD timing resolution.

Another important contribution we propose for FY23 is the use of TCAD simulation to guide detector optimization. Our recent progress in reproducing laboratory and test-beam results with both 2D and 3D simulation gives us confidence that we can provide guidance to sensor design efforts as refined prototypes are developed. The optimization space for AC-LGAD design is large, including parameters such as gain-layer doping properties, n+ layer sheet resistance, electrode patterning, edge termination, etc. Use of TCAD simulation could prove critical in finding the optimum balance in the parameter space that provides maximum position and timing resolution, in understanding strip-length effects, and in providing input to electronics design efforts.

3.1.4 Sensor characterization and simulation by ORNL

The FY23 work includes testing and characterization of the AC-LGAD sensor prototypes developed as part of this eRD project. The Oak Ridge National Laboratory (ORNL) group will contribute to the successful completion of the planned sensor testbeam campaigns in FY'23. This will include in-kind participation in the data analysis in close collaboration with the other institutes involved in this proposal.

We also propose to perform "slow" simulation work for the AC-LGAD sensors developed as part of the eRD112 consortium using appropriate silicon sensor simulation tools. These studies will support the testbeam campaign data analyses with complementary simulation results. In addition, we plan to use these validated simulation models towards a parametrized input into an AC-LGAD sensor model which will become the basis of a sensor digitization module to be included into the EPIC simulation and analysis software framework. The work for simulation and analysis will be contributed in-kind.

3.1.5 Sensor characterization by Rice

The Rice team will continue the R&D of pixel AC-LGADs, a suitable candidate for the endcap TOF, in collaboration with other teams. The main goal is to fully characterize the performance of timing and position resolution for AC-LGADs with square pixel electrodes of various pitches and thickness to optimize for physics performance, material budget and power consumption. In FY22 RDs, a position resolution of $\sim$20 μm has been demonstrated with a 500 μm pitch. However, preliminary layout design of endcap TOF based on 500×500 μm^2 pixel AC-LGADs indicates a total power consumption that is likely excessive for cooling infrastructure and nearly detectors (e.g., EMCAL). Even moderate increase of pixel size can help significantly reduce the number of readout channels and thus power consumption (e.g., a factor of 2 reduction can be achieved by increasing the pixel size to 700×700 μm^2), while still fulfilling the physics requirements. It has been suggested that even with a pitch of 1300 μm AC-LGADs, a position resolution as good as $\sim$40 μm can still be achieved by sufficient gain and novel design of electrodes. In collaboration with BNL, we propose the fabrication of pixel AC-LGADs with a few choices of pitches ranging from 500 μm to 1300 μm, and thickness from 50 μm to 20 μm. We will then work together with other teams to carry out lab and beam tests of such sensors, and lead the data analysis of their performance.

3.1.6 Sensor irradiation test by LANL

In FY23, the LANL team will first complete the offline analysis of the radiated LGAD and AC-LGAD samples with the bench tests. We also plan to participate the beam tests at FNAL and join the offline data analysis to evaluate the AC-LGAD performance and study the tracking related performance. The proposed work activities will include:

- Characterize the analog output of radiated samples before and after the irradiation tests to compare the sensor performance.
- Study the digital signal amplitudes with the wire-bound AC-LGAD carrier boards from BNL (LANL will provide the assembled carrier boards) to use the 90^Sr source bench tests.
- Compare the pixel hit occupancy before and after the irradiation tests with different doses to check the noise rate dependence on the radiation doses and possible radiation damage effects.

We will lead the efforts to write the proposal, schedule and setup irradiation tests at the LANSCE facility if needed.

3.2 Frontend Readout ASIC

In FY23, we propose to continue the frontend ASIC development work in 1) EICROC 2) FCFD 3) ASICs from third party institutions. Among these efforts, our top priority is EICROC1 design and submission. To ensure that we will have frontend readout ASICs that meet the design specifications, we think that it will be also important to support also FCFD1 submission and characterization of the ASICs from third party institutions. The detailed plan is summarized below.

3.2.1 EICROC1 design and characterization

The work planned in 2023 is organized into 2 work packages:

- WP1: "Micro-electronics design" coordinated by Christophe de la Taille (OMEGA) involving CEA/Irfu/DEDIP, IJCLab and BNL.
- WP2: "Performance characterization" coodinated by Dominique Marchand (IJCLab) involving OMEGA, CEA/Irfu/DEDIP and BNL.

The EICROC timeline and project organization are displayed in Fig. 33.

Micro-electronics design (WP1)

WP1 is organized in 2 main tasks related to the design and the production of

- (Task 1.1) a small size 8× 4 (or 16×4 pads) ASIC prototype including a lower power ADC and adapted to EIC 100 MHz clock (**EICROC1**, Milestone 1.1, 3rd quarter of 2023),
- (Task 1.2) a full size 32×16 (or 32×32) ASIC (**EICROC2**, Milestone 1.2, mid 2025) to readout large area of AC-LGAD sensors.

The tasks associated to EICROC1 and EICROC2 are similarly organized in subtasks associated to all the stages mandatory to design, produce and test an ASIC, which include the design of each ASIC components (front-end electronics, TDC, ADC), the overall ASIC design layout and documentation, as well as the design of the dedicated electronics test benches.

OMEGA will be responsible for the overall design of the ASICs and the design of the front-end electronics (pre-amplifier and discriminator). In that context, OMEGA designers will closely collaborate with the CEA/Irfu/DEDIP team in charge of the design of the TDC and the IJClab electronics department, which is in charge of the design of the lower power ADC. The development of the test bench (specific boards for the ASIC, read-out boards and firmware) will be shared between OMEGA and IJCLab.

Task 1.1 which is the object of the FY23 budget request consists in the design, production and test of a small size prototype 8 (or 16) × 4 channels, called EICROC1, to study floorplanning.

Relying on the feedback of the measurements which will be performed with EICROC0, the goal of this prototype is to further optimize the very front-end and to include a lower power ADC and TDC fulfilling the 1 mW/channel EIC requirement.

The benefit of an ADC to measure the signal amplitude was explained in section 2.2.1. It is needed to correct for the time-walk for the timing measurement and to get a precise position with a barycenter technique.The free-running ADC adapted from a version developed by the AGH Krakow group which is implemented in EICROC0 is expected to work continuously and thus will be too much power-hungry.

The speed of 20-40 MHz and a resolution of 8 bits are not extreme, but it should be achieved with a lower power than the current state of the art (mW). In particular, the power budget should include the driving stage (shaper, buffer), which usually consumes several times more than the ADC itself. The study of a lower power ADC design has begun at IJCLab in close collaboration with OMEGA.

Task 1.1 is divided into 4 subtasks in order to explore several possible architectures for the sub blocks, probably including variants in columns to evaluate low-power front-end and digitization with a target of 1 mW power consumption per channel. The clock of 40 MHz will be also adapted to EIC (100 MHz input). Requirements serving EIC Roman Pots and ToF will be taken into account. The submission of EICROC1 design is scheduled for 3rd quarter of 2023 (Milestone 1.1).

Task 1.2 which will start in 2024 will be devoted to the design of a full size prototype of 32 $\times$ 16 (or 32) channels, EICROC2. Based on the tests of smaller arrays chips, a preferred architecture will be selected and extended to a full size matrix. At this stage, a whole column (32 pixels) needs to be implemented to investigate the power supplies and ground distributions along it and the possible voltage drops. In addition, a realistic implementation of all the digital blocks and clocks is mandatory as this is often a significant source of noise in detector systems. This task will therefore move more to digital design and integration. The tasks 1.2.1, 1.2.2 and 1.2.3 will implement corrections with respect to the corresponding tasks in 1.1 while more emphasis will be given to the task 1.2.4 regarding integration, simulation and validation steps. ASIC printed boards and interface boards will be re-designed according to the EIROC2 input/output signals in the task 1.2.5.

Characterization and performance measurements (WP2)

The ultimate goal being the demonstration that large size AC-LGAD sensors can be read by an ASIC and meet the EIC specifications, each component (sensor, ASIC) will be first characterized in a stand-alone mode to assess its intrinsic performance. In a second step, assembled devices (through wire bonding and bump bonding) will be tested to check any integration issue and finally be validated in realistic conditions with particles.

At IJCLab, in 2021 and 2022, relying on the ATLAS HGTD test-bench, characterization of ALTIROC1_v2 chip wire-bonded with a 3×3 pixelated AC-LGAD have been performed and measurements have been made using a ^{90}Sr beta source. The next stage is to expose this system to an infrared pulsed laser light (1056 nm) in order to study the charge sharing between neighboring pixels benefiting from a precise location of the light injection. This laser test-bench is inspired from the one exploited by BNL for measurements with the ALTIROC0 chip [17]. All equiments required to set-up the laser test-bench have been received. The commissioning of the test-bench is expected to start shortly and the measurements will follow. This laser test-bench will be also used for characterizing systems with each version of EICROC ASIC coupled with AC-LGAD sensors.

In parallel, since October 2022, the characterization of EICROC0 (Task 2.1) has begun with the commissioning of the EICROC0 test-bench. Then, the "channel by channel" electronics characterization of the chip wire-bonded on the PCB will be performed.

Tasks 2.1, 2.2 and 2.3 are associated to each iteration of the future EICROC, EICOC1 and EICROC2, and are subdivized in same subtasks:

Subtask #.1.1 consists in the stand-alone validation of the ASIC channels. The ASIC will be wire-bonded (or bump bonded) on a dedicated printed circuit and its characteristics, "channel by channel", will be studied using a calibration charge injection and an internal capacitance mimicking the sensor one. The main steps are the determination of the lowest threshold of the discriminator, the noise measurement and efficiency as a function of the charge. The TDC quantization steps will be measured by shifting the input calibration signal with a precise delay and the jitter extracted as a function of the charge. By injecting different charge input, the ADC quantification step and the ADC non- linearity will be extracted. The signal-over-noise at the output of the ADC is also a key measurement.

Subtask #.1.2 consists in reproducing the measurements done in subtask #.1.1 with a sensor connected at the input of the ASIC through wire bonding and bump bonding. The sensor voltage will also be supplied in order to deplete the sensor. This characterization of the system is a cornerstone step before starting to look at real energy deposits in the sensor as quite often integration issues/coupling are observed at this level and require a lot of time to be understood/solved. This subtask is a joint activity between IJCLab and BNL in close collaboration with OMEGA and CEA/Irfu/DEDIP.

Subtask #.1.3 consists finally in characterizing the module with realistic energy deposits. The module will be tested with particles, first with a radioactive beta (^{90}Sr) and it will be exposed to an IR laser light. Charge sharing and time resolution can be studied at this step. Eventually the module will be tested with hadron beam particles in a setup equipped with a precise beam telescope to fully assess the position and time resolution performance. Depending on the availability of the infrastructure, the beam test facility at FNAL (Chicago) with 120 GeV protons or at CERN-SPS with charged pions will be used. As teams from IJCLab and BNL are regular users of these beam lines for other projects, there will be no cost for testbeam.

Progress reports will be made at periodic meetings within the team and within the consortium. The resulting performances will be the object of presentations and publications (Deliverables D 2.1 and D 2.2).

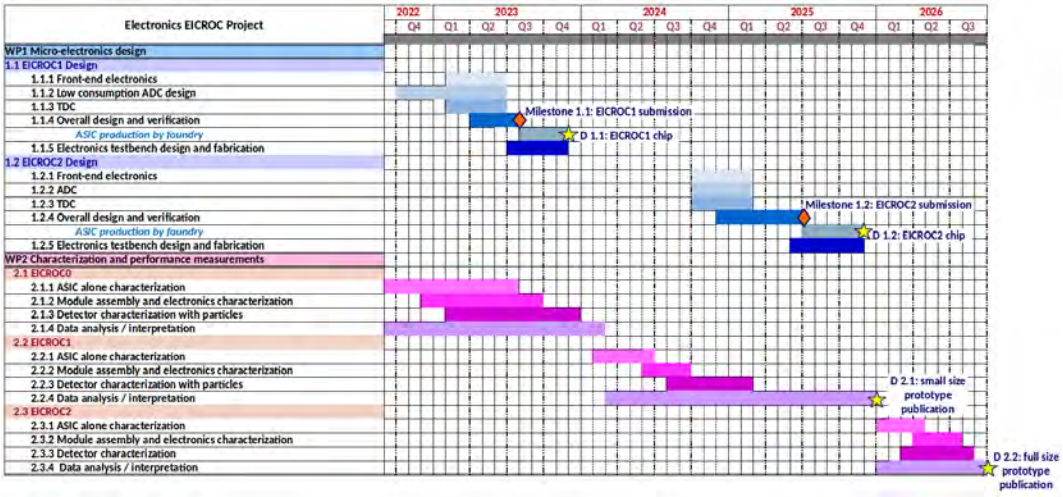


Figure 33: Timeline of the EICROC project.

3.2.2 FCFDv1 design and characterization by FNAL/UIC

We propose to develop the next generation of the FCFD chip, a specialized 10-channel ASIC designed to read out signals from LGADs. This next stage of the development program (FCFDv1) will reuse the main components of the analog part of FCFDv0, such as the preamplifier and discriminator, but will target the addition of charge measurement needed for position reconstruction in AC-LGAD sensors. The 10-chanel ASIC would allow to build a large-area demonstrator of the technology that would be able to perform simultaneous measurements of position and timing of the passage of charged particles. The development of this version is expected to take the first half of FY23. After the successful demonstration of the system readout with a 10-channel system during FY23 and FY24, the next step, FCFDv2 would aim to build a full chip, including the digital readout, during the second half of FY24 and first half of FY25 (10-channel FCFDv2). The final, mixed-signal ASIC will be produced and tested during FY25, and its performance will be characterized using a single-layer AC-LGAD demonstrator at FTBF.

In FY23 we will lead the study to finalize the specifications for the 10-channel FCFDv1 ASIC such that it is optimized for sensors suited for applications in EIC experiments, such as AC-LGADs with 500 μm pitch and 1.0 cm length of strips. Upon the completion of this study, we will lead the development of the ASIC and its submission to TSMC to manufacture a set of prototypes. Testing on the bench by the lead engineer will be performed first to validate the basic performance, followed by testing with the ASIC connected to AC-LGAD sensors in test beams. Similar to the experience with FCFDv0, we will develop specilized readout boards for the testing of ASIC+LGAD assemblies.

The ASIC design will be carried out by FNAL ASIC design engineers (Tom Zimmerman and others), who have decades of experience in designing ASICs for particle physics experiments, such as

the QIE used in CMS experiment at the LHC, ETROC for CMS timing detector, and FLORA for X-ray experiments at LCLS-II. The UIC and FNAL postdocs and students will develop the ASIC specifications based on detailed studies of test-beam data from AC-LGAD sensors, develop the DAQ, and perform the characterization of sensors in test-beams. The group will work with FNAL scientists S. Xie and C. Peña on the design and characterization of the FCFDv1 chip. The team also includes postdocs and graduate students from collaborating institutes (Caltech, BNL, UCSC, University of Santa Maria Chile).

Deliverable #1 in BY1: Specifications for the FCFDv1, and selection of the sensors for demonstrator.

Deliverable #2 in BY1: Design, submission and initial testing of 10-channel FCFDv1.

Deliverable #3 in BY2: Detailed characterization of the FCFDv1 performance summarized in a publication.

Deliverable #4 in BY2: Design of the mixed-signal final 10-channel FCFDv2 ASIC for the demonstrator.

Deliverable #5 in BY3: Completed technology demonstrator, detailed studies of its performance and publication.

3.2.3 Characterization of ASICs from third parties by SCIPP

In collaboration with two small electronics firms, SCIPP is currently a driving force in the development of two complementary approaches to LGAD readout. These include the CMOS-based HPSoC precision-timing "system on chip" development (Nalu Scientific) and the SiGe-based low-power ASROC front-end development (Anadyne, Inc.), both described above. We plan to continue our collaborative work with these two companies. For the case of HPSoC, characterization data accumulated for the initial five-channel prototype has allowed Nalu to begin, under our continued guidance, the refinement of the front-end design to meet the emerging goals of the EIC Detector effort. Support from this source, coupled with that expected from other sources, should allow the HPSoC collaboration to produce and characterize a second, more optimized prototype with a 10 Gs/s back-end digitizer. For the case of the ASROC effort, the FY23 will be expected to produce and characterize the first prototype of a 16-channel SiGe-based front-end amplifier ASIC geared towards the specific design goals of EIC LGAD sensors. SCIPP will also continue to collaborate with INFN Torino for the characterization of the FAST family of chips of which a new version is expected soon.

3.3 Frontend Electronics

To accompany the AC-LGAD frontend readout ASICs described above, dedicated readout electronics need to be developed and designed to provide the necessary clocks and slow control signals to the readout ASICs as well as receive, aggregate and submit the readout data out of the spatially constrained detector volume. To this end, we propose to form a collaborative AC-LGAD readout electronics working group between BNL, ORNL and Rice University to address these challenging questions.

This work will include fundamental R&D on an integrated clock conditioning and distribution system that meets the low jitter requirements of a sub-30 ps MIP timing system and implementation studies on streaming data acquisition architectures with the EICROC family of readout ASICs, based on "commercial off the shelf" FPGAs and components. At the same time, specific implementations of such systems, including power distribution and slow control links, will be studied and developed for the barrel and endcap regions of the TOF system. While we envision both barrel and endcap readout system to be based on the same general architecture, the differences in readout channel density, sensor module geometry and spatial constraints warrant independent (yet closely collaborative) developments for each region. The resulting readout board concepts will be applicable as an immediate basis for developments towards the readout system of the far-forward AC-LGAD detector systems.

3.3.1 Readout board and precision clock distribution by BNL

The plan of the BNL group is to develop the readout chain from the dedicated ASIC to downstream off-detector electronics. We will start by procuring a Xilinx Dev Kit and characterizing it to read the EICROC0 and EICROC1 mounted on the PCB developed by the French team. For the first step the sensor is not essential and we will only study the basic performance of the chip. The first tests

of functionality of the FEEs will focus on noise studies, time walk and jitter and compatibility with the AC-LGAD system requirements. Along this line we will also explore various timing chips ("clock cleaners and jitter removal") which is a critical component for any TOF based detector.

The deliverable for the BNL group for FY23 is development of the preliminary prototype of an integrated readout board that supports the first iterations of the EICROCx. The ultimate plan of the BNL group is to design the overall architecture of the hardware including, the design of the cable, the optimization of streaming data, and the interface of the timing and control signals.

3.3.2 Barrel TOF service hybrid by ORNL

The work proposed for FY23 includes basic R&D for the design and construction of the power delivery and readout service system ("service hybrids") for the barrel TOF system to serve as a basis for the upcoming CD2 review. These service hybrids will connect to a row of AC-LGAD readout chips on a given TOF stave module and aggregate their data into a single data stream. At the same time the service hybrids deliver power distribution, sensor biasing, voltage regulation and slow control services to and from all readout chips and sensor modules.

With the proven experience of ORNL in designing thin, durable circuits based on Kapton-flex foil, we will explore a service hybrid design based entirely on such flexible PCBs to minimize the material budget. We envision an architecture based on a single FPGA per service hybrid responsible for data reception, aggregation and slow control of the connected readout chips as well as the data transmission via a connected fiber transceiver or high bandwidth e-links. Our R&D will explore the maximum number of readout chips we can connect to a given FPGA, which informs the maximum distance between readout chip and FPGA over which raw readout data needs to be transmitted. This has to be done in close connection with the mechanical design of the barrel TOF system, as the signal routing and flex PCB layout necessarily has to follow the mechanical structure of the detector. An additional goal of our R&D will be the specification and basic demonstration of the required grounding and DC-DC powering schemes over the length of a TOF barrel stave.

The ORNL deliverable towards the TOF readout electronics includes a study to build TOF service hybrids out of flexible Kapton PCBs with integrated data aggregation and power distribution. Prototypes will be constructed to investigate the mechanical stability, signal integrity and power distribution capabilities of such assemblies.

3.3.3 Endcap TOF service hybrid by Rice

As one of main milestones planned for FY23, the Rice team will contribute to the development of a general layout of frontend readout electronics, focusing on the endcap TOF disks with pixel AC-LGADs, to be used as baseline for the CD2 review. We propose to develop a prototype frontend "service hybrid" based on a compact design of a readout board and power board to minimize material budget and space constraint. A prototype readout PCB board that provides a series of frontend services will be developed: (1) connectors that are compatible with EICROCs via flex cables; (2) data aggregation and transmission via electronic links and transceiver chips (e.g., lpGBT and VTRx+ by CERN); (3) slow control chip; (4) connectors to bias voltage power supply. A power board will provide low voltage power supplies to EICROCs and other on-detector chips for data transmission and slow control. We propose to build a power board based on CERN bPOL12V DC-DC converters with one layer planar spiral coil and a small connector that is pin compatible with the CERN bPOL12V_CLP module. The power board will also have a connector to low voltage power supply cables. With the anticipated delivery of first version of EICROC, our goal is to demonstrate a prototype full chain readout from the frontend to backend.

3.4 Mechanical Structure

3.4.1 Light-weight support structure by Purdue and NCKU/AS

Purdue University, National Cheng Kung University (NCKU, Taiwan), and Academia Sinica (AS, Taiwan) will collaborate on the design and manufacture of the mechanical support structure for the TOF detector in EPIC. To meet the required precision and material budget of TOF measurements, carbon fiber composite materials have been proposed for manufacturing the light-weight support due to their high thermal conductivity, strength to mass ratio, and radiation tolerance.

3.4.1.1 Prior Experience

- **NCKU** has been working on various detector structure and cooling related projects, including the STAR Forward Silicon Tracker (STAR FST) and AMS-02 Upgrades Thermal Tracker Pump System (AMS-02 UTTPS). NCKU also has strong collaborative relationship with the world leading aerospace company in Taiwan, Aerospace Industrial Development Corporation (AIDC), who is also the expert on composite materials including carbon fibers.
  - STAR FST: the mechanical structure is designed by the NCKU High Energy Physics group using injection moulding method with PEEK material. The thermal simulation was also performed by NCKU and tested it at BNL. The module assembly and quality assurance were done by the machines at Taiwan Instrumentation and detector consortium (TIDC). Figure 34 shows the gantry system at TIDC, fully assembled STAR FST module, and the thermal simulation and tests.
  - AMS-02 UTTPS: NCKU collaborated with AIDC working on the manufacture of the radiator for the AMS-02 UTTPS project. The radiator is made by aluminum plats with Inconel 718 tubes embedded for the heat transfer by the two-phase carbon dioxide. Figure 35 shows the basic design, final flight unit of the AMS-02 UTTPS radiator, and the installation of AMS-02 UTTPS on the International Space Station.

- **Purdue** has in-depth experience with the design and manufacturing of light-weight composite radiation-hard support structures. The CMS upgrade project due to the High-Luminosity phase of the LHC relies on Purdue for the design manufacturing of a variety of critical mechanical support structures as listed below.
  - Service Cylinder housing the Inner Tracker (IT)
    - 4+2 half cylinder structures with a length of 2.9m and transition region between small large radii
    - Barrel, Forward, and Extended Pixel Detectors
  - Components for Inner Tracker pixel detector
    - Sandwich structures to mount pixel modules (Dee's) for the forward pixel (US project)
    - CFRP structures for the barrel pixel (European led)
  - Inner Tracker Support Tube (ITST)
    - Supports the 4 IT Service Cylinders, separates Inner Tracker and Outer Tracker volumes
    - Longitudinal stiffness for the entire Outer Tracker
    - Directly supports 1st layer of the flat barrel section
  - Components for Outer Tracker (OT) modules
    - CFRP stiffeners for the OT modules assembly
    - More than 100,000 stiffeners corresponding to a CFRP area of 3000 square feet with extreme flatness.
  - Barrel Timing Layer Tracker Support Tube (BTST)
    - Supports timing layer and entire tracker
    - 5.9m long and 2.4m diameter structure with a sandwich of CFRP and a NOMAX core

  Each of these structures come with tight tolerances and specific demands to maintain envelope which results in the need for novel approaches and custom solutions to any and and all of these structures. Figure 36 shows a selection of pictures of prototypes, final structures, R&D related activities and finite element analysis related to these projects.

For the initial design of barrel TOF layout, the design concept similar to the STAR Intermediate-Silicon Tracker is adopted. In this design, the barrel is split into two sections in the beam direction and there are 144 TOF modules in each section. These 288 modules in total are estimated to have a weight of about 70 kg with power consumption of about 4 kW. The main body of a module consists of the mechanical support made by carbon fiber, with a cooling tube embedded. With the length of

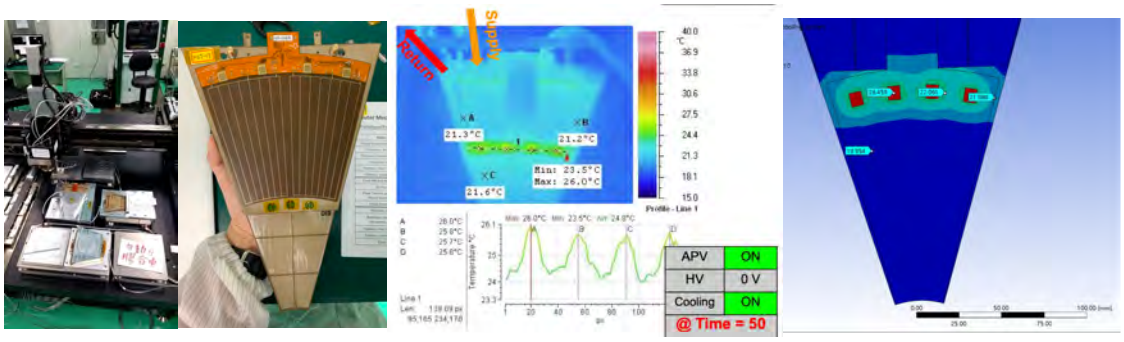


Figure 34: From the left to right: the gantry system at TIDC, fully assembled STAR FST module, thermal test and simulation results.

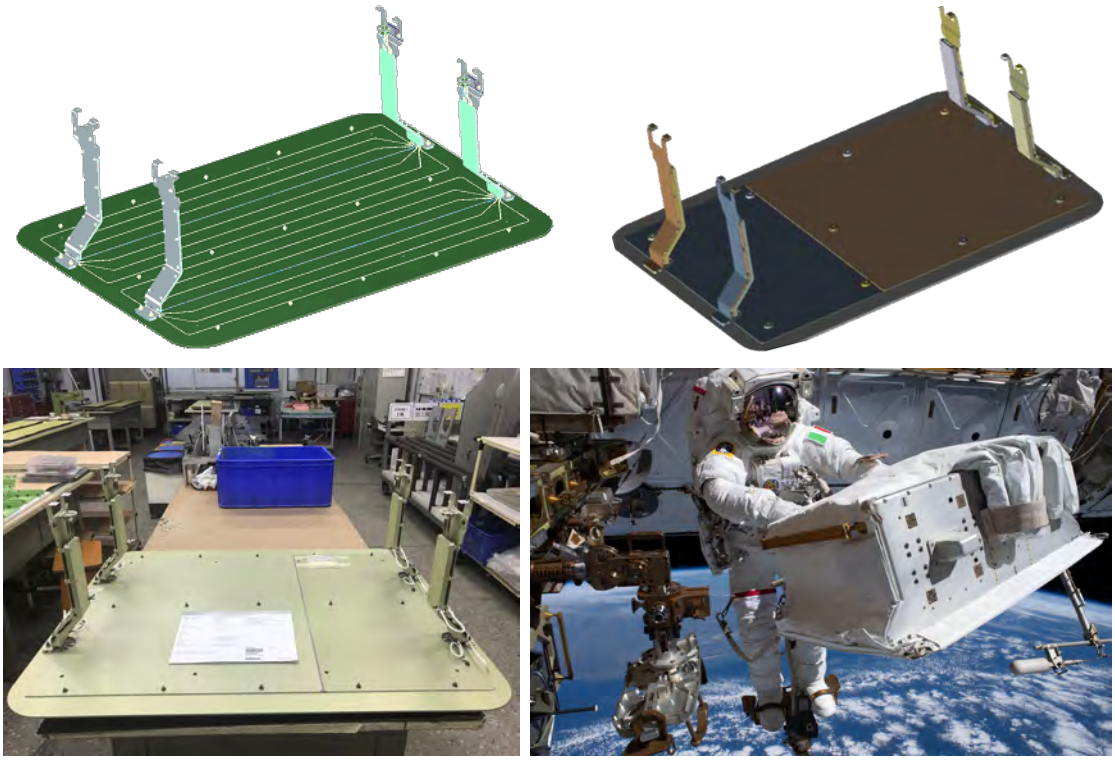


Figure 35: Top: the design of the radiator of the AMS-02 UTTPS. Bottom left: the flight unit of the AMS-02 UTTPS radiator. Bottom right: the installation of AMS-02 UTTPS on the International Space Station [18].

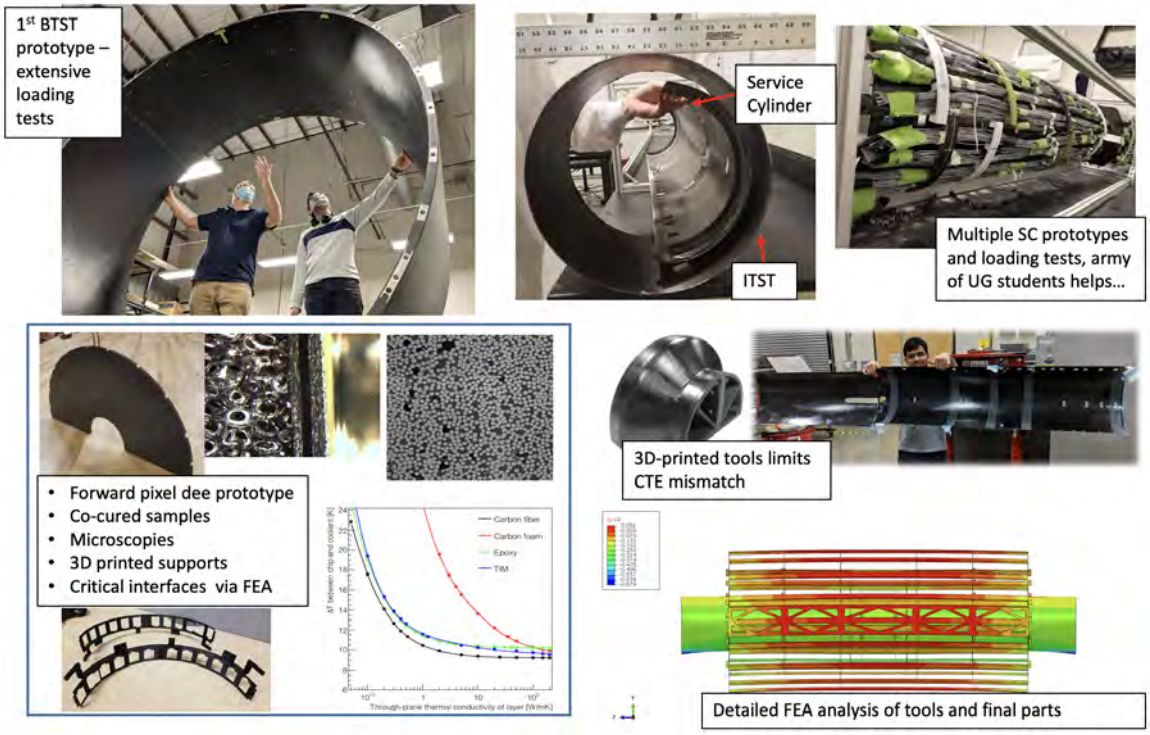


Figure 36: Selection of pictures of prototypes, final structures, R&D related activities and finite element analysis done at Purdue University. Labels provide minimal guidance to these pictures.

each module of 1.35 m, the challenge of this R&D project will be controlling the deflection within the order of a few hundred μm and the average material budget of a TOF module to be less than 1%.

As to the endcap TOF layout, a "clam shell" (DEE) design similar to the CMS End Cap Timing Layer has been brought up. The support structure will be designed to meet the same deflection tolerance and similar material budget mentioned for the barrel TOF, in the same time manage the total power consumption which can be as high as about 14 kW in the forward endcap and 8 kW in the backward endcap in a rough estimation. However, the other possibility for the endcap TOF module can be based on the similar design of the STAR Forward Silicon Tracker using the PEEK material with cooling tubes embedded. This proposed R&D project will proceed in both directions.

We expect to have a prototype in September 2023. A cost-effective approach will be adopted by using non-final material instead and the finite element analysis for the optimization of design.

3.5 Required Project Engineering and Design (PED)

A number of AC-LGAD detector system aspects which constitute project engineering, rather than the fundamental R&D proposed here, will need to be addressed in time for the CD2/3a review. This includes preliminary mechanical and electrical engineering design of the far-forward and TOF barrel and endcap detector systems to be able to connect all electrical, optical and cooling services and provide a realistic plan of pre-assembling modules and services onto the mechanical structure, so that the assembled detectors can be integrated into EPIC with minimal post-assembly. Prototype mockup structures will need be constructed to demonstrate the feasibility of production and assembly of individual parts where necessary. A detailed study of an appropriate cooling system will also be needed to quantify potential heating effects of surrounding detector systems, specifically the very temperature sensitive backwards ECAL crystals. Prototype production and testing of full scale service hybrid boards, firmware implementations of the downstream link towards the data aggregation modules are also needed to demonstrate the readiness of the concept at CD2/3a. The details of the plan and funding requests will be described in a separate Project Engineering and Design (PED) request submitted to the EIC project.

4 FY23 Resource Request

To perform the proposed work in FY23, we request 462k$ funds through eRD112 for sensor, sensor/ASIC integration, and light-weight mechanical structure R&D, and 267k$ through eRD109 for frontend ASIC and electronics R&D. The breakdown of these requests can be found in Tab. 8-11. Details of resource allocation at each institution are also included.

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Sensor Production				**175**
BNL IO	Sensor fabrication (incl. labor)	50 (10 wafers)	1.5	75
HPK/FBK	Sensor fabrication	75+3-5/wafer	1	100
Sensor Characterization				**13.7**
UIC	M&S for test beam setup	-	-	5
LANL	M&S for irradiation test	-	-	5
SCIPP	Fermilab 16-channel boards	-	-	3.7
Sensor/ASIC Integration				**30**
UIC	Interposer fabrication and bump-bonding	30	1	30
Mechanical Structure				**15**
NCKU	Material for light-weight support structure	-	-	10
Purdue	Material for light-weight support structure	-	-	5
Travel				**21**
BNL	Trips to Fermilab testbeam	2	2	4
UIC	Trips to Fermilab testbeam	1	5	5
ORNL	Trips to Fermilab testbeam	3	2	6
Rice	Trips to Fermilab testbeam	3	2	6
TOT.				**254.7**

Table 8: eRD112 resource request for M&S costs in FY23, excluding frontend ASIC and electronics.

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Sensor R&D				**172.3**
BNL	Sensor+ASIC and test board assembly	El. Tech.	10	20
UIC	Sensor+ASIC and test board assembly	El. Tech.	10	15
	lab/beam test for sensors and ASICs	Research Sp.	50	45
LANL	Sensor irradiation test	Scientist	2.5	10
	Sensor irradiation test	Student	5	5
Rice	pixel sensor test	Postdoc	40	40
SCIPP	Oversight and coordination	Project Scientist	5	9
	TCAD sim. and sensor design	El. Design Specialist	10	16.5
	Prototype Assembly	EM Engineer	5	11.8
Sensor/ASIC Integration				**15**
UIC	interposer design and testing	El. Engineer	10	15
Mechanical Structure				**20**
NCKU	light-weight support structure R&D	Mech. Engineer	10	5
Purdue	light-weight support structure R&D	Mech. Engineer	10	15
TOT.				**207.3**

Table 9: eRD112 budget request for labor costs in FY23, excluding frontend ASIC and electronics.

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Frontend ASIC				**118.3**
IJCLAB	EICROC1 submission	65	1	65
	EICROC test boards	-	-	10
FNAL	FCFDv1 submission	25	1	25
	FCFD test boards	-	-	15
SCIPP	ASIC service boards	-	-	3.3
Frontend Readout Electronics				**31**
BNL	Xilinx Dev Kit	4	1	4
	Timing cihps and boards	15	-	15
ORNL	Xilinx Dev Kit	4	1	4
	M&S	8	-	8
TOT.	-	-	-	**149.3**

Table 10: eRD109 budget request for M&S costs in FY23 on frontend ASIC and electronics.

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Frontend ASIC				**29.7**
SCIPP	Service board design layout	Electronic Design Specialist	7.5	12.4
	Board Assembly	Electro-Mechanical Engineer	5	11.8
	Board loading and lab msmt	Assistant specialist	5	5.5
Frontend Readout Electronics				**88**
BNL	Readout and Timing Distribution	Research Associate	20	38
ORNL	Barrel TOF Low-Mass Service Hybrid	Electric Engineer	10	32
Rice	Endcap TOF Service Hybrid	Electric Engineer	15	18
TOT.	-	-	-	**117.7**

Table 11: eRD109 budget request for labor costs in FY23 on frontend ASIC and electronics.

4.1 AC-LGAD Sensor

4.1.1 BNL

Given the BNL deliverables listed above, the BNL budget request for FY23 consists of 75k$ for the fabrication of 1.5 batches of AC-LGADs: 50k$ for a batch of 10 wafers and 25k$ for half a batch of 5 wafers. In addition, 20k$ for sensor+testboard assembly (incl. wire/bump-bonding). Sensor dicing and testing before distribution as well as sensor testing by a technician and a postdoc will be provided in-kind. Finally, we request 4k$ for the cost of 2 travels to FNAL for test-beams (2k$ each).

4.1.2 HPK/FBK production

We request 100k$ for the cost of new sensor production with the commercial vendors (HPK/FBK).

4.1.3 UIC

Workforce at UIC on EPIC includes: 2 faculties, 1 electrical engineer, 1 electrical technician, 1 postdoc, 2 graduate and 1 undergraduate students. Tab. 12 contains the resource allocation on sensor R&D.

4.1.4 LANL

Workforce at LANL on EPIC include: 1 staff scientist and 1 graduate student. Tab. 13 contains the breakdown of the resource allocation at LANL on sensor R&D.

Resource	Task	FTE (%)	Budget (k$)
Faculty	coordination, detector design	15	0 (in-kind)
Researcher	lab/beam test	50	45
Graduate Student	lab/beam test	25	0 (in-kind)
Undergraduate Student	3D printing and assembly of AC-LGAD telescope	15	0 (in-kind)
Electric Technician	Testboard assembly and bump/wire-bonding	10	15
Materials and Supplies	test beam setup	-	5
Travel	beam test	-	5
Total	-	-	**70**

Table 12: UIC budget request for FY23 on sensor R&D. All entries in thousands of dollars.

Resource	FTE (%)	Budget (k$)
Staff Scientist	2.5	10
Graduate Student	5	5
Materials and Supplies	-	5
Total	-	**20**

Table 13: LANL budget request for FY23 on sensor R&D. All entries in thousands of dollars.

4.1.5 ORNL

Workforce at ORNL on EPIC include: 0.5 Faculty (20% FTE) + 4 staff scientists (20% FTE), 2 technical staff, 1 postdoc (50% FTE), and part time of 1-2 graduate students. Tab. 14 contains ORNL allocation on sensor R&D.

Resource	Task	FTE (%)	Budget (k$)
Staff Scientist	Sensor simulation	20	0 (in-kind)
Travel	beam test	-	6
Total	-	-	**6**

Table 14: ORNL budget request for FY23 on sensor R&D. All entries in thousands of dollars.

4.1.6 Rice

The budget request by Rice group is summarized in Tab. 15 including support of a postdoc researcher at 0.5 FTE to advance the TOF layout design and carrying out pixel sensor (focusing on endcap TOF) testing and optimization toward the final design choice.

Resource	Task	FTE (%)	Budget (k$)
Postdoc	endcap TOF layout design	10	0 (in-kind)
Postdoc	pixel sensor testing (lab/beam)	40	40
Travel	beam test	-	6
Total	-	-	**46**

Table 15: Rice budget request for FY23 on sensor R&D. All entries in thousands of dollars.

4.1.7 SCIPP

Workforce at SCIPP on EPIC include: 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, 8 undergrad students.

Resource	Task	FTE (%)	Budget (k$)
Project Scientist	Oversight and coordination	5	9.0
Electronic Design Specialist	TCAD sim. and sensor design	10	16.5
Electro-Mechanical Engineer	Prototype Assembly	5	11.8
Materials and Supplies	Fermilab 16-channel boards	-	3.7
Total (Sensors)	-	-	**41**

Table 16: SCIPP budget request for FY23 on sensor R&D. All entries in thousands of dollars.

4.2 Frontend Readout ASIC (eRD109)

4.2.1 IJCLab, OMEGA and CEA/Irfu

The FY23 budget request presented in Table 17 relates to the submission of EICROC1 within a Multi-Project Wafer (MPW) and the purchase of associated components such as the fabrication of printed circuit boards and cabling. The labor of French institutions collaborators will be in-kind. For future developments, such as those related to EICROC2, IJCLab, OMEGA and CEA/Irfu/DEDIP team will keep seeking funds from French funding agencies but such funds are not secured.

Institution	Resource	Task	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	WP2	60	0 (in-kind)
	Senior scientist	WP2	35	0 (in-kind)
	Senior scientist	WP1&2	20	0 (in-kind)
	Research engineer	WP1&2	30	0 (in-kind)
	Research engineer	WP2	25	0 (in-kind)
	PhD student	WP2	50	0 (in-kind)
	EICROC1 [8 (or 16) $\times$ 4 channels] submission (MPW)	-	-	65
	Fabrication of testboards and associated components	-	-	10
OMEGA	Senior research engineer	WP1	25	0 (in-kind)
	Senior research engineer	WP1	20	0 (in-kind)
	Research engineer	WP1	15	0 (in-kind)
	Assistant engineer	WP1	20	0 (in-kind)
CEA/Irfu	Senior research engineer	WP1	30	0 (in-kind)
	Senior research engineer	WP1	10	0 (in-kind)
Total	-	-	-	**75**

Table 17: eRD109 budget request for FY23 on EICROC. All entries in thousands of dollars.

4.2.2 FNAL

The FY23 budget request of the FNAL team is to support the production cost of the ASIC submission, and production cost of the readout boards ($40k).

Resource	Task	FTE	Budget (k$)
Staff Scientists	oversight and coordination	5	0 (in-kind)
Postdoc	Sensor testing	15	0 (in-kind)
Engineers	FCFDv1 design	25	0 (in-kind)
Postdoc	FCFD+Sensor testing	25	0 (in-kind)
FCFDv1 Multi-Project Wafer (MPW)	-	-	25
FCFD test boards and components	-	-	15
Total	-	-	**40**

Table 18: eRD109 FNAL Budget request for FY23 on FCFD. All entries in thousands of dollars.

4.2.3 SCIPP

Workforce at SCIPP on EPIC: 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, 8 undergrad students. Given the involvement of SCIPP both in the sensor and ASIC development a support in both. The total budget amount requested by SCIPP is 100 k$ split evenly between the two efforts, Tab. 19 contains the breakdown of the budget allocation at SCIPP.

Resource	Task	FTE (%)	Budget (k$)
Electronic Design Specialist	Service board design and layou	7.5	12.4
Electro-Mechanical Engineer	Board Assembly	5	11.8
Assistant specialist	Board loading and lab msmt	5	5.5
Materials and Supplies	ASIC service boards	-	3.3
Total	-	-	**33**

Table 19: eRD109 SCIPP budget request for FY23 on frontend ASIC R&D. All entries in thousands of dollars.

4.3 Sensor/ASIC Integration

Tab. 12 contains the resource allocation on sensor/ASIC integration R&D.

Resource	Task	FTE (%)	Budget (k$)
Electrical Engineer	interposer design and testing	10	15
External vendor	interposer fabrication and bump-bonding with ASIC	-	30
Total	-	-	**45**

Table 20: UIC budget request for FY23 on sensor/ASIC integration. All entries in thousands of dollars.

4.4 Frontend Electronics (eRD109)

The budget request for the AC-LGAD system frontend electronics R&D described in section 3.3 is given in Table 21.

Inst.	Resource	FTE (%)	Budget (k$)
	Readout and Timing Distribution R&D		
BNL	Research Associate	20	38
BNL	2 Staff Scientists	2x20	0 (in-kind)
BNL	Xilinx Dev. Kit	-	4
BNL	Timing Chips + Boards	-	15
	Barrel Low-Mass Service Hybrid R&D		
ORNL	Electrical Engineer	10	32
ORNL	Staff Scientist	10	0 (in-kind)
ORNL	Materials and Supplies	-	8
ORNL	Xilinx Dev. Kit	-	4
	Endcap Service Hybrid R&D		
Rice	Faculty	10	0 (in-kind)
Rice	Electrical Engineer	15	18
Total			**119**

Table 21: eRD109 Budget request for the TOF system readout electronics R&D in FY23. All entries in thousands of dollars.

4.5 Mechanical Structure

Workforce at NCKU/AS and Purdue on EPIC includes: 3 faculties (20% FTE) + 1 senior scientist (20% FTE), 3 engineers (10% FTE), 1 PhD student (20% FTE from NCKU), 1 undergrad student (100% FTE from NCKU). Tab. 22 contains the breakdown of the budget allocation at the mechanical structure R&D.

Institution	Resource	FTE (%)	Budget (k$)
Purdue	Faculty	20	0 (in-kind)
Purdue	Mechanical engineer	10	15.0
Purdue	Material and Supplies	-	5.0
NCKU/AS	2 Faculties	2×20	0 (in-kind)
NCKU/AS	Senior scientist	20	0 (in-kind)
NCKU/AS	2 Engineers	2×10	0 (in-kind)
NCKU/AS	Graduate Student	20	0 (in-kind)
NCKU/AS	Undergraduate Student	100	0 (in-kind)
NCKU/AS	Production cost	-	5.0
NCKU/AS	Materials and Supplies	-	10.0
Total	-	-	**35.0**

Table 22: NCKU/Purdue/AS budget request on light-weight support structure R&D in FY23. All entries in thousands of dollars.

References

[1] EIC at Brookhaven National Laboratory, Conceptual Design Report, J. Adam *et al.*, http://www.eicug.org/web/sites/default/files/EIC_CDR_Final.pdf; https://www.bnl.gov/eic/

[2] Design and Fabrication of a Highly Integrated Silicon Detector for the STAR Experiment at Brookhaven National Laboratory, B. Buck, *et al.*, arXiv.1404.0993 (2014).

[3] A MIP Timing Detector for the CMS Phase-2 Upgrade: Technical Design Report, CMS collaboration, CERN-LHCC-2019-003/CMS-TDR-020 (2019).

[4] EIC AC LGAD R&D Proposal, https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY22

[5] Quan Sun *et al.*, "The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL", FERMILAB-PUB-21-643-PPD, arXiv.2012.14526 [physics.ins-det], 2020, https://arxiv.org/abs/2012.14526

[6] Apresyan, Artur and Chen, Wei and D'Amen, Gabriele and Di Petrillo, Karri Folan and Giacomini, Gabriele and Heller, Ryan and Lee, Hakseong and Los, Sergey and Moon, C. S. and Tricoli, Alessandro *et al.*,"Measurements of an AC-LGAD strip sensor with a 120 GeV proton beam. Journal of Instrumentation, IOP Publishing, 2020, 15 (09), pp.P09038.

[7] R. Heller and C. Madrid and A. Apresyan and W.K. Brooks and W. Chen and G. D'Amen and G. Giacomini and I. Goya and K. Hara and S. Kita and S. Los and A. Molnar and K. Nakamura and C. Peña and C. San Martín and A. Tricoli and T. Ueda and S. Xie *et al.*,"Characterization of BNL and HPK AC-LGAD sensors with a 120 GeV proton beam. Journal of Instrumentation, IOP Publishing, 2022, 17 (05), pp.P05001.

[8] R. Heller and A. Abreu and A. Apresyan and R. Arcidiacono and N. Cartiglia and K. DiPetrillo and M. Ferrero and M. Hussain and M. Lazarovitz and H. Lee and S. Los and C.S. Moon and C. Peña and F. Siviero and V. Sola and T. Wamorkar and S. Xie,"Combined analysis of HPK 3.1 LGADs using a proton beam, beta source, and probe station towards establishing high volume quality control. Nucl. Instrum. Meth. A, 2021, 1018 (0168-9002), pp.165828.

[9] The ATLAS Collaboration, "A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade", CERN-LHCC-2020-007, ATLAS-TDR-031, CERN (2020). https://cds.cern.ch/record/2719855/files/ATLAS-TDR-031.pdf

[10] C. Agapopoulou, C. de la Taille, L. Serin *et al.*,"Performance of a Front End prototype ASIC for picosecond precision time measurements with LGAD sensors. Journal of Instrumentation, IOP Publishing, 2020, 15 (07), pp.P07007.
https://dx.doi.org/10.1088/1748-0221/15/07/P07007
https://hal.archives-ouvertes.fr/hal-02497834
https://arxiv.org/pdf/2002.06089.pdf

[11] C. Agapopoulou *et al.*, "ALTIROC 1, a 25 ps time resolution ASIC for the ATLAS High Granularity Timing Detector", 2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2020, pp. 1-4, https://ieeexplore.ieee.org/document/9507972

[12] http://www.p2io-labex.fr

[13] P.-K. Wang, "Simulation and instrumentation for the Roman Pot in the future Electron-Ion Collider", EIC User Group Early Career Workshop 2022, July 24-25, CFNS Stony Brook University. https://indico.jlab.org/event/485/contributions/10232/

[14] CMS Collaboration. Technical Proposal for a MIP Timing Detector in the CMS Experiment Phase 2 Upgrade. (2017). CERN-LHCC-2017-027 ; LHCC-P-009
https://cds.cern.ch/record/2296612/files/LHCC-P-009.pdf

[15] D. Thienpont and C. de la Taille for the CMS Collaboration, "Performance study of HGCROC-v2: the front- end electronics for the CMS High Granularity Calorimeter", JINST15 (2020) C04055, 3rd Conference on Calorimetry for the High Energy Frontier, Fukuoka, Japan, 25 - 29 Nov 2019, CMS-CR-2020-014.
https://cds.cern.ch/record/2712269/files/CR2020_014.pdf

[16] K. Kim, Y. Kim, W. Yu and S. Cho, "A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier" in IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 1009-1017, April 2013, doi: 10.1109/JSSC.2013.2237996. https://uma.ac.ir/files/site1/g_zare_3fd00a8/tdc2.pdf

[17] G. D'Amen *et al.*, "Signal formation and sharing in AC-LGADs using the ALTIROC0 front-end chip", Sept. 2022, arXiv:2209.07329 [physics.ins-det], https://doi.org/10.48550/arXiv.2209.07329

[18] NASA - https://www.flickr.com/photos/nasa2explore/49165334137/