FY22 Report and FY23 Proposal on EIC AC-LGAD R&D - Frontend ASIC and Electronics -

eRD112

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Contents

1 Introduction

In March 2021, Brookhaven National Laboratory (BNL) and Thomas Jefferson National Accelerator Facility (JLab) together issued a call for Collaboration Proposals for Detectors at the EIC. Three proto-collaborations (ATHENA, CORE and ECCE) formed and submitted three proposals. All the proposals utilize the AC-coupled Low Gain Avalache Detector (AC-LGAD) technology for Time-of-Flight (TOF) particle identification (PID) and tracking in the central detector, and timing measurement and tracking in the far-forward direction. In March 2022, the EIC Detector Proposal Advisory Panel announced its recommendation to choose the ECCE proposal to be the reference design for the EIC project detector. Since then, a new collaboration (EPIC) has been formed to work on the technical design of the detectors in preparation for the DOE CD2/3A review anticipated in October 2023. Specifications of the AC-LGAD detectors for EPIC are summarized in Tab. 1 and discussed below. Note that the requirements on the timing and spatial resolutions and material budget are still being evaluated and are subject to changes as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

	Area (m^2)	Time resolution	Spatial resolution	Material budget
Barrel Timing Tracking Layer	11	25 ps	30 μm in $r \cdot \phi$	0.01 X_0
Endcap Timing Tracking Layers	1.2+2.2	25 ps	30 μm in x and y	0.08 X_0
B0 Tracker	0.07	30 ps	$500/\sqrt{12}$ μm	0.01 X_0
Roman Pots	0.14	30 ps	$500/\sqrt{12}$ μm	no strict req.
Off-Momentum Detectors	0.08	30 ps	$500/\sqrt{12}$ μm	no strict req.

Table 1: Specifications of AC-LGAD detectors for EPIC, the EIC project detector. The timing and spatial resolutions are given for single hits, while the material budgets are given per detector layer.

1.1 AC-LGAD for the Central Detector

The central EPIC detector includes the following AC-LGAD detectors (see Fig. 1):

- Electron Timing and Tracking Layer (ETTL) with a single layer of pixel sensors at $-171 < z < -161$ cm, with an inner radius of 12 cm and outer radius of 64 cm.
- Central Timing and Tracking Layer (CTTL) with a single layer of strip sensors at $62.5 < R < 65.5$ cm with a total length of 270 cm.
- Forward Timing and Tracking Layer (FTTL) with a single layer of pixel sensors at $155.5 < z < 170.5$ cm, with an inner radius of 12 cm and outer radius of 85 cm.

The layouts of these detectors are shown in Fig. 2. The CTTL follows the STAR Intermediate Silicon Tracker design [1], while the ETTL/FTTL follow the CMS Endcap Timing Layer design [2]. The CTTL consists of 288 tilted staves, each of which is 135 cm long. AC-LGAD strip sensors are mounted on low mass Kapton flexible circuit boards (hybrids), and are wire-bonded with front-end ASICs. The hybrids are glued onto mechanical structures made from low density Carbon-Fiber (CF) materials, and bring power and input/output signals to the sensors and ASICs. The heat generated by the frontend ASICs are removed by an embedded Aluminium cooling tube in the CF structure. The ETTL/FTTL consist of detector modules made from AC-LGAD pixel sensors bump-bonded with front-end ASICs. These detector modules are mounted from both sides onto a thermal-conductive supporting disk with embedded liquid cooling lines. Since the irradiation flux at the EIC is much smaller than that at the LHC, it is assumed that the radiation damage will not be a concern and the AC-LGAD sensors can be operated at room temperature.

With single hit timing resolution of 25 ps, the CTTL and ETTL/FTTL can separate pions and kaons at the 3σ level for $p_T < 1.2$, and $p < 2.5$ GeV/c, respectively. By combining the PID information from the AC-LGAD detectors and Cherenkov detectors, EPIC will have excellent PID capability over a wide momentum range in a nearly 4π acceptance, which is crucial to achieve the goals of the EIC physics program. Besides precise timing resolution, AC-LGAD sensors can also provide precise spatial

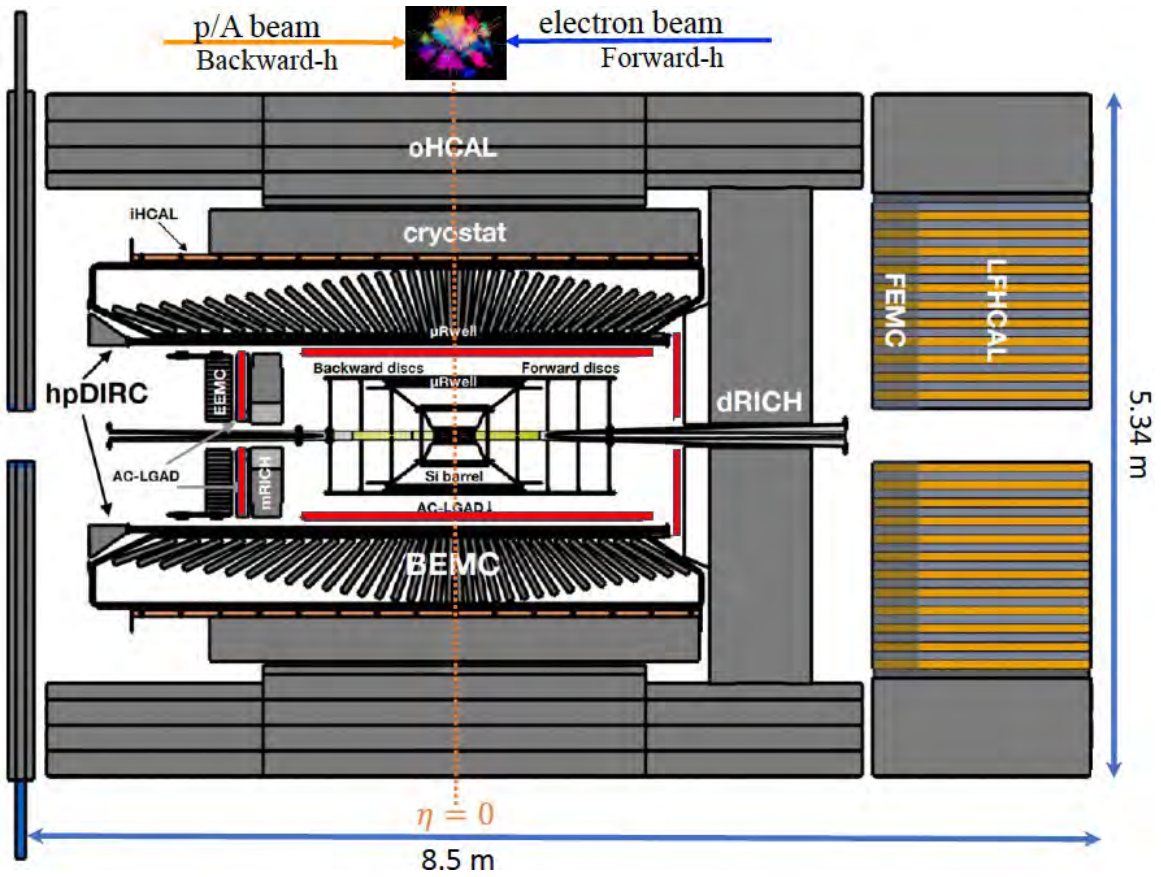

Figure 1: Layout of the central detector of the EPIC detector reference design, which includes a AC-LGAD Timing and Tracking Layer detectors (in red) in the backward, central, and forward directions.

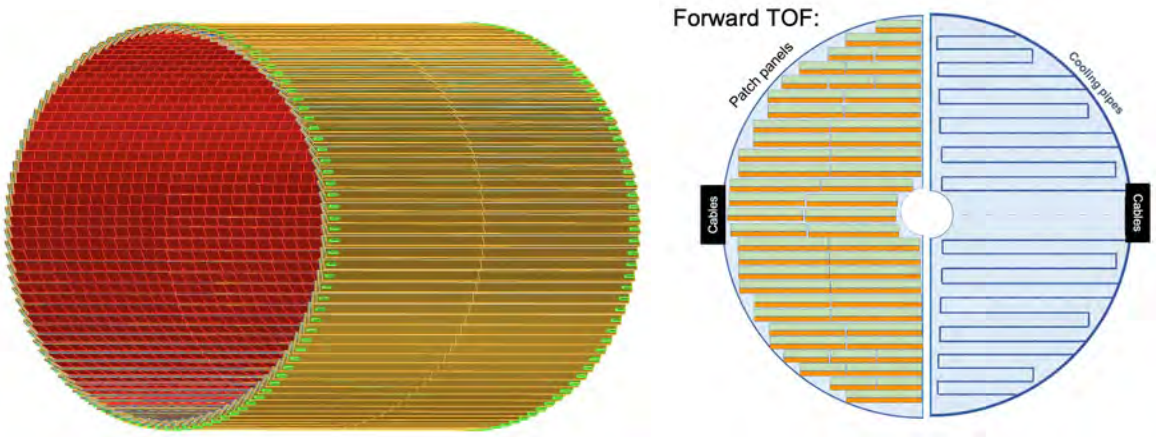

Figure 2: Layout of the EPIC AC-LGAD TTL detectors in the barrel (left) and endcap regions (right).

resolution, and thus aid track reconstruction and momentum determination. The requirements on the timing and spatial resolutions, as well as the material budgets of the TTL detectors are being evaluated in EPIC MC simulation to find the optimal configuration without over-designing these detectors.

1.2 AC-LGAD for Far-Forward Detectors

The EIC physics program includes a strong emphasis on exclusive and diffractive final states, which produce charged and neutral particles at $\eta > 4.5$, outside of the main detector fiducial acceptance. In

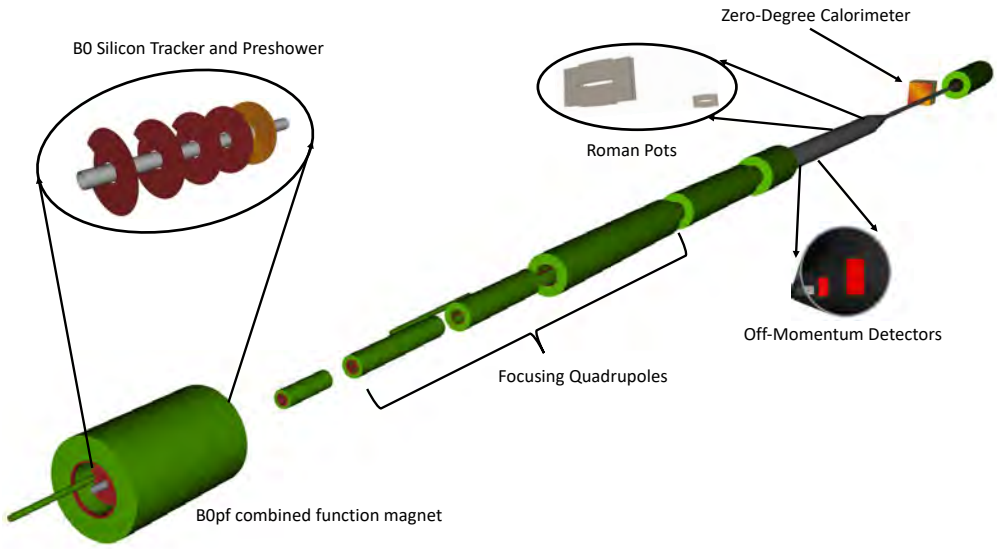

Figure 3: Layout of the EPIC far-forward detector systems, which include a tracking spectrometer and a silicon pre-shower embedded in an accelerator dipole magnet (the so-called "B0 detector"), silicon tracking detectors directly in the machine vacuum (Roman Pots and Off-Momentum Detectors), and a Zero-Degree Calorimeter with both hadronic and electromagentic calorimetry capabilities.

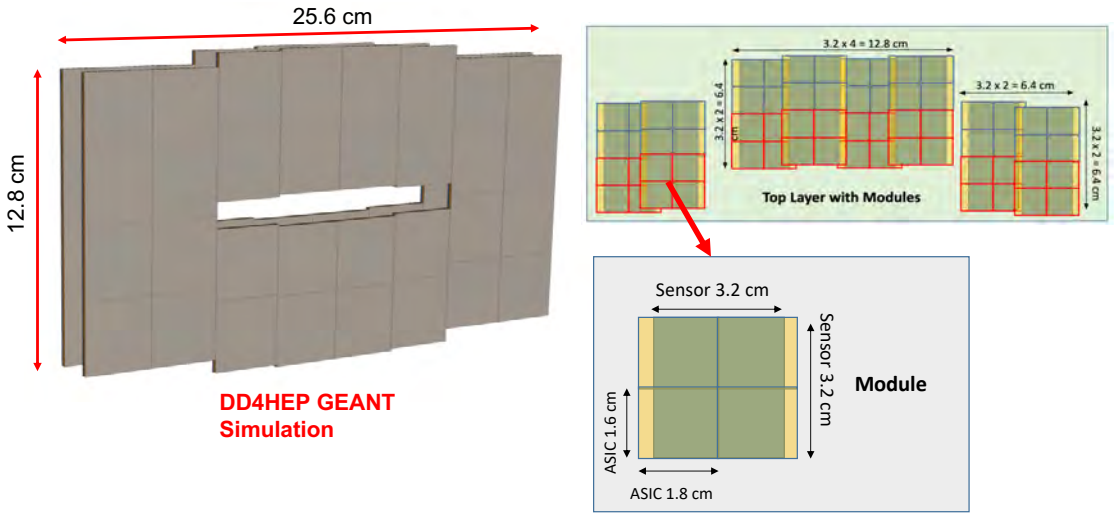

Figure 4: Layout Roman Pots far-forward detector subsystem. The current layout has been implemented in the GEANT4 simulations, and includes the sensor and ASIC package, as well as material estimates for the cooling and shielding layers of the detector.

order to tag and fully reconstruct these "far-forward" final states, a suite of detectors integrated with the hadron beam-line at interaction point (IP) 6 (the project IP) are required. The layout of this suite of far-forward detectors is shown in Fig. 3.

All four far-forward sub-systems require silicon detection components with spatial resolutions between 5 and 145 μm, and timing resolution ~30ps to achieve the required performance to reconstruct charged particle momenta at $\eta > 4.5$. In particular, the timing requirement is important for background rejection from both beam+machine component and beam+gas events, but also for disentangling the transverse momentum kick provided to the bunch particles by the EIC crab cavities. These devices account for the 25mrad crossing angle at IP6 by rotating the bunches via transverse momentum kicks, which vary longitudinally along the bunch, and cause an effective vertex smearing when performing reconstruction of the final-state particles. Given these requirements, AC-LGADs provide the unique

benefit of enabling accurate measurement of spatial and timing information, making them perfect for many applications in the far-forward region. Below, the subsystems for which use of AC-LGAD technology is planned are summarized.

In the case of the B0 Detector, AC-LGADs are planned to be used as a timing layer in the main tracking system, while also providing an additional spatial point for tracks, and perhaps also in the silicon pre-shower detector. The AC-LGAD sensor was also considered for the main technology for the entire subsystem, but it was determined that even with the incredible improvement in spatial resolution provided by signal-sharing in the sensor, the highly demanding specification ($\sim$5-10μm) for the B0 tracking was more-readily met with a different technology.

In the case of both the Roman Pots (RP) and the Off-Momentum Detectors (OMD), the spatial resolution requirements are less-stringent ($\sigma_{x,y} \sim 140\mu m$), enabling use of the AC-LGAD technology as a primary choice for implementation of the detector. This option allows for 4D information to be extracted from a single technology, which enables the Roman Pots and OMD subsystems to be efficiently realized in a very limited space inside the beam vacuum system. The current layout of the Roman Pots sensor and readout ASIC packages are shown in Fig. 4. The RP and OMD subsystems do not have stringent requirements on material budget since the particles being detected are all at energies $>$ 41 GeV (most above 100 GeV), and therefore not greatly affected by multiple scattering. However, in the timing layer of the B0 tracking system, we will need a material budget more-consistent with the forward tracking disks ($< 1\%$).

The size of the sub-systems are based on the spatial extent of the scattered beam particles which are produced from the various EIC beam energy/species configurations. The largest scattered proton envelope occurs for the 5x41 GeV beam energy configuration, and requires the 26cm x 13cm plane size for the Roman Pots detector systems. The Off-Momentum Detectors require smaller planes of 10cm x 20cm. In total, the combined active (sensor) area of the RP and OMD subsystems is $2152cm^2$. Since these detectors are operated close to the beam, and within vacuum, spatial care needs to be taken in cooling and shielding the detectors. Work is underway to better understand these requirements as both the ASIC and machine design matures, but current estimates place the expected detector occupancies at least two orders of magnitude lower than what is seen at the LHC for systems employing DC-LGAD technology for timing measurements.

For all applications in the far-forward area, a pixelated AC-LGAD with a minimum of 500 μm pixels is required, not just for accurate spatial reconstruction, but also for background rejection, and separation of multi-particle final states containing charged spectators with small angular separation (e.g. in the case He-3 breakup with the neutron as the active nucleon). Additionally, using pixelated detectors requires less overall layers in subsystems for the Roman Pots and OMD, which will be very important for engineering solutions required to minimize impedance on the hadron beams from the presence of these detectors in the beam vacuum.

2 FY22 Report

While finalizing the layouts and requirements of the AC-LGAD detectors for EPIC, we have advanced the development of AC-LGAD sensors and frontend readout ASICs in order to meet such requirements. The efforts on ASIC development are described below.

2.1 Frontend Readout ASICs

The far-forward AC-LGAD detectors use pixelated sensors, and the CTTL detector uses strip sensors to have reduced number of channels and power consumption. These require different frontend readout ASICs optimized for pixel sensors and for strip sensors, respectively. In FY22, we have pursued more than one frontend ASIC development effort, including 1) EICROC0 design and submission 2) FCFD0 design, submission and initial testing, and 3) investigation of ASICs developed by third party institutions.

2.1.1 EICROC0 design and submission

While specific ASICs have been designed to readout DC-LGADs of ATLAS HGTD and CMS ETL, namely ALTIROC [8, 9] and ETROC [4], the development of a dedicated ASIC optimized to readout

novel fine pixelated AC-LGAD sensors is mandatory to fully exploit their potential in terms of time and spatial resolutions, taking into account their intrinsic properties (lower capacitance) and the signal sharing (sensitivity to small charges). The goal of the EICROC team is to develop an ASIC with a pitch size of 0.5×0.5 mm^2 to readout AC-LGAD sensors and to characterize the integrated sensor+ASIC detector system in an environment close to the experimental conditions.

The needs for fast timing performance and finer granularity pose significant challenges to the readout electronics and specifically to the ASIC readout chips. Present ASIC chips designed for ATLAS and CMS timing detectors have a jitter on the order of 20–30 ps, and a pixel granularity of 1.3×1.3 mm^2. Reduced granularity and better timing resolution requirement will make it more challenging to fit all the circuit components within the available space, and also likely lead to significantly increased power consumption due to increased total number of channels.

The EICROC project relies on complementary teams with expertise in micro-electronics, instrumentation and semi-conductor detector characterization from French institutes (IJCLab, CEA-Saclay/Irfu/DEDIP and OMEGA) and from Brookhaven National Laboratory (BNL) also involved in the design and the production of AC-LGAD sensors for EIC. In 2022, in close collaboration within the consortium (periodic meetings), the electronics activity was many folds:

- Measurements and data analysis by the BNL team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC0** chip using a Beta source (^{90}Sr) and exploiting an infrared laser test bench,
- Measurements and data analysis by the IJCLab team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC1_v2** chip using a Beta source (^{90}Sr). Based on the BNL IR laser test bench, all equipment have been ordered to set-up an IR laser test bench at IJCLab,
- Relying on simulations developed at IJCLab and OMEGA, an ASIC prototype has been designed involving the CEA-Saclay/Irfu team for the TDC and collaborators from AGH University of Science and Technology (Krakow, Poland) for the 8-bit ADC (Analogical to Digital Converter). The chip design has been submitted for fabrication at the end of March 2022 and EICROC0 chips have been received at the end of July 2022.
- The dedicated printed circuit board (PCB) which holds the EICROC0 and the AC-LGAD sensor has been designed by the OMEGA team, fabricated and 10 pieces were received at the end of July 2022. The PCBs have been cabled at IJCLab. PCBs and EICROC0 chips have been shipped to BNL for the wire-bonding.
- A ZC706 Xilinx board acting as the interface board to control EICROC0 parameters has been provided and the associated firmware has been developed by IJCLab team.

All the FY22 costs have been covered by funds granted by the LabEx P2IO [11] (Université Paris-Saclay, France) for the period 2020-2022 within the call "Projets Emergents" (AC-LGAD Project), French institutions has thus provided in-kind labor and material contributions during 2022. Below we present these works.

Studies based on (HGTD) ALTIROC1_v2 chip (IJCLab):

ALTIROC1_v2 is a 5×5 pixelated ASIC designed by OMEGA in 130 nm node technology for ATLAS HGTD [10]. It holds 2 kinds of Pre-Amplifiers, 15 Voltage Pre-Amplifiers (VPA) and 10 Trans-Impedance Pre-Amplifiers (TZ). Each channel uses two Time Digital Converters (TDCs), one measuring the Time-Of-Arrival and the other the Time-Over-Threshold (TOT) as an estimate of the signal amplitude to correct for time-walk effect. This ASIC which was designed to read out HGTD DC-LGAD sensors with 1.3×1.3 mm^2 pixels is used as a stepping stone to read out AC-LGAD sensors and to constrain the design of a proper ASIC prototype.

After each individual ALTIROC1_v2 channel on the printed circuit board #19 (B19) has been characterized using HGTD test bench at IJCLab to identify best working channels (TOA and TOT), the circuit has been shipped to BNL where 8 channels of a 3×3 pixelated AC-LGAD sensor have been wire-bonded to the ASIC and sent back to IJCLab in July 2021 where a characterization of each connected channel of the system ALTIROC1_v2 + AC-LGAD sensor has been performed.

Figure 5 shows on the left the observed pre-amplifier signal amplitudes from each AC-LGAD connected channels corresponding to an input charge of $\sim$8 fC when the sensor is biased at -160

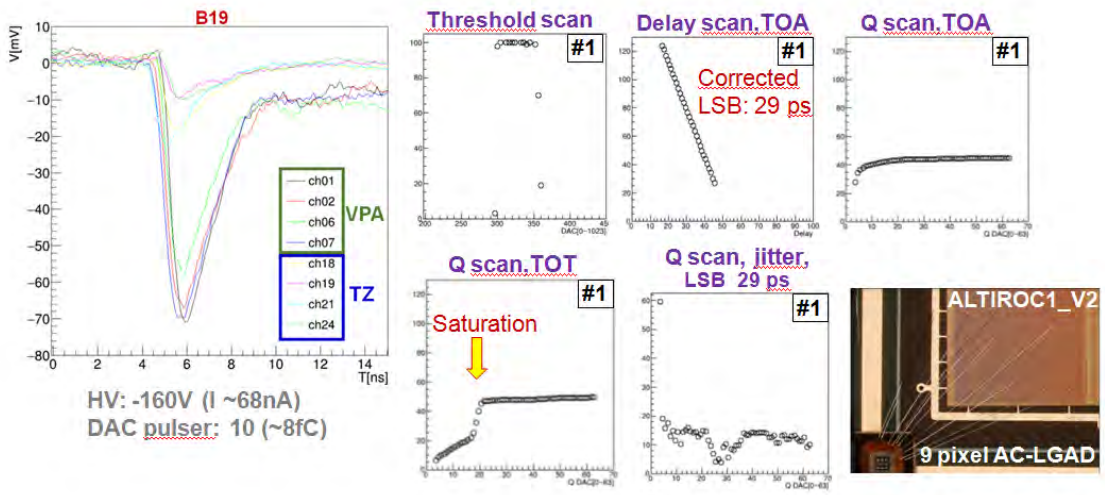

Figure 5: Left: observed ALTIROC1_v2 pre-amplifier signal amplitudes corresponding to a $\sim$ 8 fC input charge for each channel connected to a pixelated 3×3 AC-LGAD sensor biased at -160 V. Right: results from threshold scan, delay scan, and injected charge scan (TOA and TOT). The picture on the bottom right shows a 3×3 AC-LGAD sensor wire-bonded to an ALTIROC1_v2 chip.

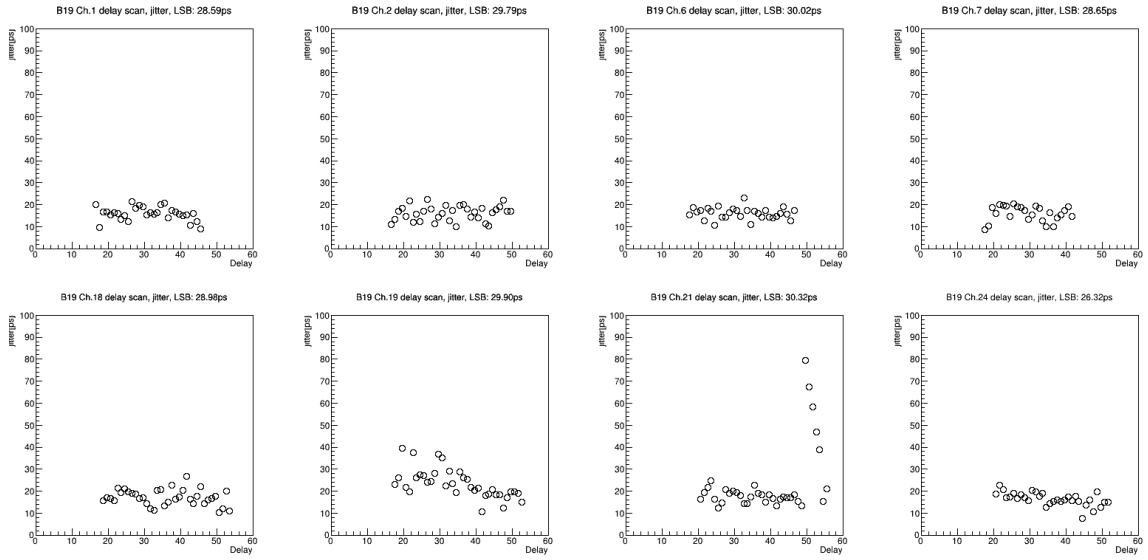

Figure 6: Measured jitter as a function of the delay in arbitrary units for each channel connected to the AC-LGAD sensor.

V. The other plots concern channel 1, as an illustration, and have been obtained after scanning the threshold, the delay (TOA), the charge (TOA and TOT). From the delay scan (TOA), the corrected Least Significant Bit (LSB) is found to be of the order of 30 ps for each connected TDC channel showing a uniformity among all channels (see Fig. 6). For TOT, while scanning the injected charge, an effect looking like a saturation is observed for most channels above an injected charge of 21 fC. After investigation, this "saturation" effect, already mentioned in [9] is due to afterpulses observed on the discriminator falling edge signal.

The threshold of each channel has been measured and the lowest detectable charge being about 2.5 fC makes us confident that the goal of 2 fC for EICROC can be achieved. The average jitter for each channel is of the order of 20 ps for an injected charge higher than 5 fC, which is in agreement with measurements and simulations performed earlier by ATLAS HGTD team, see Fig. 7 and [10].

The charge sharing between pads/pixels has been studied exploiting ALTIROC (self) charge injec-

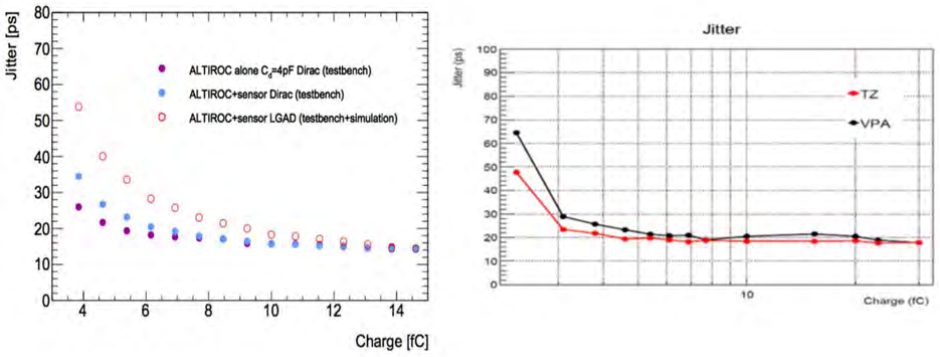

Figure 7: Left: ALTIROC1 measured and simulation-extrapolated total hit jitter for increasing input charges [10]. Right: jitter measured from VPA and TZ pre-amplifier AC-LGAD wire-bonded channels (HV -190 V) as a function of the injected charge.

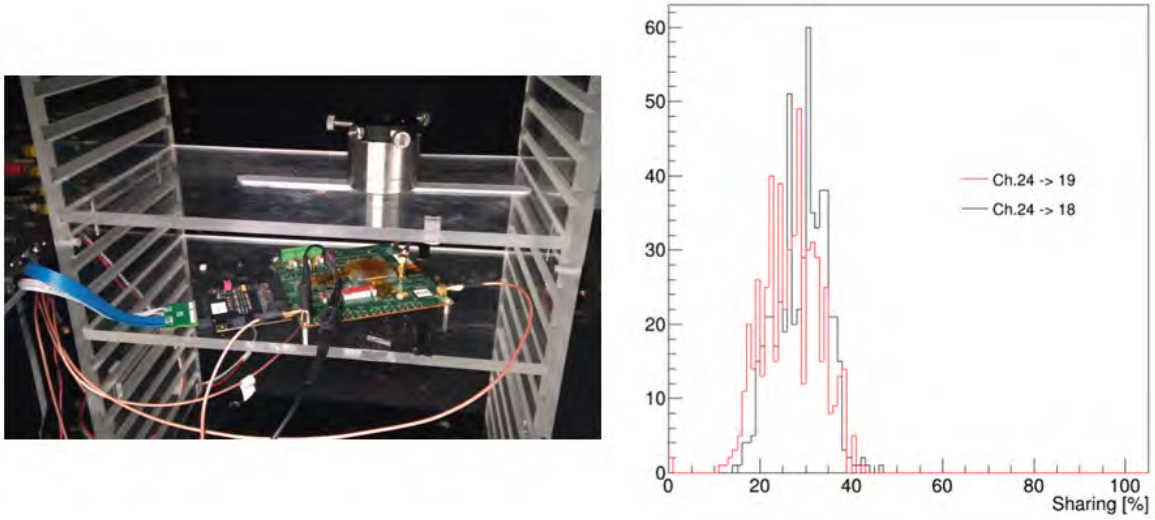

Figure 8: Left: experimental Beta source set-up. Right: amplitude distributions of channels #18 and #19 versus the charge sharing selecting #24 as the highest measured amplitude.

tion, using a beta source (^{90}Sr) and through simulations.

Using the ATLAS HGTD electronic test-bench, a study has consisted in injecting a 8 fC charge in one ALTIROC1_v2 channel and measuring pre-amplifier output signal amplitude in the neighboring pads placing the whole system in a black box. The resulting sharing was found to be of the order of 15% of the injected channel for 2 clusters: one involving VPA channels and one involving TZ channels.

A beta source (^{90}Sr, 37 MBq) has been used to acquire data with the system (ALTIROC1_v2 + 3 × 3 AC-LGAD sensor 8 channels wire-bonded) placed in a black box to screen from light. The experimental set-up is presented on Fig. 8 (left). Considering TZ connected neighboring channels (#18, #19 and #24), AC-LGAD biased at -170 V, the charge sharing was found to be of the order 30% for neighboring channels (#18 and #19) with respect to #24 selected as the highest measured amplitude (see Fig. 8 (right)). This result includes the TOT issue due to afterpulses observed at the falling edge of discriminators signals.

To study the charge sharing among pads, an electronics simulation modeling the charge injection has been developed considering a matrix of 12 pads and TZ pre-amplifiers, as illustrated on Fig. 9 (left). The study consisted of comparing pre-amplifier signal amplitudes obtained at each pad after injecting a 19 fC charge at a distance ratio between pads between 0 and 1 (a ratio of 0.5 meaning

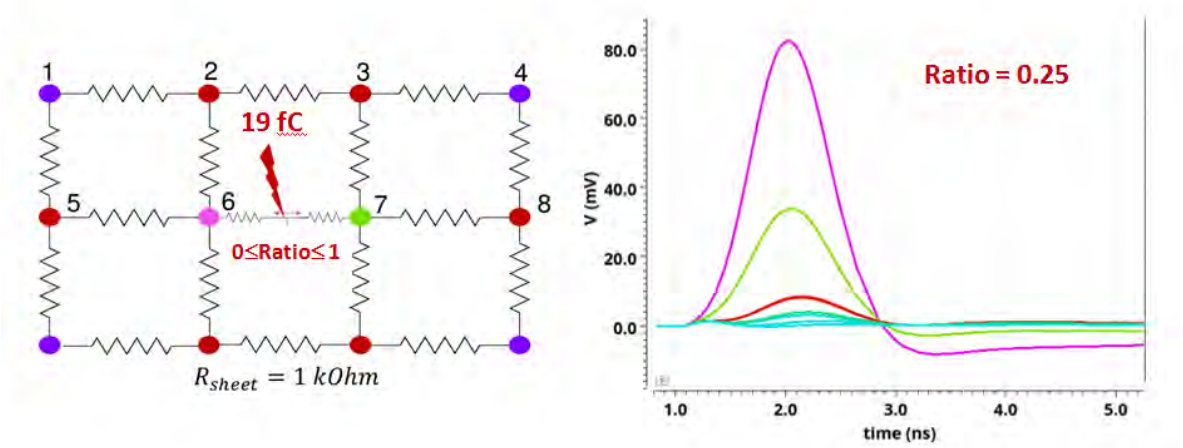

Figure 9: Left: schematic model of 12 pads on which rely the electronics simulation that has been developed to study charge sharing among pads. Right: pre-amplifier signal amplitudes corresponding to each pad according to the pad matrix model for a distance ratio of 0.25 and considering a LGAD sheet resistance (R_{sheet} of 1 kΩ.

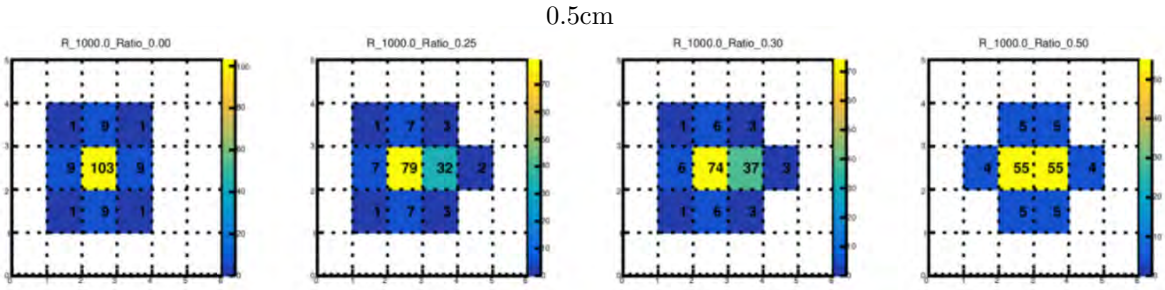

Figure 10: A 2D-representation of pre-amplifier signal amplitudes in mV obtained in each neighboring pad for a distance ratio of 0, 0.25, 0.30 and 0.50 (from left to right) considering a LGAD resistance sheet of 1 kΩ.

that the charge is injected at equal distance between 2 pads, pads #6 and # 7). As an example, the pre-amplifier signal amplitudes corresponding to a distance ratio of 0.25 and considering a LGAD sheet resistance of 1kΩ are presented on Fig. 9 (right). In the simulation different values of LGAD resistance sheet have been taken into account: 0.1, 1, 2.5, 5 and 10 kΩ. The optimization of the sheet resistance layer is a trade-off between the best time resolution in the central pixel (requiring the largest amplitude, thus a large sheet resistance value) and the position measurement (requiring enough amplitude sharing in the neighbours, thus a small sheet resistance value). A few kΩ will satisfy both requirements.

The results of this electronics simulation have been exploited as inputs of another simulation which provides a 2D representation of the results obtained by the electronics simulation which is shown in Fig. 10 for distance ratios of 0, 0.25, 0.30 and 0.50 and a 1 kΩ AC-LGAD sheet resistance. In the context of the design of a specific ASIC prototype to readout AC-LGAD, due to the need of a threshold for precise position determination and the strongly nonlinear behaviour of the TOT, the goal of this simulation was to determine the position resolution which could be achieved relying on the barycenter method as a function of the dynamic range of the ADC to be used to measure the amplitude. This second simulation including the Landau(1,0.3)-distributed (smearing) deposition and a 1 mV gaussian noise has shown that a 8-bit ADC was sufficient to achieved a position resolution < 50 μm. On Fig. 11, one can see that 8 and 10-bit ADC are leading to an equivalent position resolution of the order of 4% (RMS) of the pixel size which corresponds to 20 μm when considering a 500 μm pixel size.

These studies have been presented at the 2022 EIC User Group Early Carreer [12] and allowed us to develop analysis tools which will be exploited in the next step consisting of the characterization of

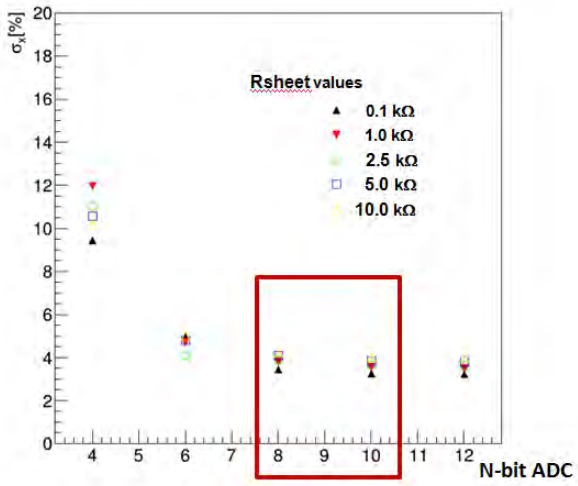

Figure 11: Position resolution in % of the pixel size as a function of the ADC dynamic range for several AC-LGAD sheet resistance.

the system (EIROC0 + AC-LGAD sensor).

EICROC0 Design

Based on the expertise in mircro-electronics of OMEGA (responsible for the design of HGCROC [13, 14] readout chip for the CMS High Granularity Calorimeter and the ATLAS ALTIROC ASIC) and from CEA/Irfu/DEPIP (responsible for the design of the TDC of HGCROC), the goal is to design a novel ASIC in 130 nm CMOS technology, EICROC, with a pitch size of 0.5×0.5 mm^2 that meets the requirements set by EIC providing a precise time measurement with a TDC combined with an Analog Digital Converter (ADC) for the amplitude measurement based on the simulations undertaken at OMEGA and IJClab.

For the EICROC ASIC associated to the EIC Roman Pots detector, due its location (in vacuum) and its proximity to the beam (limited space), one challenge is to reduce the power per channel to a fraction of mW, while ensuring GHz bandwidth, ultra-low noise ($<$ 1mV) for the front–end, picosecond accuracy in the TDCs and good signal-to-noise ratio at the ADC level. Most common architectures dissipate only when the TDC is converting but the large currents drawn during conversion limit drastically the number of TDCs that can be placed on a chip and the voltage drop for large ASIC. In addition, fitting the current electronic blocks, such as the HGCROC-like TDC, in a smaller pixel area represents a second challenge while maintaining their performance. Therefore, the development of a pixel-like ASIC with a few picoseconds timing accuracy represents a technological challenge and requires several iterations that have to be characterized. Table 2 summarizes the specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities as well as the EICROC0, the first EICROC iteration, that has been designed and delivered in July 2022.

EICROC0 is a 4×4 pixelated prototype ASIC with a pitch size of 0.5×0.5 mm^2 based on ALTIROC front-end (TZ pre-amplifiers) and HGCROC ADC/TDC. Collaborators from AGH University of Science and Technology (Krakow) who designed the HGCROC 10-bit ADC provided an 8-bit version of the ADC for EICROC0. The purpose of EICROC0 is to evaluate the readout of AC-LGAD sensors with a dedicated ASIC. The schematic and the design corresponding to one EICROC0 pixel are represented on Fig. 12 and 13. The main components in a EICROC0 channel are:

- TZ Pre-amplifiers and discriminators taken from ALTIROC,
- I2C slow control taken from HGCROC,
- TOA TDC adapted by CEA/Irfu from HGCROC to EICROC0,
- ADC taken from HGCROC adapted to 8-bits by AGH Krakow,

	HGCROC	ALTIROC/ETROC	EICROC0
Sensor type	Si	LGAD	AC-LGAD
Pixel size [mm^2]	5 × 5	1.3 × 1.3	0.5 × 0.5
Pixel thickness [μm]	100-300	50	50
Pixel capacitance [pF]	50	4	0.5
MIP equivalent charge [fC]	4	5-20	10
Power per channel [mW]	20	5	1
TDC Least Significant Bit (LSB) [ps]	20	20	12
Threshold [fC]	12	4	2
Band width [MHz]	200	800	800
TDC (Time-Over-Threshold)		8 bits/10 bits	
ADC	10 bits@40 MHz		8 bits@40 MHz

Table 2: Comparison of specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities. ALTIROC and ETROC are similar but in different technologies: 130 nm CMOS for ALTIROC and 65 nm CMOS for ETROC.

- digital readout: FIFO depth 8 (200 ns),
- 5 slow control bytes per pixel:
  - 6 bits local threshold,
  - 6 bits ADC pedestal,
  - 16 TDC calibration bits,
  - several on/off and probes

The TDC developed by CEA/Irfu/DEDIP and included in HGCROC has been fully characterized. It used an architecture inspired by [15], based on time residual amplification but with extended dynamic range and improved robustness against PVT (Process, Voltage, Temperature) variations. Its orientation for low power consumption is also a key point in a pixelated environment. Indeed, the power consumption of this TDC is only present during the conversion of an event. Therefore, the consumption of this part is directly proportional to the rate of events arriving on the pixels. This multichannel architecture is presented in Fig. 14. The TDC is driven by a 160 MHz clock (CLK). This clock sequences an 8-bit Gray counter which outputs are broadcasted to all the channels. When a hit occurs on a channel, the counter output is captured on an 8-bit register. To refine the measurement, a coarse TDC (CTDC) based on a 32- step Delay Line (CDL) provides 5 more bits. To extract the less significant bits, the time residue between the hit and the next step of the CDL is multiplied by 8 (optionally by 16) by a time amplifier (TA) before being coded by a fine DL (FDL) over 3 (optionally 4) bits. Then, a digital block decodes and combines the data from the counter, the CDL and the FDL to form the TDC data coded in the nominal TOA mode of operation and 10 bits are kept. In order to keep these performances stable in time and with the environment, a common block (called MASTER DLL) is used which allows to make a permanent calibration on all the TDC channels. There is therefore no dead time relative to the calibration. In addition, a fine calibration system per channel is added. Even if the common calibration is essential, a fine calibration is necessary to compensate for the mismatch effects of the channels. This calibration is currently included in the chip and is adjustable by channel. As an illustration of the performance of this TDC, Fig. 15 shows that the Integral Non Linearity (INL) is close to ± 2 LSB (Least Significant Bit) and the LSB is as low as 13 ps. Such a performance fulfills EIC requirements. This existing TDC (1 mm × 120 μm) needed to be adapted in terms of dynamic range and resolution as well as spatially optimized to fit within a pad of 500 × 500 μm^2. On the other hand, the trigger-less architecture of EIC allows some simplification of the digital part of the ASIC compared to ALTIROC, giving a larger available area for the TDC. To achieve an excellent time resolution, any coupling between the sensor input and the digital electronics activity in the ASIC or the bias voltage connection (inductance) needed to be carefully controlled, which implied constraints on the module design.

The printed circuit board (testboard) associated to EICROC0 has been designed by OMEGA, was received and cabled at IJCLab in July 2022. Main components are level translators (1.2V and 2.5V),

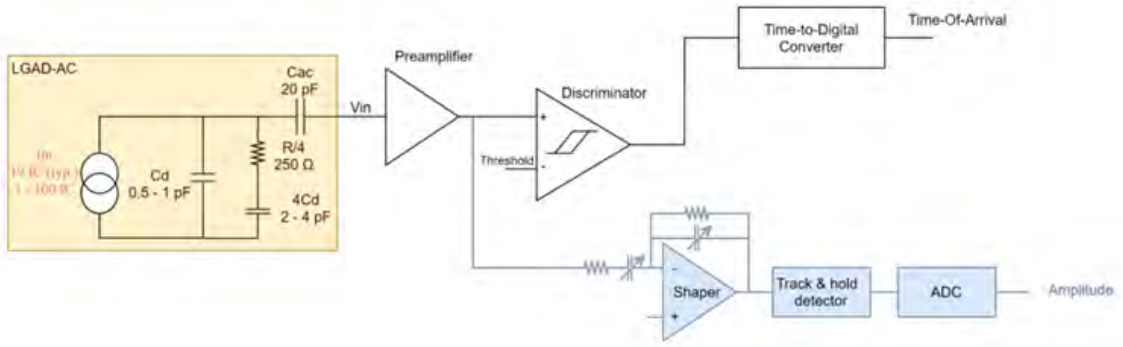

Figure 12: Schematic architecture of one channel of the EICROC0 ASIC prototype dedicated to the readout of an AC-LGAD sensor. A TDC is used to measure the time of arrival (TOA) of the charge and an 8-bit ADC measures the amplitude of the charge filtered by a shaper step.

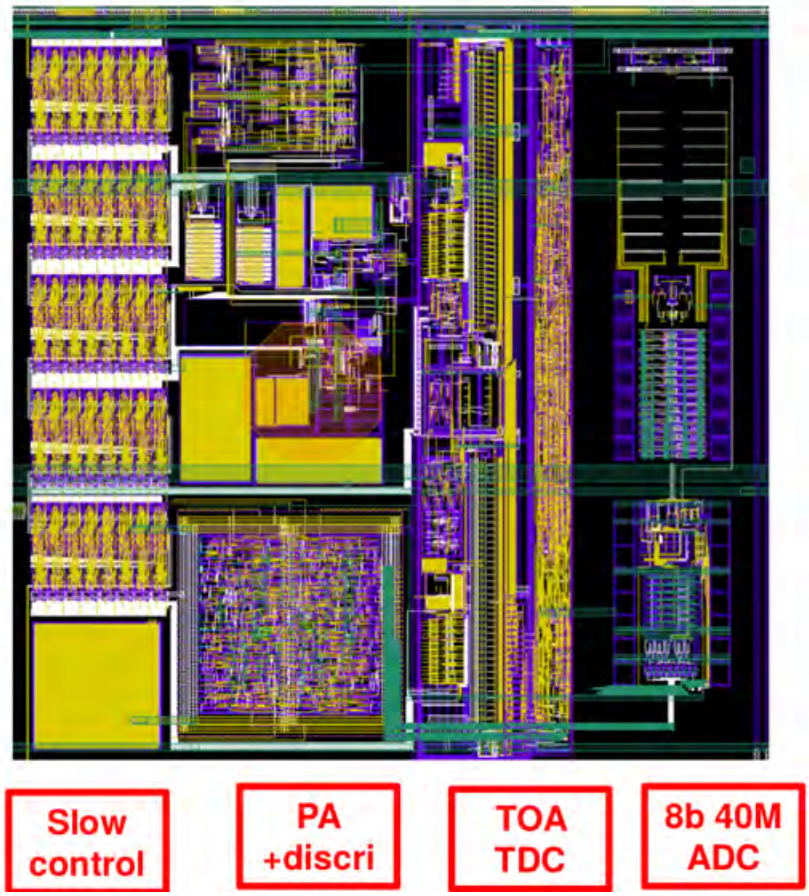

Figure 13: Design of one channel of the EICROC0 chip.

on-board regulators for low voltage, 4 SMA connectors for pre-amplifier signal output. Space have been left near the chip location to accomodate for AC-LGAD sensor wire-bonding. Pictures of an EICROCO chip placed on the bare printed circuit board are shown on Fig. 16.

As a first step, in September 2022, an EICROC0 has been wire-bonded by BNL. PCBs holding an EICROC0 are available at BNL and IJCLab. In order to control the parameters of the system, a Xilinx ZC706 (interface board) was purchased and the dedicated firmware has been developed at IJCLab.

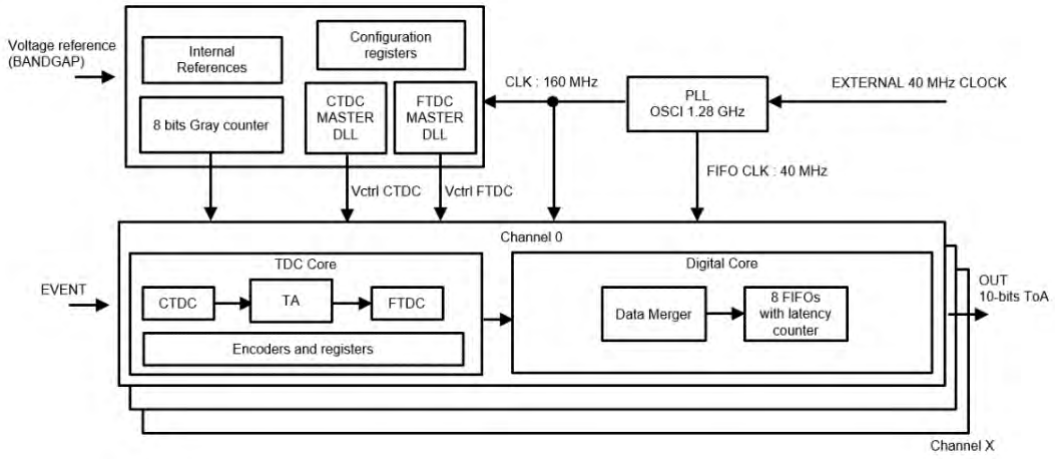

Figure 14: Block-diagram of the improved 3-steps multi-channel TDC.

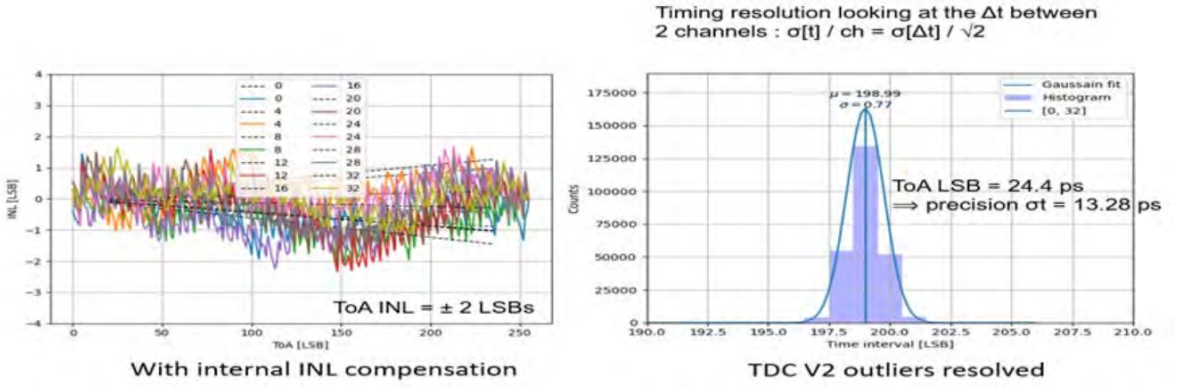

Figure 15: TOA channel INLs with internal compensation (left) and timing resolution histogram by difference between two channels (right). An individual temporal precision of 13 ps is extracted.

The connection between the interface board and the test board is made through a FMC connector. A picture representing a bare printed circuit board connected to the Xilinx ZC706 is shown on Fig. 17.

2.1.2 FCFDv0 design, submission and initial testing by FNAL

Design of the front-end electronics capable to extract precision timing information from LGAD sensors presents many challenges but plays a key role in the applications of the LGAD technology. The Fermilab and UIC team has been studying optimal methods for extraction of timing information from LGADs, using either Leading Edge (LE) or Constant Fraction Discriminator (CFD). Timestamping using the LE requires time-of-walk correction for optimal time resolution of the reconstructed signal, due to the dependance of the threshold-crossing on the signal amplitude. The CFD discriminant does not require such a correction and is therefore much simpler to operate and implement in large systems, without a need to derive and monitor signal dependence as the detector ages. Additionally, our studies in [5] showed that CFD outperforms LE for smaller signals, making it a preferred choice for AC-LGAD sensors which have smaller signals in non-primary channels due to signal sharing.

Following the studies presented in [5] the Fermilab team designed and produced the single-channel version an ASIC based on the CFD concept using TSMC 65nm technology (Fermilab CFD version 0, or FCFDv0). The FCFDv0 uses several new techniques to achieve low power, area, jitter, time walk. This enables a simple and robust timing measurement (30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required. The FCFDv0 is a single-channel ASIC that only contains analog blocks, i.e. the amplifier and discriminator.

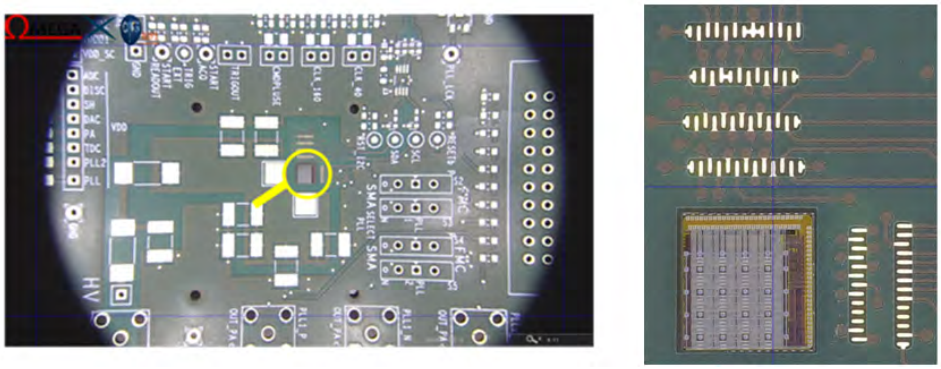

Figure 16: Pictures of an EICROC0 placed at its location on the bare printed circuit board. The picture on the right represents a zoom on EICROC0.

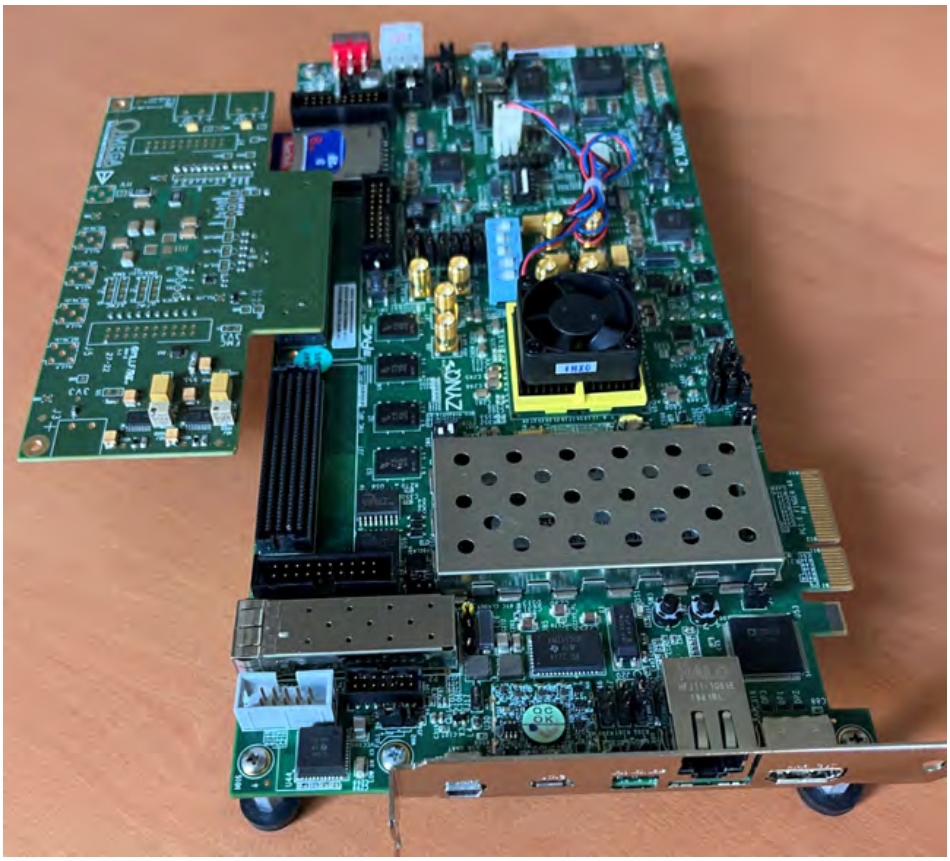

Figure 17: Picture of a bare printed circuit board connected trough FMC connector to a Xilinx ZC706.

Another critical feature in the design and implementation of the ASIC was complete testability with simple bench-top equipment, to properly characterize and adjust the settings on the chip for optimal operation.

The FCFDv0 forms both an attenuated and a delayed version of the amplified input pulse. The input stage is an integrator with a feedback capacitor and a parallel feedback resistor to provide "slow" continuous reset. The attenuated signal is derived very efficiently by splitting the integration capacitance into two series capacitors and buffering the midpoint node. The delayed signal is formed by a programmable RC delay on the integrator output, followed by a buffer. These two buffered signals then directly feed a fast differential amplifier. The single-ended output of the differential amplifier

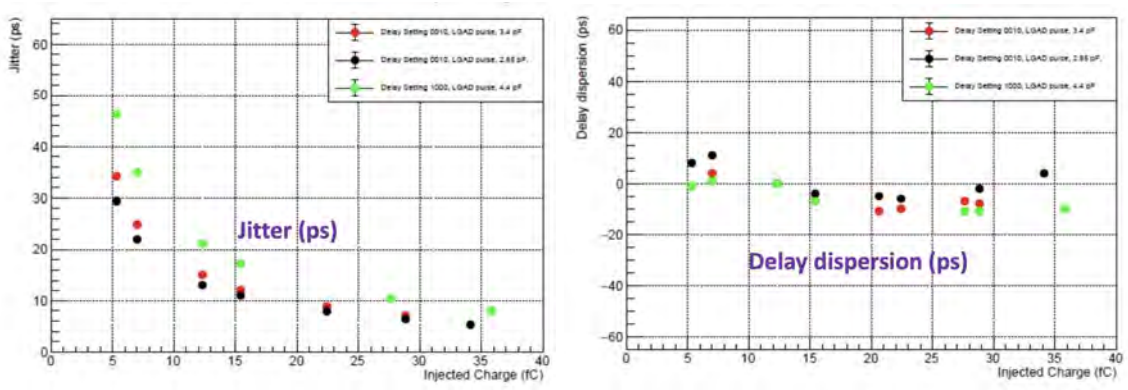

Figure 18: Measured delay jitter (left) and delay dispersion (right) vs. input charge. Red, black, and green points correspond to 3.4, 2.85 and 4.4 pF respectively.

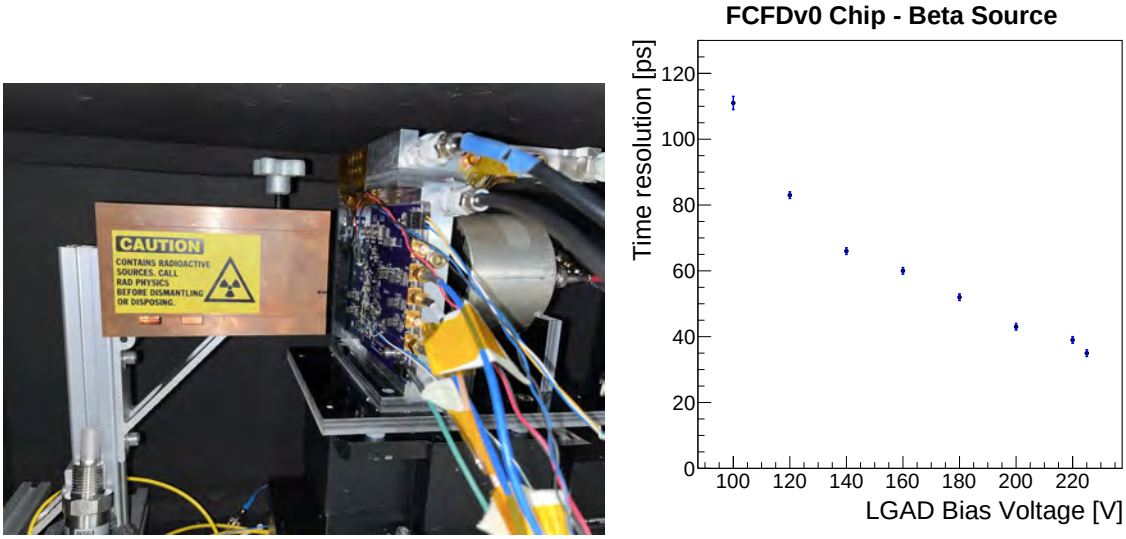

Figure 19: The setup to measure performance of the FCFDv0 with the beta-source (left), and the time resolution vs bias voltage measured using the beta source (right).

feeds a very simple output comparator that compares it to an internal DC threshold voltage. The biasing of the integrator and differential amplifier chain is critical to achieving the best performance and eliminating the need for any trimming. The integrator capacitor midpoint must have a DC bias established, and the differential amplifier has a significant random input offset. A servo loop is used to establish the differential amplifier output voltage by sensing and filtering it and comparing it to an on-chip DC level setting. The capacitor midpoint is then driven appropriately to establish the desired DC output level of the differential amplifier. In a classical CFD, the output comparator would have its threshold set to the quiescent value of the differential amplifier output. However, large signals have more comparator overdrive than small signals, and thus smaller delays. To compensate for this effect, the differential amplifier output is biased at a critical level away from the comparator threshold.

The FCFDv0 chip has been characterized using internal charge injection circuit [6], and recently using an infrared (IR) laser at SiDet. The performance of the FCFDv0 chip was initially tested using the internal charge injection circuit. The LGAD-like pulse corresponding to a 50 μm thick DC-LGAD with 1.3x1.3 mm^2 pixels (C_{in}=3.4 pF) was injected into the circuit to emulate the realistic signals, and signal size was varied from 2.4 to 25.8 fC. The input transistor current was varied from 520 to 820 μA to study the dependence on the gain of the amplifier. Results are shown in Fig. 18 and demonstrate that the chip can measure the ToA down to about 8 ps with simulated signals. We also studied the delay of

signals of various signals, to evaluate whether any residual time-walk correction is still necessary and observe negligible dispersion of the ToA of signals of different sizes, therefore demonstrating no need for time-walk correction.

As a next step we moved to characterize the performance of the FCFDv0 chip using signals from DC-LGAD sensors. A specialized readout board was designed by the Fermilab team for the measurements with source, shown in Fig. 19. For this test, sensors of 1.3×1.3 mm^2 are used. Sensors mounted on the readout board were placed inside an environmental chamber, and the beta source directed at the channel connected to the input of the FCFDv0. The output of the comparator was sent to one of the channels of the Lecroy Waverunner 8208HD oscilloscope, and trigger was generated by the Photek MCP-PMT behind the LGAD sensor. The difference between the time of arrival of two signals was then histogrammed, and the width of the distribution is extracted to evaluate time resolution of the LGAD+FCFDv0 system. The resulting dependence on the bias voltage applied to the LGAD is shown in Fig. 19, demonstrating that we achieve around 30 ps time resolution in a system containing real signals from LGADs, consistent with expectations for this LGAD sensor [7].

2.1.3 ASICs from third party institutions by SCIPP

The development work of LGAD sensors is currently based on high-speed readout boards with discrete components introduced by SCIPP and FNAL. This allowed the crucial characteristics of LGAD signals to be mapped out, however for EIC integrated ASIC has to be developed to allow for high density readout while maintaining a low power dissipation. The readout has to be suitable to the chosen sensor thickness, in Tab. 3 the signal proprieties of 50 μm and 20 μm LGADs are presented with the respective requirements for the ASIC.

LGAD characteristic	50 μm	20 μm
Rise time (10-90%) [ps]	455	182
Input charge [fC]	11	4.6
ASIC characteristic	**50 μm**	**20 μm**
Jitter [ps]	10	5
S/N	>50	>40
Voltage signal [mV]	70	70
Noise RMS [mV]	1.4	1.8
Internal sensor gain	20	20

Table 3: LGAD and ASIC characteristics for 50 μm and 20 μm LGAD sensor thicknesses.

In the area of ASIC development, in FY22 the SCIPP at UC Santa Cruz contributed by collaborating with third party institutions and companies to characterize and fabricate ASICs suitable for the readout of AC-LGADs at EIC. SCIPP role is to guide the chip development, develop of electronic board for chip characterization and testing the chip performance with calibration input and with an LGAD sensor with laser and Sr90 source. The three projects that SCIPP followed in the past year follows. A summary table of the ongoing efforts is in Tab. 4.

- FAST2, developed by INFN Torino: Longer shaping time ($\geq$ 800 ps) not optimized for thin sensors (200–500ps signal rise). Power draw: 1 mW/channel for analog, 1 mW/channel for discriminator/TDC. New design (FAST3) ready soon.
- ASROC: Uses fast SiGeprocess for front end. Promising design but prototype not yet in hand. Front-end power draw good ($\leq$1 mW) but not clear it can be mated to low-power CMOS for back-end. Future funding sources unclear
- HP-SoC: Full, highly flexible "system on chip" (SoC). Both front and back end carefully optimized for timing precision. Integrated 65 nm process promises low power for full readout chain. Ongoing project with DOE recognition and support. Prospective performance characteristic on following page. Power draw: 1.6 mW/chfor analog, 1 mW/ch for digitizer and 1 mW/ch for digital (current goal, still under development).

ASIC results have been reported during eRD112 meetings. In Fig. 20 (left) a photo of the HP-SoC chip mounted on the readout board developed at SCIPP can be seen, in Fig. 20 (right) the output

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

Table 4: Characteristics of ASICs followed by SCIPP.

pulse of the analog amplifier of HP-SoC using a 50 μm thick LGAD prototype from FBK. The pulse shows a very fast rise time of about 500 ps.

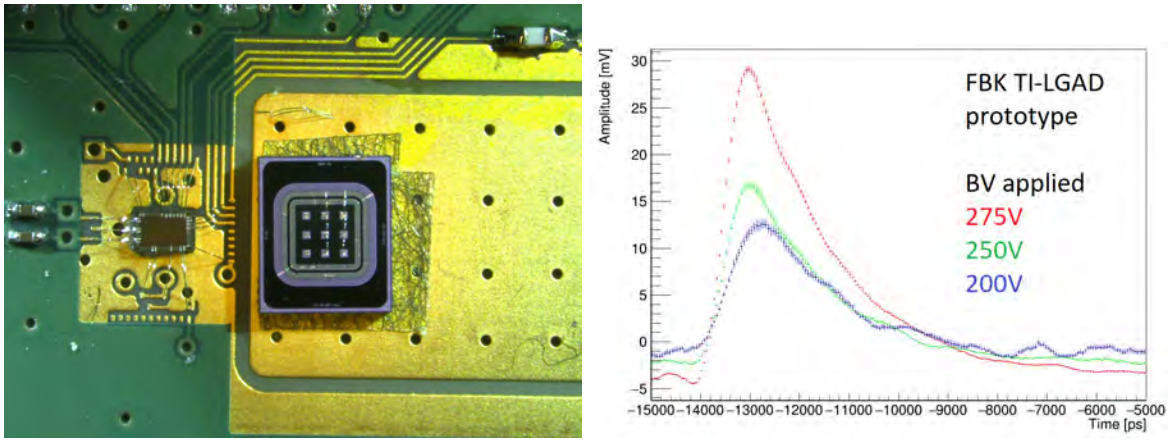

Figure 20: Left: HPSoC prototype by NALU Scientific (left) mounted on the test board developed at SCIPP and wire bonded to an FBK AC-LGAD (right). Right: Measured averaged pulses with HPSoC using an FBK TI-LGAD test sensor, biased at different voltages and irradiated with a Sr90 beta source.

3 FY23 Plan

In FY23, we will continue our efforts in frontend readout ASIC development, and start working on frontend electronics. Below we describe our plans in these areas.

3.1 Frontend Readout ASIC

In FY23, we propose to continue the frontend ASIC development work in 1) EICROC 2) FCFD 3) ASICs from third party institutions. The detailed plan is summarized below.

3.1.1 EICROC1 design and characterization

The work planned in 2023 is organized into 2 workpackages:

- WP1: "Micro-electronics design" coordinated by Christophe de la Taille (OMEGA) involving CEA/Irfu/DEDIP, IJCLab and BNL.
- WP2: "Performance characterization" coodinated by Dominique Marchand (IJCLab) involving OMEGA, CEA/Irfu/DEDIP and BNL.

The EICROC timeline and project organization are displayed in Fig. 21.

Micro-electronics design (WP1)

WP1 is organized in 2 main tasks related to the design and the production of

- (Task 1.1) a small size 8× 4 (or 16×4 pads) ASIC prototype including a lower power ADC and adapted to EIC 100 MHz clock (**EICROC1**, Milestone 1.1, 3rd quarter of 2023),
- (Task 1.2) a full size 32×16 (or 32×32) ASIC (**EICROC2**, Milestone 1.2, mid 2025) to readout large area of AC-LGAD sensors.

The tasks associated to EICROC1 and EICROC2 are similarly organized in subtasks associated to all the stages mandatory to design, produce and test an ASIC, which include the design of each ASIC components (front-end electronics, TDC, ADC), the overall ASIC design layout and documentation, as well as the design of the dedicated electronics test benches.

OMEGA will be responsible for the overall design of the ASICs and the design of the front-end electronics (pre-amplifier and discriminator). In that context, OMEGA designers will closely collaborate with the CEA/Irfu/DEDIP team in charge of the design of the TDC and the IJClab electronics department, which is in charge of the design of the lower power ADC. The development of the test bench (specific boards for the ASIC, read-out boards and firmware) will be shared between OMEGA and IJCLab.

Task 1.1 which is the object of the FY23 budget request consists in the design, production and test of a small size prototype 8 (or 16) × 4 channels, called EICROC1, to study floorplanning.

Relying on the feedback of the measurements which will be performed with EICROC0, the goal of this prototype is to further optimize the very front-end and to include a lower power ADC and TDC fulfilling the 1 mW/channel EIC requirement.

The benefit of an ADC to measure the signal amplitude was explained in section 2.1.1. It is needed to correct for the time-walk for the timing measurement and to get a precise position with a barycenter technique.The free-running ADC adapted from a version developed by the AGH Krakow group which is implemented in EICROC0 is expected to work continuously and thus will be too much power-hungry.

The speed of 20-40 MHz and a resolution of 8 bits are not extreme, but it should be achieved with a lower power than the current state of the art (mW). In particular, the power budget should include the driving stage (shaper, buffer), which usually consumes several times more than the ADC itself. The study of a lower power ADC design has begun at IJCLab in close collaboration with OMEGA.

Task 1.1 is divided into 4 subtasks in order to explore several possible architectures for the sub blocks, probably including variants in columns to evaluate low-power front-end and digitization with a target of 1 mW power consumption per channel. The clock of 40 MHz will be also adapted to EIC (100 MHz input). Requirements serving EIC Roman Pots and ToF will be taken into account. The submission of EICROC1 design is scheduled for 3rd quarter of 2023 (Milestone 1.1).

Task 1.2 which will start in 2024 will be devoted to the design of a full size prototype of 32 $\times$ 16 (or 32) channels, EICROC2. Based on the tests of smaller arrays chips, a preferred architecture will be selected and extended to a full size matrix. At this stage, a whole column (32 pixels) needs to be implemented to investigate the power supplies and ground distributions along it and the possible voltage drops. In addition, a realistic implementation of all the digital blocks and clocks is mandatory as this is often a significant source of noise in detector systems. This task will therefore move more to digital design and integration. The tasks 1.2.1, 1.2.2 and 1.2.3 will implement corrections with respect to the corresponding tasks in 1.1 while more emphasis will be given to the task 1.2.4 regarding integration, simulation and validation steps. ASIC printed boards and interface boards will be re-designed according to the EIROC2 input/output signals in the task 1.2.5.

Characterization and performance measurements (WP2)

The ultimate goal being the demonstration that large size AC-LGAD sensors can be read by an ASIC and meet the EIC specifications, each component (sensor, ASIC) will be first characterized in a stand-alone mode to assess its intrinsic performance. In a second step, assembled devices (through wire bonding and bump bonding) will be tested to check any integration issue and finally be validated in realistic conditions with particles.

At IJCLab, in 2021 and 2022, relying on the ATLAS HGTD test-bench, characterization of ALTIROC1_v2 chip wire-bonded with a 3×3 pixelated AC-LGAD have been performed and measurements have been made using a ^{90}Sr beta source. The next stage is to expose this system to an infrared pulsed laser light (1056 nm) in order to study the charge sharing between neighboring pixels benefiting from a precise location of the light injection. This laser test-bench is inspired from the one exploited by BNL for measurements with the ALTIROC0 chip [16]. All equiments required to set-up the laser test-bench have been received. The commissioning of the test-bench is expected to start shortly and the measurements will follow. This laser test-bench will be also used for characterizing systems with each version of EICROC ASIC coupled with AC-LGAD sensors.

In parallel, since October 2022, the characterization of EICROC0 (Task 2.1) has begun with the commissioning of the EICROC0 test-bench. Then, the "channel by channel" electronics characterization of the chip wire-bonded on the PCB will be performed.

Tasks 2.1, 2.2 and 2.3 are associated to each iteration of the future EICROC, EICOC1 and EICROC2, and are subdivized in same subtasks:

Subtask #.1.1 consists in the stand-alone validation of the ASIC channels. The ASIC will be wire-bonded (or bump bonded) on a dedicated printed circuit and its characteristics, "channel by channel", will be studied using a calibration charge injection and an internal capacitance mimicking the sensor one. The main steps are the determination of the lowest threshold of the discriminator, the noise measurement and efficiency as a function of the charge. The TDC quantization steps will be measured by shifting the input calibration signal with a precise delay and the jitter extracted as a function of the charge. By injecting different charge input, the ADC quantification step and the ADC non- linearity will be extracted. The signal-over-noise at the output of the ADC is also a key measurement.

Subtask #.1.2 consists in reproducing the measurements done in subtask #.1.1 with a sensor connected at the input of the ASIC through wire bonding and bump bonding. The sensor voltage will also be supplied in order to deplete the sensor. This characterization of the system is a cornerstone step before starting to look at real energy deposits in the sensor as quite often integration issues/coupling are observed at this level and require a lot of time to be understood/solved. This subtask is a joint activity between IJCLab and BNL in close collaboration with OMEGA and CEA/Irfu/DEDIP.

Subtask #.1.3 consists finally in characterizing the module with realistic energy deposits. The module will be tested with particles, first with a radioactive beta (^{90}Sr) and it will be exposed to an IR laser light. Charge sharing and time resolution can be studied at this step. Eventually the module will be tested with hadron beam particles in a setup equipped with a precise beam telescope to fully assess the position and time resolution performance. Depending on the availability of the infrastructure, the beam test facility at FNAL (Chicago) with 120 GeV protons or at CERN-SPS with charged pions will be used. As teams from IJCLab and BNL are regular users of these beam lines for other projects, there will be no cost for testbeam.

Progress reports will be made at periodic meetings within the team and within the consortium. The resulting performances will be the object of presentations and publications (Deliverables D 2.1 and D 2.2).

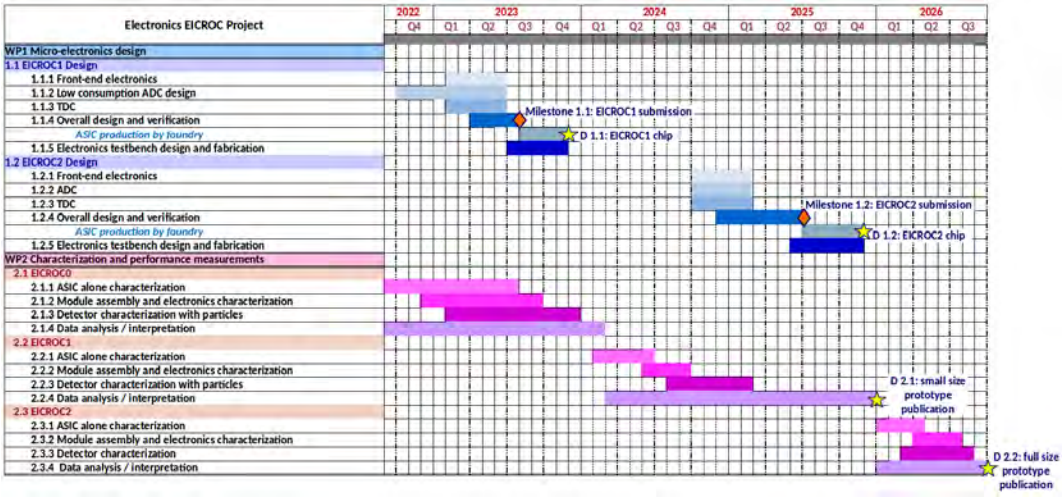

Figure 21: Timeline of the EICROC project.

3.1.2 FCFD1 design and characterization by FNAL/UIC

We propose to develop the next generation of the FCFD chip, a specialized 10-channel ASIC designed to read out signals from LGADs. This next stage of the development program (FCFDv1) will reuse the main components of the analog part of FCFDv0, such as the preamplifier and discriminator, but will target the addition of charge measurement needed for position reconstruction in AC-LGAD sensors. The 10-chanel ASIC would allow to build a large-area demonstrator of the technology that would be able to perform simultaneous measurements of position and timing of the passage of charged particles. The development of this version is expected to take the first half of FY23. After the successful demonstration of the system readout with a 10-channel system during FY23 and FY24, the next step, FCFDv2 would aim to build a full chip, including the digital readout, during the second half of FY24 and first half of FY25 (10-channel FCFDv2). The final, mixed-signal ASIC will be produced and tested during FY25, and its performance will be characterized using a single-layer AC-LGAD demonstrator at FTBF.

In FY23 we will lead the study to finalize the specifications for the 10-channel FCFDv1 ASIC such that it is optimized for sensors suited for applications in EIC experiments, such as AC-LGADs with 500 μm pitch and 1.0 cm length of strips. Upon the completion of this study, we will lead the development of the ASIC and its submission to TSMC to manufacture a set of prototypes. Testing on the bench by the lead engineer will be performed first to validate the basic performance, followed by testing with the ASIC connected to AC-LGAD sensors in test beams. Similar to the experience with FCFDv0, we will develop specilized readout boards for the testing of ASIC+LGAD assemblies.

The ASIC design will be carried out by FNAL ASIC design engineers (Tom Zimmerman and others), who have decades of experience in designing ASICs for particle physics experiments, such as

the QIE used in CMS experiment at the LHC, ETROC for CMS timing detector, and FLORA for X-ray experiments at LCLS-II. The UIC and FNAL postdocs and students will develop the ASIC specifications based on detailed studies of test-beam data from AC-LGAD sensors, develop the DAQ, and perform the characterization of sensors in test-beams. The group will work with FNAL scientists S. Xie and C. Peña on the design and characterization of the FCFDv1 chip. The team also includes postdocs and graduate students from collaborating institutes (Caltech, BNL, UCSC, University of Santa Maria Chile).

Deliverable #1 in BY1: Specifications for the FCFDv1, and selection of the sensors for demonstrator.

Deliverable #2 in BY1: Design, submission and initial testing of 10-channel FCFDv1.

Deliverable #3 in BY2: Detailed characterization of the FCFDv1 performance summarized in a publication.

Deliverable #4 in BY2: Design of the mixed-signal final 10-channel FCFDv2 ASIC for the demonstrator.

Deliverable #5 in BY3: Completed technology demonstrator, detailed studies of its performance and publication.

3.1.3 ASICs from third party institutions by SCIPP

In collaboration with two small electronics firms, SCIPP is currently a driving force in the development of two complementary approaches to LGAD readout. These include the CMOS-based HPSoC precision-timing "system on chip" development (Nalu Scientific) and the SiGe-based low-power ASROC front-end development (Anadyne, Inc.), both described above. We plan to continue our collaborative work with these two companies. For the case of HPSoC, characterization data accumulated for the initial five-channel prototype has allowed Nalu to begin, under our continued guidance, the refinement of the front-end design to meet the emerging goals of the EIC Detector effort. Support from this source, coupled with that expected from other sources, should allow the HPSoC collaboration to produce and characterize a second, more optimized prototype with a 10 Gs/s back-end digitizer. For the case of the ASROC effort, the FY23 will be expected to produce and characterize the first prototype of a 16-channel SiGe-based front-end amplifier ASIC geared towards the specific design goals of EIC LGAD sensors. SCIPP will also continue to collaborate with INFN Torino for the characterization of the FAST family of chips of which a new version is expected soon.

3.2 Frontend Electronics

To accompany the AC-LGAD frontend readout ASICs described above, dedicated readout electronics need to be developed and designed to provide the necessary clocks and slow control signals to the readout ASICs as well as receive, aggregate and submit the readout data out of the spatially constrained detector volume. To this end, we propose to form a collaborative AC-LGAD readout electronics working group between BNL, ORNL and Rice University to address these technically challenging questions.

This work will include fundamental R&D on an integrated clock conditioning and distribution system that meets the low jitter requirements of a sub-30 ps MIP timing system and implementation studies on streaming data acquisition architectures with the EICROC family of readout ASICs, based on "commercial off the shelf" FPGAs and components. At the same time, specific implementations of such systems, including power distribution and slow control links, will be studied and developed for the barrel and endcap regions of the TOF system. While we envision both barrel and endcap readout system to be based on the same general architecture, the differences in readout channel density, sensor module geometry and spatial constraints warrant independent (yet closely collaborative) developments for each region. The resulting readout board concepts will be applicable as an immediate basis for developments towards the readout system of the far-forward AC-LGAD detector systems

3.2.1 Readout board and precision clock distribution by BNL

The plan of the BNL group is to develop the readout chain from the dedicated ASIC to downstream off-detector electronics. We will start by procuring a Xilinx Dev Kit and characterizing it to read the EICROC0 and EICROC1 mounted on the PCB developed by the French team. For the first step

the sensor is not essential and we will only study the basic performance of the chip. The first tests of functionality of the FEEs will focus on noise studies, time walk and jitter and compatibility with the AC-LGAD system requirements. Along this line we will also explore various timing chips ("clock cleaners and jitter removal") which is a critical component for any TOF based detector.

The deliverable for the BNL group for FY23 is development of the preliminary prototype of an integrated readout board that supports the first iterations of the EICROCx. The ultimate plan of the BNL group is to design the overall architecture of the hardware including, the design of the cable, the optimization of streaming data, and the interface of the timing and control signals.

3.2.2 Barrel TOF service hybrid by ORNL

The work proposed for FY23 includes basic R&D for the design and construction of the power delivery and readout service system ("service hybrids") for the barrel TOF system to serve as a basis for the upcoming CD2 review. These service hybrids will connect to a row of AC-LGAD readout chips on a given TOF stave module and aggregate their data into a single data stream. At the same time the service hybrids deliver power distribution, sensor biasing, voltage regulation and slow control services to and from all readout chips and sensor modules.

With the proven experience of ORNL in designing thin, durable circuits based on Kapton-flex foil, we will explore a service hybrid design based entirely on such flexible PCBs to minimize the material budget. We envision an architecture based on a single FPGA per service hybrid responsible for data reception, aggregation and slow control of the connected readout chips as well as the data transmission via a connected fiber transceiver or high bandwidth e-links. Our R&D will explore the maximum number of readout chips we can connect to a given FPGA, which informs the maximum distance between readout chip and FPGA over which raw readout data needs to be transmitted. This has to be done in close connection with the mechanical design of the barrel TOF system, as the signal routing and flex PCB layout necessarily has to follow the mechanical structure of the detector.

An additional goal of our R&D will be the specification and basic demonstration of the required grounding and DC-DC powering schemes over the length of a TOF barrel stave.

The ORNL deliverable towards the TOF readout electronics includes a study to build TOF service hybrids out of flexible Kapton PCBs with integrated data aggregation and power distribution. Prototypes will be constructed to investigate the mechanical stability, signal integrity and power distribution capabilities of such assemblies.

3.2.3 Endcap TOF service hybrid by Rice

As one of main milestones planned for FY23, the Rice team will contribute to the development of a general layout of frontend readout electronics, focusing on the endcap TOF disks with pixel AC-LGADs, to be used as baseline for the CD2 review. We propose to develop a prototype frontend "service hybrid" based on a compact design of a readout board and power board to minimize material budget and space constraint. A prototype readout PCB board that provides a series of frontend services will be developed: (1) connectors that are compatible with EICROCs via flex cables; (2) data aggregation and transmission via electronic links and transceiver chips (e.g., lpGBT and VTRx+ by CERN); (3) slow control chip; (4) connectors to bias voltage power supply. A power board will provide low voltage power supplies to EICROCs and other on-detector chips for data transmission and slow control. We propose to build a power board based on CERN bPOL12V DC-DC converters with one layer planar spiral coil and a small connector that is pin compatible with the CERN bPOL12V_CLP module. The power board will also have a connector to low voltage power supply cables. With the anticipated delivery of first version of EICROC, our goal is to demonstrate a prototype full chain readout from the frontend to backend.

4 FY23 Resource Request

To perform the proposed work in FY23, we request in total 267k$ funds, including 148k$ for frontend readout ASIC development, and 119k$ for frontend electronics. A breakdown of these requests can be found in Tab. 5-6 and further detailed for each effort including in-kind contributions by participating institutions. Among these efforts, our top priority is frontend readout ASIC development, in particular EICROC1 design and submission. To ensure that we will have frontend readout ASICs that meet the design specifications for EPIC AC-LGAD detectors, we think that it will be crucial to support also FCFD1 submission and characterization of the ASICs, including those from third party institutions. Given the schedule of EIC project, we will need to design on-/off-detector electronics and validate the design by building prototypes by the time of CD2/3A review in October 2023. Therefore, it will also be important to support the R&D effort to design and build prototype service hybrids and work on readout board and precision clock distribution that meet the requirements.

Vendor/ Institute	**M&S Item**	**Cost per Item (k$)**	**N. Items**	**Tot. Cost (k$)**
Frontend ASIC				**118.3**
IJCLAB	EICROC1 submission	65	1	65
	EICROC test boards	-	-	10
FNAL	FCFD1 submission	25	1	25
	FCFD test boards	-	-	15
SCIPP	ASIC service boards	-	-	3.3
Frontend Readout Electronics				**31**
BNL	Xilinx Dev Kit	4	1	4
	Timing cihps and boards	15	-	15
ORNL	Xilinx Dev Kit	4	1	4
	M&S	8	-	8
TOT.	-	-	-	**149.3**

Table 5: eRD109 budget request for M&S costs in FY23 on frontend ASIC and electronics.

Inst.	**Task**	**Labor Type**	**FTE (%)**	**Tot. Cost (k$)**
Frontend ASIC				**29.7**
SCIPP	Service board design layout	Electronic Design Specialist	7.5	12.4
	Board Assembly	Electro-Mechanical Engineer	5	11.8
	Board loading and lab msmt	Assistant specialist	5	5.5
Frontend Readout Electronics				**88**
BNL	Readout and Timing Distribution	Research Associate	20	38
ORNL	Barrel TOF Low-Mass Service Hybrid	Electric Engineer	10	32
Rice	Endcap TOF Service Hybrid	Electric Engineer	15	18
TOT.	-	-	-	**117.7**

Table 6: eRD109 budget request for labor costs in FY23 on frontend ASIC and electronics.

4.1 Frontend Readout ASIC

4.1.1 EICROC

The FY23 budget request presented in Table 7 relates to the submission of EICROC1 within a Multi-Project Wafer (MPW) and the purchase of associated components such as the fabrication of printed circuit boards and cabling. The labor of French institutions collaborators will be in-kind. For future developments, such as those related to EICROC2, IJCLab, OMEGA and CEA/Irfu/DEDIP team will keep seeking funds from French funding agencies but such funds are not secured.

Institution	Resource	Task	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	WP2	60	0 (in-kind)
	Senior scientist	WP2	35	0 (in-kind)
	Senior scientist	WP1&2	20	0 (in-kind)
	Research engineer	WP1&2	30	0 (in-kind)
	Research engineer	WP2	25	0 (in-kind)
	PhD student	WP2	50	0 (in-kind)
	EICROC1 [8 (or 16) × 4 channels] submission (MPW)	-	-	65
	Fabrication of testboards and associated components	-	-	10
OMEGA	Senior research engineer	WP1	25	0 (in-kind)
	Senior research engineer	WP1	20	0 (in-kind)
	Research engineer	WP1	15	0 (in-kind)
	Assistant engineer	WP1	20	0 (in-kind)
CEA/Irfu	Senior research engineer	WP1	30	0 (in-kind)
	Senior research engineer	WP1	10	0 (in-kind)
Total	-	-	-	**75**

Table 7: eRD109 budget request for FY23 on EICROC. All entries in thousands of dollars.

4.1.2 FNAL

The FY23 budget request of the FNAL team is to support the production cost of the ASIC submission, and production cost of the readout boards ($40k).

Resource	Task	FTE	Budget (k$)
Staff Scientists	oversight and coordination	5	0 (in-kind)
Postdoc	Sensor testing	15	0 (in-kind)
Engineers	FCFD1 design	25	0 (in-kind)
Postdoc	FCFD+Sensor testing	25	0 (in-kind)
FCFD1 Multi-Project Wafer (MPW)	-	-	25
FCFD test boards and components	-	-	15
Total	-	-	**40**

Table 8: eRD109 FNAL Budget request for FY23 on FCFD. All entries in thousands of dollars.

4.1.3 SCIPP

Workforce at SCIPP on EPIC: 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, 8 undergrad students. Given the involvement of SCIPP both in the sensor and ASIC development a support in both. The total budget amount requested by SCIPP is 100 k$ split evenly between the two efforts, Tab. 9 contains the breakdown of the budget allocation at SCIPP.

Resource	Task	FTE (%)	Budget (k$)
Electronic Design Specialist	Service board design and layou	7.5	12.4
Electro-Mechanical Engineer	Board Assembly	5	11.8
Assistant specialist	Board loading and lab msmt	5	5.5
Materials and Supplies	ASIC service boards	-	3.3
Total	-	-	**33**

Table 9: eRD109 SCIPP budget request for FY23 on frontend ASIC R&D. All entries in thousands of dollars.

4.2 Frontend Electronics

The budget request for the AC-LGAD system frontend electronics R&D described in section 3.2 is given in Table 10.

Inst.	Resource	FTE (%)	Budget (k$)
	Readout and Timing Distribution R&D		
BNL	Research Associate	20	38
BNL	2 Staff Scientists	2x20	0 (in-kind)
BNL	Xilinx Dev. Kit	-	4
BNL	Timing Chips + Boards	-	15
	Barrel Low-Mass Service Hybrid R&D		
ORNL	Electrical Engineer	10	32
ORNL	Staff Scientist	10	0 (in-kind)
ORNL	Materials and Supplies	-	8
ORNL	Xilinx Dev. Kit	-	4
	Endcap Service Hybrid R&D		
Rice	Faculty	10	0 (in-kind)
Rice	Electrical Engineer	15	18
Total			**119**

Table 10: eRD109 Budget request for the TOF system readout electronics R&D in FY23. All entries in thousands of dollars.

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