ePIC Endcap TOF Layout: optimization and update

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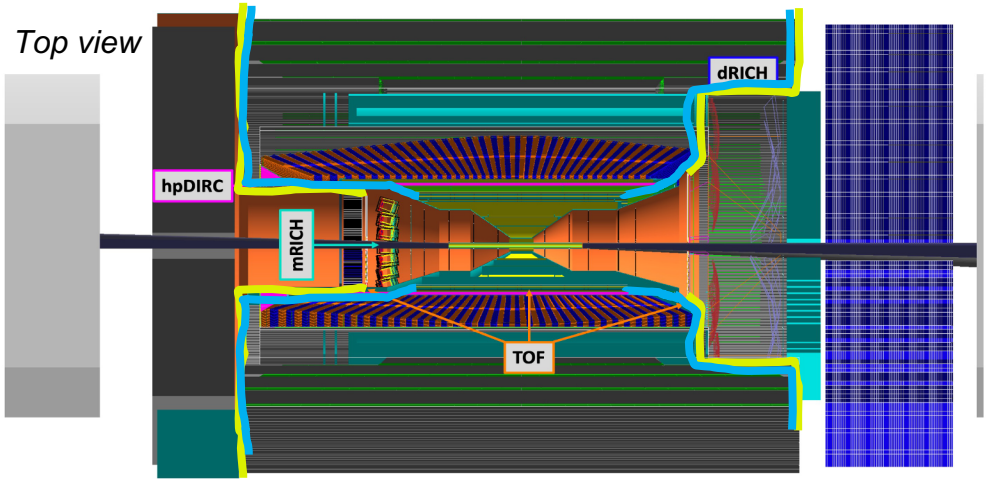
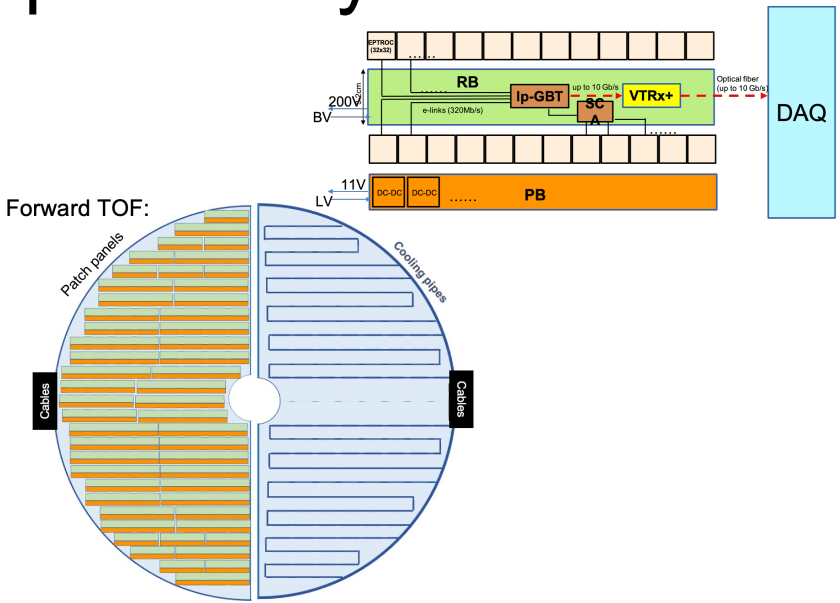
EPIC TOF-PID WG meeting
September 30, 2022

v0 design of endcap TOF layout

For v0 design, we propose:

- **Barrel: 0.5x10 mm^2 strips** – Zhenyu, 9/10
- **Endcap: 0.5x0.5 mm^2 pixels (same as RPs)** – Wei, 8/29





Forward+backward TOFs:

- A total of **~13M pixel channels**
- Total power: **20 kW** (7 for backward and 13 for forward)

Reducing the # of channels, if possible, will help mitigate pressure on the cooling infrastructure and reduce material budget

Sensors, ASICs and Service Hybrids

Sensors:

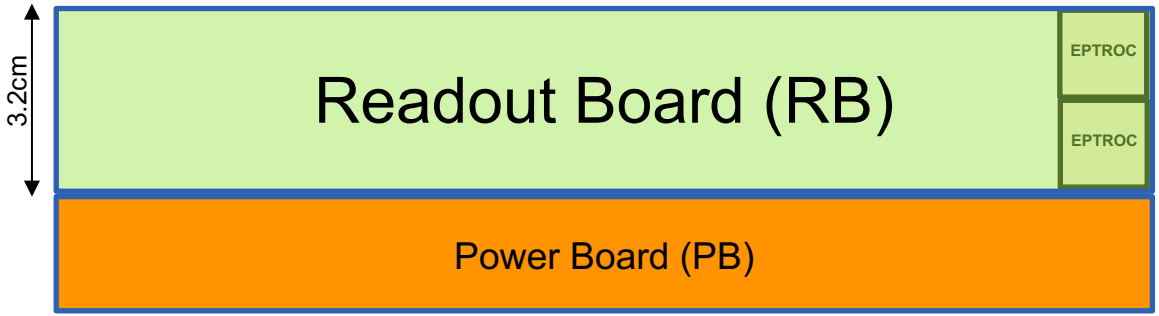
- Each sensor is a matrix of 0.5x0.5 mm^2 pitch pixels
- In general, larger sensors are preferred to maximize active area but also have to consider yields etc. in fabrication
- **Each sensor is assumed to be 32x32 pixels or 1.6x1.6 cm^2**

ASICs:

- Match the sensor pixelization and size and bump bonded to the sensor

EPTROC (32x32)

Service Hybrids: situated **on top of sensor+ASICs** provide power and readout services to the modules via flex circuit connectors

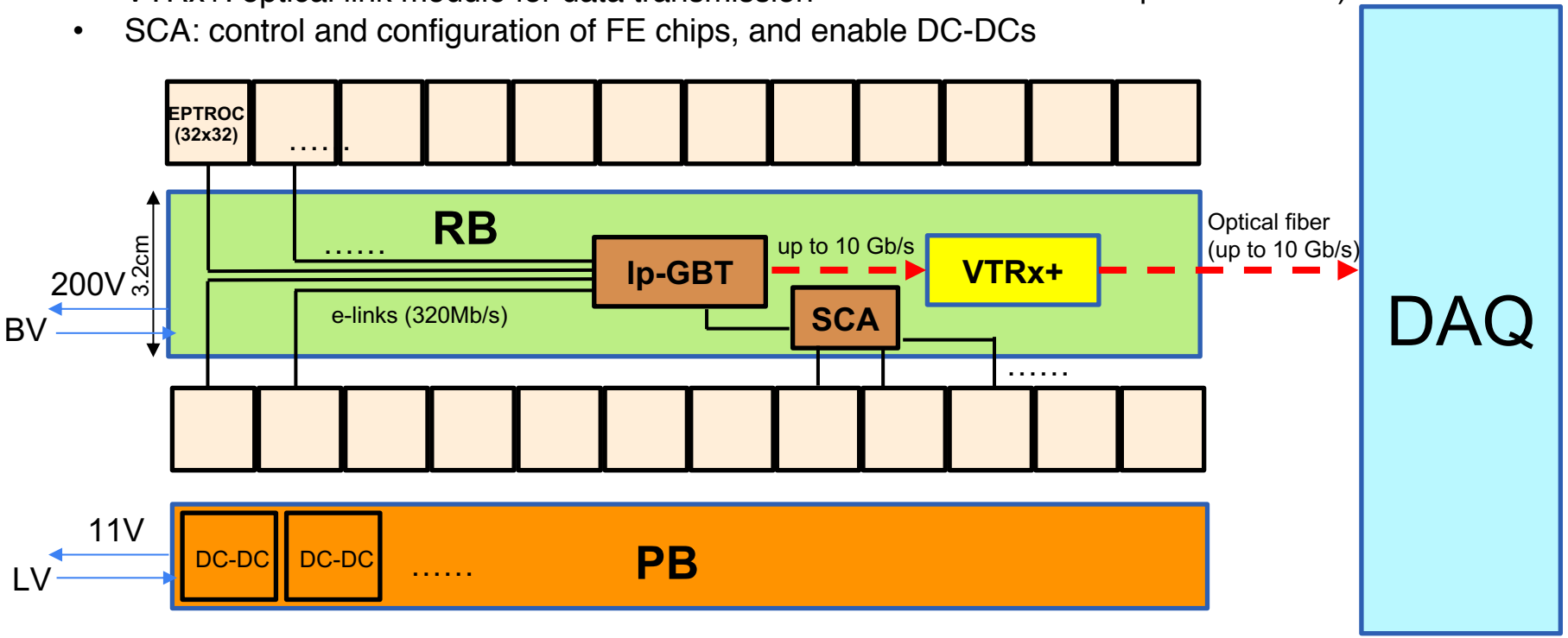


Service Hybrids

Each service hybrid will serve a number of EPTROCs

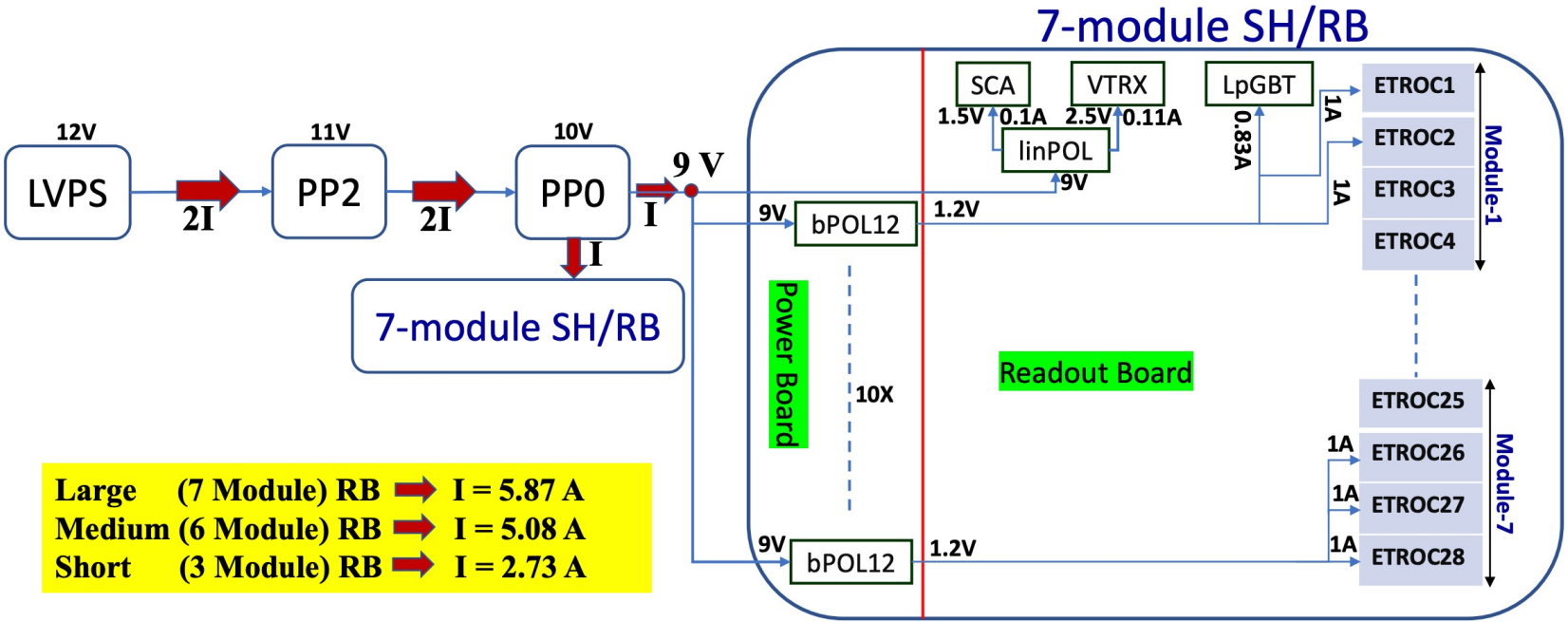
- lp-GBT: low power gigabit transceiver
- VTRx+: optical link module for data transmission
- SCA: control and configuration of FE chips, and enable DC-DCs

(CERN chips or
EIC equivalent ones)



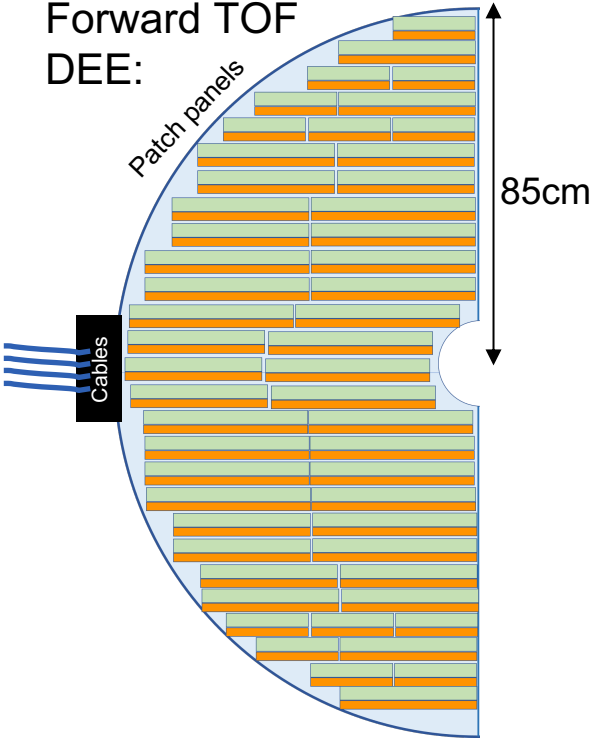
Service Hybrids

Powering of Readout board

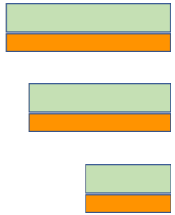


ETOF Layout (v0)

Forward TOF DEE:



3 types of modules to tile the full DEE:



48 EPTROCs

40 EPTROCs

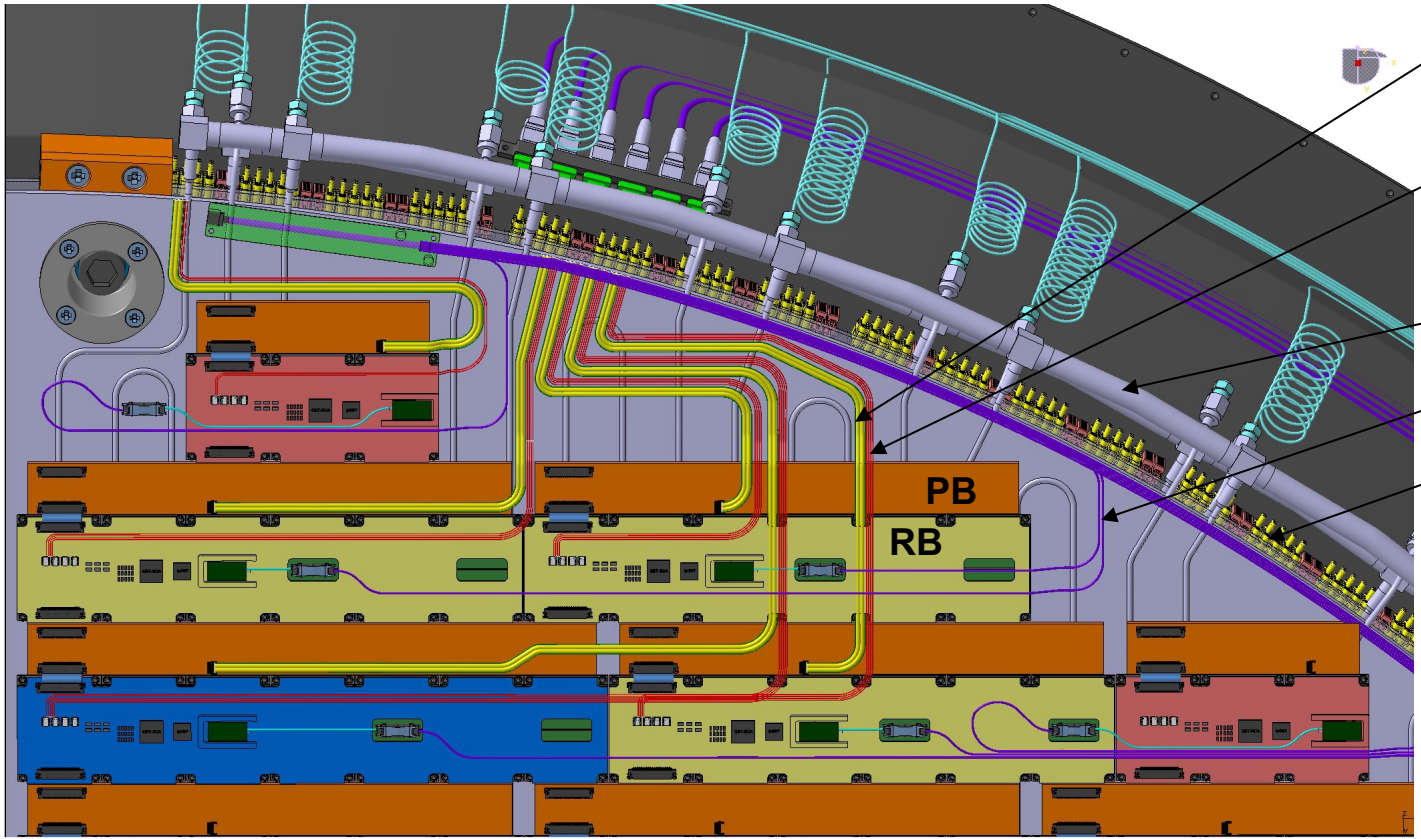
24 EPTROCs

For each module:

- 1 fiber to DAQ
- 2 LV cables (1 supply, 1 return)
- 2 BV cables (1 supply, 1 return)

	Forward	Backward
Sensors/ASICs	8704	4608
LV cables	424	248
HV cables	424	248
Fibers	212	124

Service routing in CMS ETL



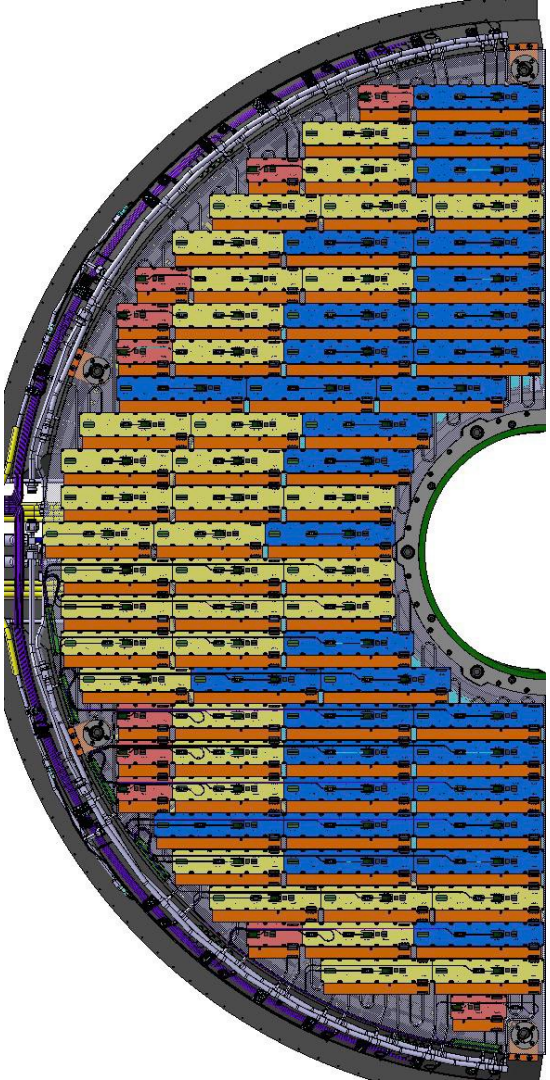
LV cables

BV cables

Cooling pipes

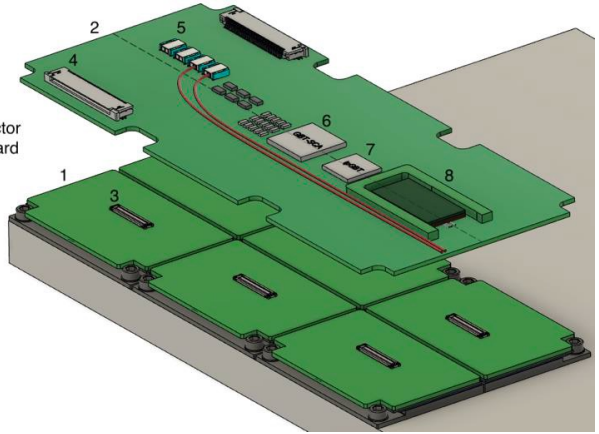
Fibers

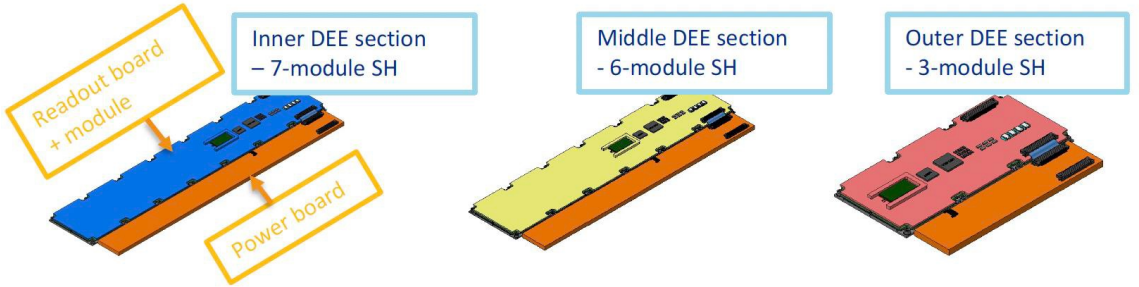
Patch panel connectors



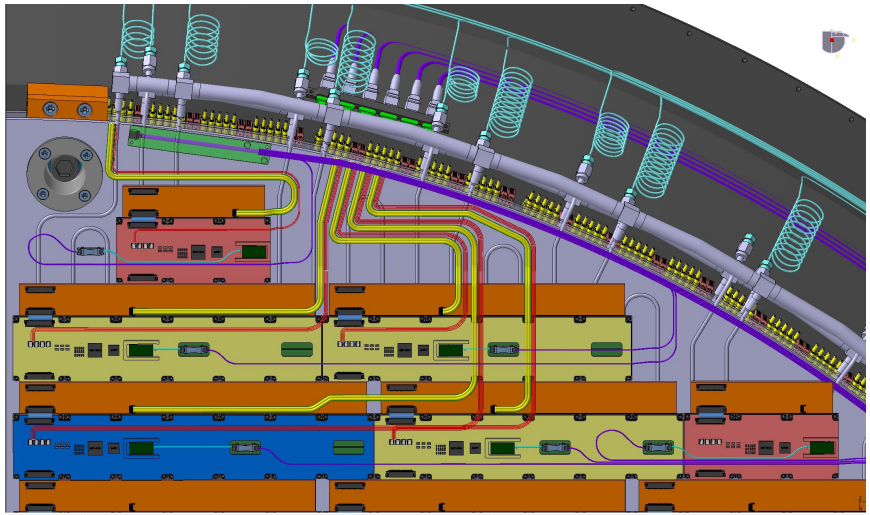
CMS ETL Layout

1: Flipped module
2: Readout board
3: Board-to-board connector
4: Connector to powerboard
5: BV connector
6: GBT-SCA
7: lpGBT
8: VTRx+





CMS ETL Layout



Power budget

0.5x0.5 mm^2 option

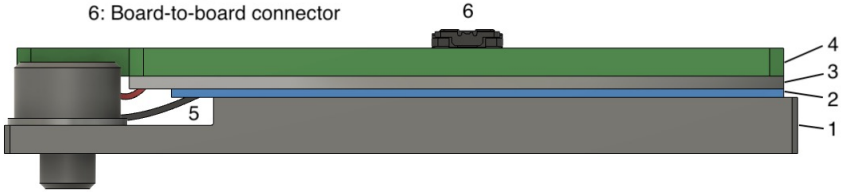
0.5x0.5	Forward	Backward
Sensors	0.6kW	0.35kW
EPTROC	8.5kW	4.8kW
DC-DC	3.5kW	2kW
lpGBT, VTRx+, SCA	0.5kW	0.3kW
Power cables	0.5kW	0.3kW
Total	13.6kW	7.75kW

0.8x0.8 mm^2 option

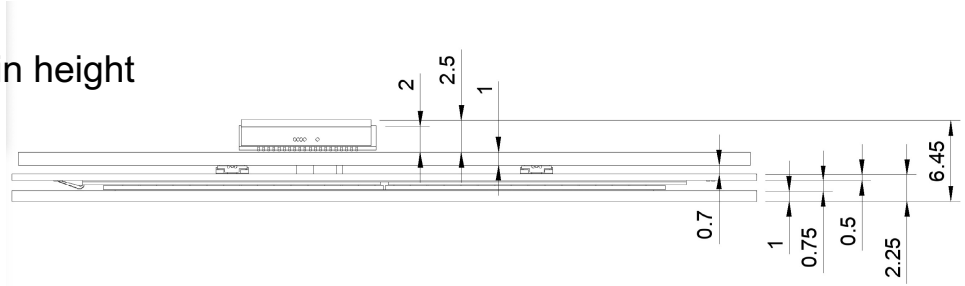
0.8x0.8	Forward	Backward
Sensors	0.2kW	0.13kW
EPTROC	3.2kW (6.4kW)	1.8kW (3.6kW)
DC-DC	1.3kW	0.75kW
lpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	6.1kW	2.9kW

Space requirement in z

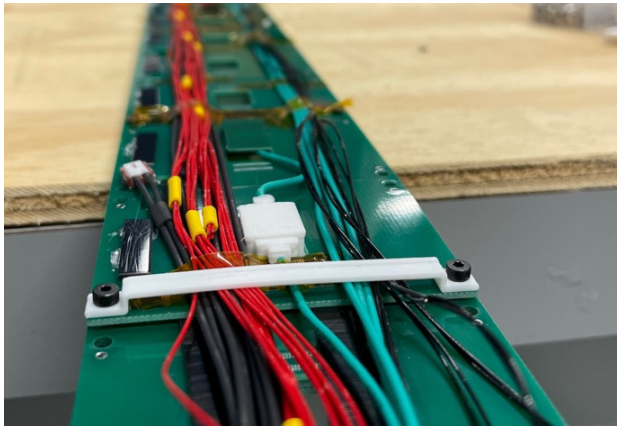
1: Base plate (AIN)
2: LGAD
3: ETROC
4: PCB
5: Wire bonds
6: Board-to-board connector



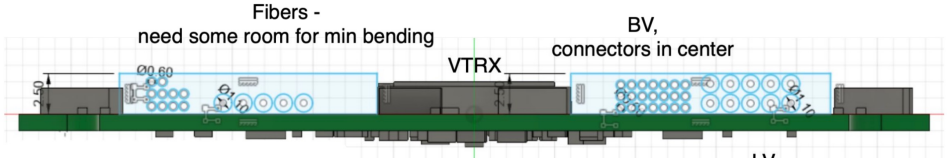
Sensor module: ~7mm total in height



Mockups developed for CMS-ETL

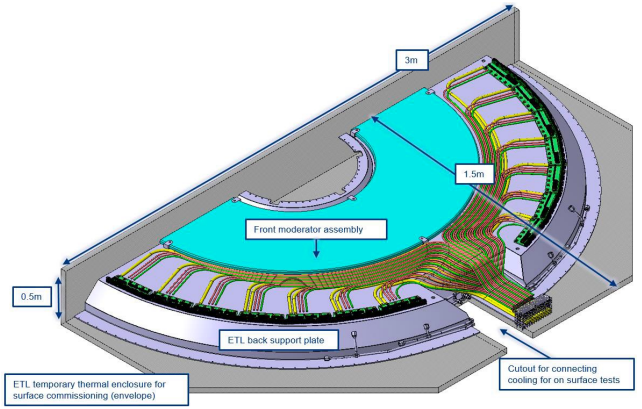


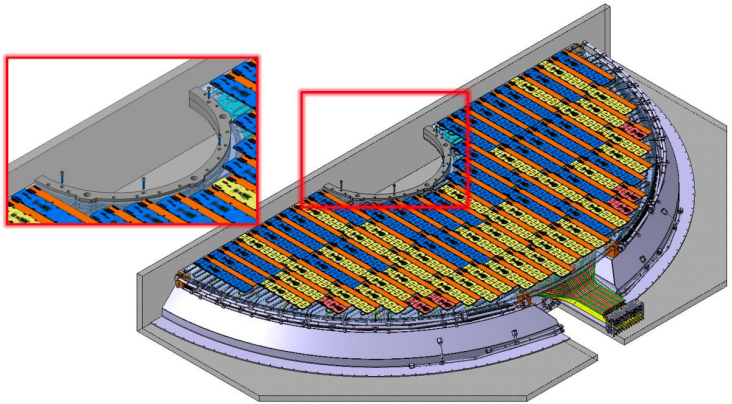
Servce on top of readout board: ~2.8mm



Space requirement in z

Elements in Z	Envelope
Front face of electronics	7 mm
Cooling and support disk	8 mm
Rear face of electronics	7 mm
Patch panels + cables	22 mm
Back support plate	5 mm
Thermal screen (if needed)	18 mm
Total	67 mm





Q&A from Tim

Q. slide # 5: This is the internal detector wiring?

Yes, correct. This is wiring on the readout PCB board.

Q. how is the power regulation done on the read-out board?

LV is regulated via DC-DC converters

I see here you have an inner assembly where everything is connected via a patch panel.

Q. Do you envision the patch panel as separate circuit boards mounted around the detector?

Yes, this is correct.

Q. Are you considering specific connector types or part numbers at this point, for both the modules and patch boards?

Yes, we have some preliminary estimate of numbers but they may change a bit as the design evolves

Q. What is the LV and HV requirement for the modules?

12V for LV and 200-350V for HV.

Q. slide #13: what is ~ space given here for cable routing?

We estimated total space requirement in z of about 7 cm max including all cables, service etc.

Summary

Considered alternative design of eTOF layout with large pitches of AC-LGADs

- 0.5x0.5 mm^2 pixel option could leverage the same ASIC design as RPs but may impose high demand in cooling infrastructure and more materials budget
- Increasing the pixel pitch can help substantially reduce the # of channels and thus cooling requirements (by a factor of 2.56 for 0.8x0.8 mm^2 and 4 for 1x1 mm^2), while still meeting the requirement in position resolution (also true for RPs?)
- For 0.8x0.8 mm^2 pitch as an example, cooling budget is estimated around 9-15 kW. Designs with other options can be easily derived.

We should study the performance and impact of increased pitch size in simulations (in progress) and R&Ds (eRD112 in FY23) in detail.

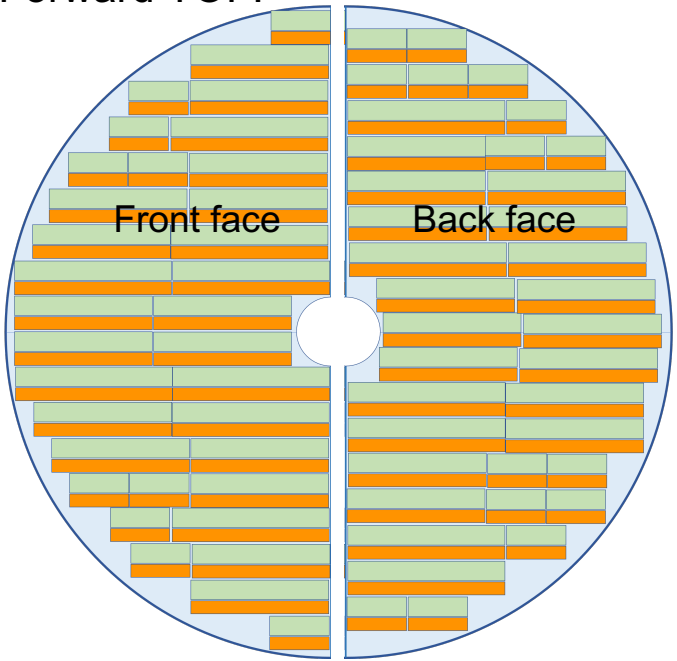
Next, we plan also to start working on details of design including electronics, cables etc. and evaluate more realistic material budget.

Backups

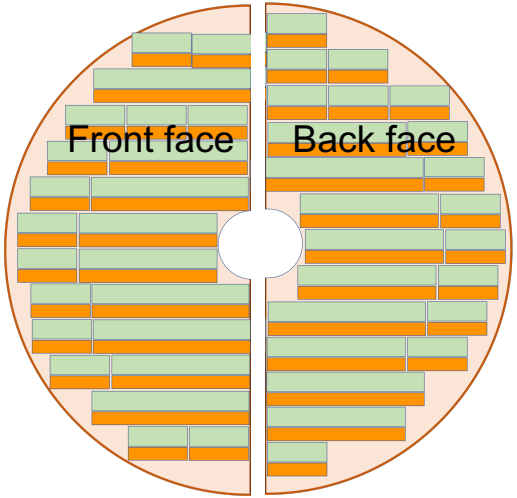
Optimizing the layout (v1)

Sensors+ASICs: matrix of 32x32 pixels,
with pitch of **0.8x0.8 mm^2**

Forward TOF:



Backward TOF:



Optimizing the layout

0.5x0.5 mm^2 option

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0.8x0.8 mm^2 option

	Forward	Backward
Sensors/ASICs	3112	1744
LV cables	248	184
HV cables	248	184
Fibers	124	92

For each module:

- 1 fiber to DAQ
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ETOF Power budget

0.8x0.8	Forward	Backward
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DC-DC	1.3kW	0.75kW
lpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	6.1kW	2.9kW

1.3x1.3	Forward	Backward
Sensors	0.1kW	0.05kW
EPTROC	1.2kW (2.4kW)	0.7kW (1.4kW)
DC-DC	1.3kW	0.75kW
lpGBT, VTRx+, SCA	0.2kW	0.12kW
Power cables	0.2kW	0.12kW
Total	3kW	1.8kW

ETOF Layout

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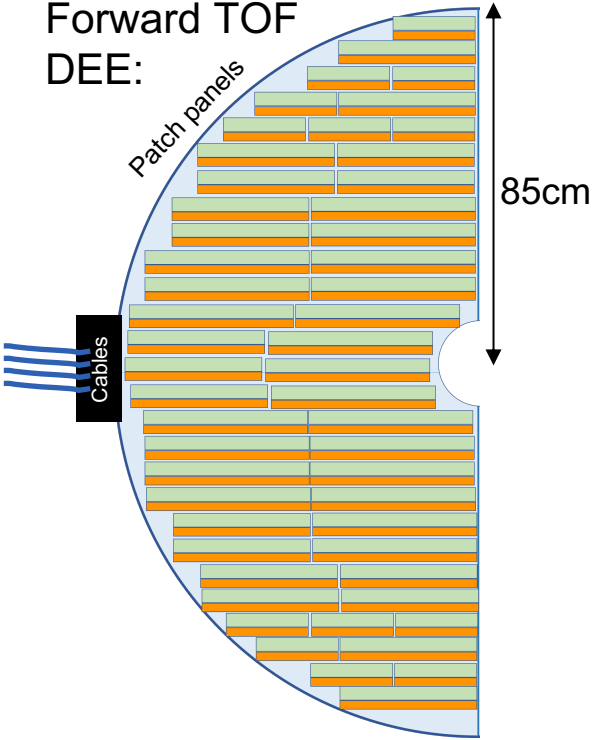
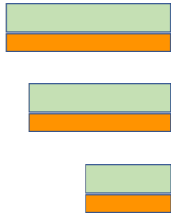


3 types of modules to tile the full DEE:



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