DAQ WG Action Items 9/29/22

* Define Structure for E/O boards
  + Are these shared boards that support each detector
  + Are these IP blocks each detector must incorporate in their specific design
* Define Electrical protocols for E/O boards.
* Define E/O boards protocol
  + Timing information
  + Synchronous commands
  + Flow control
  + Configuration &/or Slow Control
  + Error handling
  + Firmware loading
  + Hardware trigger details including latency and E/O board requirements
* Verify that we can 20ps timing accuracy using reconstructed clock through felix
  + Measure jitter
  + Measure phase stability over time / over power cycle
  + Measure effect of temperature variation
  + Measure effect of PS voltage variation
* Find & Share EIC/CAD document with electronics safety standards
* Standardize terminology
  + Timing System Distribution Board (interface between CAD timing and FELIX)
  + Board containing E/O interface
  + FEE and initial steps of aggregation before E/O interface
  + DAM / SAM / Felix
* Define list and count of boards required for full system
* Define schedule for this list
* Track, document, or have contact person for each detector FEE chain up to E/O interface. Maintain the status documents. This needs to be at the individual detector level, not just the detector WG level.
* Define overall data format
* Define output file structure (how many files per time slice & data model within files)
* Simulations of System Architecture
* Simulations of Beam Data Volume, Backgrounds
* Parameterization of each detectors expected noise
* Work with software group to merge streaming concept with offline simulation. Refactor simulation hits to be by time rather than event.
* Provide detailed design / description of data reduction plan for SiPM based RICH detectors
* Work out how to provide test setups for detector FEE design.
* Define Linux system administration scheme
* Define data quality monitoring system