10/20/2022 ePIC DAQ WG Agenda

1. Introduction / General points
    - 60% design, the requirement for the pre-TDR next summer and CD 2/3a, means well enough specified to define defendable detailed costing of components
    - Elke pointed out that we are the Electronics and DAQ WG and need to take an active part in the ASIC / FEE as well as the common DAQ. (I have been assuming that the responsibility for this is in the detector groups, but we need to be more involved in the early stages).
    - Streaming Workshop XI to focus on E/O interface and timing please raise agenda requests to Alexandre, Chris, Jo or Jeff
2. Far Backward DAQ Detectors and Requirements - Krzysztof Piotrzkowski
3. DAQ Task List Updates – Jeff Landgraf
    - Take aways from Dave Abbot's visit
    - Updates to task list
4. Streaming Workshop XI plans – Alexandre Camsonne

Summary of Take-aways from BNL visit last week

- FELIX
  - Hao Xu from BNL Atlas is lead engineer doing all hardware design. BNL was not/is not involved in the hardware design of the FELIX
  - sPHENIX FELIX production was manged by Jin Huang using the design from Hao
  - For sPHENIX (and potentially for EPIC) there were large cost savings by purchasing the FPGA along with ATLAS. The purchaser is BNL, not ATLAS or CERN so the external deal is simple, but the synchronization must be manged.
  - Atlas schedule milestones are:
    - Design Review - Oct 2023
    - Pre-production ready – December 2024
    - Production complete – May 2025
    - I think this means ASIC purchases done in FY 2024-25
  - Plan for a cheap stand-alone system is not clear, and not in the Hao's plan. The firefly 25gb/10gb interfaces can be swapped in/out and pin compatible FPGAs can be swapped in
  - The 182 needs external power, can be run independent of PCI, and supports 100Gb ethernet. These suggest to me that for most ePIC detectors a separate enclosure may be the most appropriate way to set up the DAQ interface to computing.

Summary of Take-aways from BNL visit last week (2)

- sPHENIX
  - The FEE's have multi-fiber connections, some of which go to the FELIX and some which are routed to a configuration/control/error handling interface. This requires the separation of the fiber bundles in "SOB" boxes. We need to consider carefully any similar need in ePIC.
  - Martin gave Dave & I a tour and demo of daqrc. He will present the QA system at a later ePIC DAQ meeting
- We understand the mechanics of getting EE/firmware support from instrumentation and other BNL resources better. We need to develop a roadmap for manpower requirements over the long term for BNL, JLAB and other institutions to build some stable relationships.
- Near term focus
  - Study TWEPP method to replicate high-precision clock
  - Define the FPGA features required for this high-precision clock
  - Evaluate the implications of these requirements for the FPGA cost in the optical interfaces.

Updates to Task List (1)

- Referring to WIKI table: https://wiki.bnl.gov/EPIC/index.php/DAQ
- “Define Structure of E/O Boards”
  - Probably multiple boards, but can multiple of electrical protocols be implemented in a generic board to use as a pattern.
- “Define Electrical Protocol for E/O Boards”
  - Need to go to sensor level and document operation and readout chain for:
    - MAPS (sPHENIX readout unit as example)
    - AC-LGAD – EICROC
    - SiPM/PMT – HDSoc
    - SiPM/PMT – HGCROC3
    - SiPM/PMT – ALCOR-EIC
    - SiPM/PMT – Custom ADC/FPGA FEE
    - MPGD- SALSA
  - Also need to define the power, cables, form-factors, and cooling so this need to be further divided to specific subdetectors soon as well…
  - A lot of this may be compilation from detectors/eRD groups

Updates to Task List (2)

- “Electrical Standards”
  - State the ESH process at BNL and mark done. We should note that generally BNL requires the UL standards so expect any CE only equipment to go through additional review as part of the ESH process.
- “Standardize Terminology”
  - The confusion was differing definitions of FEB/FEP. I think this will go away as specific FEE chains are documented, but for now my proposal is to use Electrical Interface and Optical Interface.
- “Detailed System Description”
  - Define standard information for each board in the system. FGPA cost, ASIC cost, high cost components (transceivers), cable lists, location / space /cooling requirements, # of boards needed
- Add a new task “FELIX production management”