Thoughts on the EPIC DAQ Readout Chain

(an opinionated & informal set of proposals)

Tonko Ljubicic, BNL

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Overview

EPIC Readout Scheme:

ASICs ⇒ Readout Board ⇒ FELIX Board ⇒ DAQ PC ⇒ onwards…

In this presentation I will:

- mention the ASICs briefly
- discuss the Readout Board & FELIX parts of the chain
- barely mention DAQ PCs or other parts of the DAQ

ASIC Model

- Usual ASIC signals:
  - in: 1 (or more) high precision clocks (e.g. 100 MHz); differential; LVDS or similar low-swing
  - out: 1 (or more) high speed serial links (e.g. 100-1000 Mbs); differential; LVDS or some other funky low-swing standard
  - in: sync/trigger/frame/revtick/orbit; differential
  - in/out: I2C or SPI control/configuration bus; single-ended, low pin count, multidropped; e.g. 1.2V or similar
  - in: I2C/Id pins; chip address; hardcoded hi/lo to rails/ground
  - in: optional RESET pulse; chip-dependent; diff or single
  - in: LV power; typically 1-1.2 V these days; possibly separate analog & digital
  - in: ground signals (usually need to be excellently implemented!)
  - perhaps others – depending on the ASIC
- It might be mounted on its own carrier/PCB with custom connectors for access to the above signals
  - BTW, in STAR we call such a PCB board a “FEE”
- it might need level adapters (passive? active?) to/from typical FPGA pin voltage standards
- note: an “ASIC” is also a COTS ADC
- but ASICs are not the subject of this presentation…

Readout Board (“Electrical-Optical Interface”)

- core function is to act as the mux/funnel of (electrical) ASIC data onto an optical fiber to DAQ
  - also serves as the demux of configuration data from the fiber (DAQ) to the ASICs
  - clock/timing source to the ASICs (important in EPIC discussions)
    - recovered clocks from the downlink fiber data link (as our Option A) or separate links for the clock/command interface (as our Backup Option which I think we should maintain)
  - other functions
    - light data processing (e.g. zero suppression, reformatting/reordering); detector specific
    - source & control of LV for the ASICs? (detector specific)
- known under many names & acronyms: FEE, FEB, RDO, FEP, etc.
  - I will call it Readout Board (RDO) in this presentation but we should *really* adopt a final name/acronym within EPIC
  - let’s set a vote on proposals :-)
- I am tacitly assuming that most RDOs will be close or on the detector
  - do we have this info? can we poll the detector groups, if not?
- requirements/assumptions:
  - low cost → we will have lots of them (as many as we have fibers)
  - low(ish) power
  - radiation tolerant (to some level…)
  - works in the magnetic field
  - small(ish) size, low mass

RDO Model

- a PCB, specific to every detector in shape/size/form but with expected common features
  - FPGA acting as the SERDES to/from DAQ and control of the ASICs
    - and source of the recovered main EIC clock
    - and some algorithms e.g. zero-suppression or something “simple”
  - PROM for the FPGA configuration (omitted if we use flash-based FPGAs)
  - JTAG connector for PROM programming
  - SFP+ module for electrical-optical interfaces and fiber (1 at least)
    - perhaps some other form factor?
  - clock/jitter cleaner chip (optional for some detectors, e.g. TOF)
  - low jitter clock fanout chips to the ASICs
  - DC/DC converters and/or regulators for LV power to the RDO (e.g. FPGA, etc)
    - but possibly also for the ASICs
  - connection/connector for a number (e.g. N=2-32) of ASICs
    - or none if the ASICs are directly connected to the RDO PCB
  - connector to LV cable (e.g. incoming 10V)
  - ID chip (e.g. I2C or 1wire to uniquely id the board), temperature chip (I2C or 1wire; can be within the ID chip)
  - debugging port (e.g. USB or serial; can be omitted for production versions)
  - LEDs (power, clock received & locked, other activity)
  - jumpers/switches (always put jumpers :-))
  - test pins (lots), some high speed (SMA); don’t need to be populated in production version
- more on RDOs in later slides…

Receiver Boards (“FELIX”)

- all right, let’s just call those “FELIX” :-)
- PCIe board sitting in a DAQ PC; receives data from the detectors over fiber; distributes clock/cmd & configuration to detectors
  - Questions: what kind of PCs are we assuming? 1U? 2U? 3U??? Can a 1U PC house the FELIX card sizewise at all? (full length? full height?) Power needs of this board? Do we envision more than 1 FELIX per PC?
- 24-48 fiber interfaces to the detector RDOs
  - via high density optical connectors
- 1 fiber (?) interface to the EPIC Clock & Command Distribution System [more later]
- FELIX for ATLAS is under further development: eventually Xilinx Versa based (is my understanding), currently Kintex Ultrascale+ (see e.g. sPHENIX)
  - designed at BNL (US) for ATLAS (big advantage IMHO)
  - firmware local to EPIC (I propose; e.g. see sPHENIX)
- I propose we form a *DAQ subgroup* responsible for the design & implementation of the FELIX system for EPIC
  - firmware, support device drivers, readout model, etc.
  - I propose this subgroup crafts a document **“FELIX Board Design & Users Guide for EPIC”**
- I also propose a contact person in charge of interfacing with the BNL FELIX hardware designers
  - this is a core EPIC DAQ component and we can’t let it “just happen” without having possibilities of inputs and control decisions; perhaps even formalized with BNL PO?
  - soon!
- Availability of current generation FELIX boards seems questionable to me (?) ⇒ I propose we define & use a development kit for our immediate prototyping:
  - Xilinx ZCU106 (with Zynq) or KCU116 (with Kintex)
  - (which availability is also questionable due to general chip shortages but we should agree now)
  - Zynq (my favorite) gives you a Linux backend which I feel is very convenient (one less PC to require)

Clock and Command Distribution System (or similar title)

- I propose a *DAQ subgroup* in charge of:
  - interfacing to the EIC accelerator clock distribution scheme/boards/whatnot
    - what do we expect to get from the accelerator and how? (in detail!)
  - designing the main Clock and Command System & Hardware for EPIC
    - distributes the EIC clock to all clients (FELIX boards, I assume)
    - distributes the command primitives (sync, heartbeat, trigger, other streaming commands) to all clients (FELIX boards)
      - we don't need a complete set right now but let's start with the very, very basics!
    - has significant monitoring/setup capabilities for the Shifcrew
    - etc, etc, etc….
  - responsible for the "Clock and Command Interface Specifications" document
    - signatories are detector groups
      - the detector groups need to understand and agree to the protocol at all times
    - as a bonus: such a document can be practically inserted as-is into an upcoming TDR

Back to the RDO: FPGA choice

- I propose we consider the Xilinx Artix Ultrascale+ as the baseline candidate
  - newest Xilinx technology, cheap (200$), expected to support clock recovery ala lpGBT
  - in case some detector finds this FPGA underperformant (speed might be an issue, yes) those groups should consider Kintex Ultrascale+ (but significantly more expensive)
- in case of issues with radiation tolerance we can evaluate a Microchip Polarfire FPGA
  - flash based (better rad tolerance, lower power), cheap ($200)
  - also has 10+ Gbs SERDES cores but we need to make sure it can support our clock-recovery scheme! (the biggest question to me at this moment)
  - the MAPS Detector eRD is considering its evaluation
    - any others?
- Nobody mentioned Altera or Lattice or …?
  - so I won't either…
  - however, now is the time for someone/somegroup to come forward

RDO: Proposed 3 Steps: Step 1 – Devkits (FY23)

- The DAQ/Electronics Group should propose its own evaluation board (devkit) for DAQ electronics development
  - evaluation of the clock transmission, commands, data, etc
- Requirements
  - 1x SFP+ 10 Gbs interface
  - FMC connector for extensions to ASICs or other items requiring testing
  - Xilinx Ultrascale+ technology
  - I would add a CPU core with Linux for convenience (Zynq)
- Detector groups (actually ASIC groups) already have/use their favorite developments kits. They all seem to be Xilinx based (right?)
  - we should poll all those groups to make sure the DAQ board will meet their requirements as well
  - we should urge detector groups which don't yet have a devkit to use the "DAQ approved" version
- Use this devkit in FY23 for:
  - establish a scheme for clock recovery and measure the various jitters (ASAP)
  - evaluate possible clock cleaner chips using small PCBs connected via FMC
  - establish the data & command canonical interface firmware which interfaces to the FELIX board
  - offer a common platform for detector/ASIC electronics testing
- My proposal: Xilinx ZCU106
  - Zynq Ultrascale+ FPGA

Step 2: DAQ-approved Reference RDO design (FY24)

- Already now (Step 1) I propose we form a DAQ/Electronics Subgroup for the design and specification of an EPIC DAQ RDO
- creates and maintains a document “EPIC Electronics Readout Design Guide for the Detector Frontends”
  - NB, this document should be easily incorporated into the Electronics/DAQ TDR
- based on this Design Guide this group *designs and manufactures* the “EPIC Detector’s RDO Reference Board”
  - with all required DAQ data & timing interfaces, with reasonably complete LV DC/DC converter design, with all other components
    - and firmware blocks as well
  - FMC connector for continued connections to ASIC prototypes and/or test pins
  - board is suitable for radiation tolerance tests as well as magnetic field tests
    - and other tests: power consumption, burn-in, link errors, etc.etc.
  - can be distributed in some quantity to all detector groups

Step 3: detector-specific RDOs (FY24+)

- the Detector Groups will eventually be responsible for
  - the final design of their specific RDOs: electronics and firmware
  - manufacturing, Q&A, testing, installation (& associated personpower)
  - formal budgeting (???)
  - ⇒ is this going to be the case? *We should get guidance from the Project*
- the DAQ RDO Subgroup should know and understand the Detector RDO plans at all times
  - general overview to avoid miscommunication
  - but also to take advantage of technology savings (cost and design, risk maintenance) among all Detector Groups
    - common items: FPGAs, PROMs, LV DC/DC converters, etc.etc.
  - common firmware blocks should be shared and treated as “hardware” for the purpose of lowering the engineering cost (and time), risk maintenance, etc

A Proposed Readout Chain for Right Now

1. ZCU106 as the eFELIX board for prototyping
   a. later subsumed by a real FELIX (or prototype)
2. ZCU106 as the RDO board (pre)prototype
   a. later subsumed by the Reference Design RDO
   b. with available ASICs on FMC connector
3. Measuring devices *and* expertise
   a. high speed oscilloscopes (or other devices) for clock jitter and phase measurements of ~1 ps resolution
   b. 100 MHz low jitter clock source injected into our “FELIX” board devkit (1 ps jitter)
   c. expertise on the required measurements (and interpretation)
4. ⇒ establish, verify & measure the jitter & phase of the clock recovery scheme which we plan to use (ala lpGBT)
   a. yes, there will be a cost for the hardware and yes, there will be (cost of) engineers involved e.g. 6 person-months

Other Electronics Subjects

- Grounding Scheme
  - under the Electronics/DAQ Group or Global Integration?
  - I will tentatively assume that the main on-detector ground will be the steel of the magnet and the detector is floating
  - ***but*** this needs to be designed and not left to each detector to figure out
  - with ground loop sensors too
- LV Distribution
  - under the Electronics/DAQ Group or Global?
  - LV distribution needs to be designed and supported
  - cable types, connectors, voltages?
  - power supplies (commercial? custom?), cooling of PS? location? AC power needs?
- HV (or bias voltage) distribution
  - not DAQ's problem IMHO but I mention it for completeness

Summary

- form Subgroups
  - Readout Board Subgroup
    - delivers the document “Design Guide for the EPIC Detector Frontend Electronics”
    - delivers a PCB example/reference implementation of an RDO
    - provides & maintains common firmware blocks (SERDES iface, clock distribution etc.)
  - Receiver Board (FELIX) Subgroup
    - delivers “User Guide for the EPIC FELIX Board” (not the best name, agreed)
    - interfaces to the BNL PO ATLAS FELIX project
    - provides firmware & device drivers for the EPIC “eFELIX” incarnation
    - perhaps with interfaces to or sub-subgroup for AI/ML or other processing on the FELIX board?
  - Clock & Command Distribution Subgroup
    - delivers “EPIC Detector Clock & Command Interface Specifications”
    - designs the Clock & Command Distribution System (a set of electronics boards)
  - the subgroups can be formalized as CAMx levels or work packages (but not mine to say)
  - I would propose that the delivered documents be already made in a form suitable for inclusion into the DAQ/Electronics TDR as paragraphs (to save time)
    - BTW, I would propose we start on the TDR: enumerate paragraph titles at least
- start with the clock recovery scheme verification ASAP using development kits

Conclusion

I think we should promptly start making operational decisions regarding a practical path forward which can additionally be utilized for the DAQ/Electronics TDR.

[along these or any other lines]

Thank You for Your Patience!