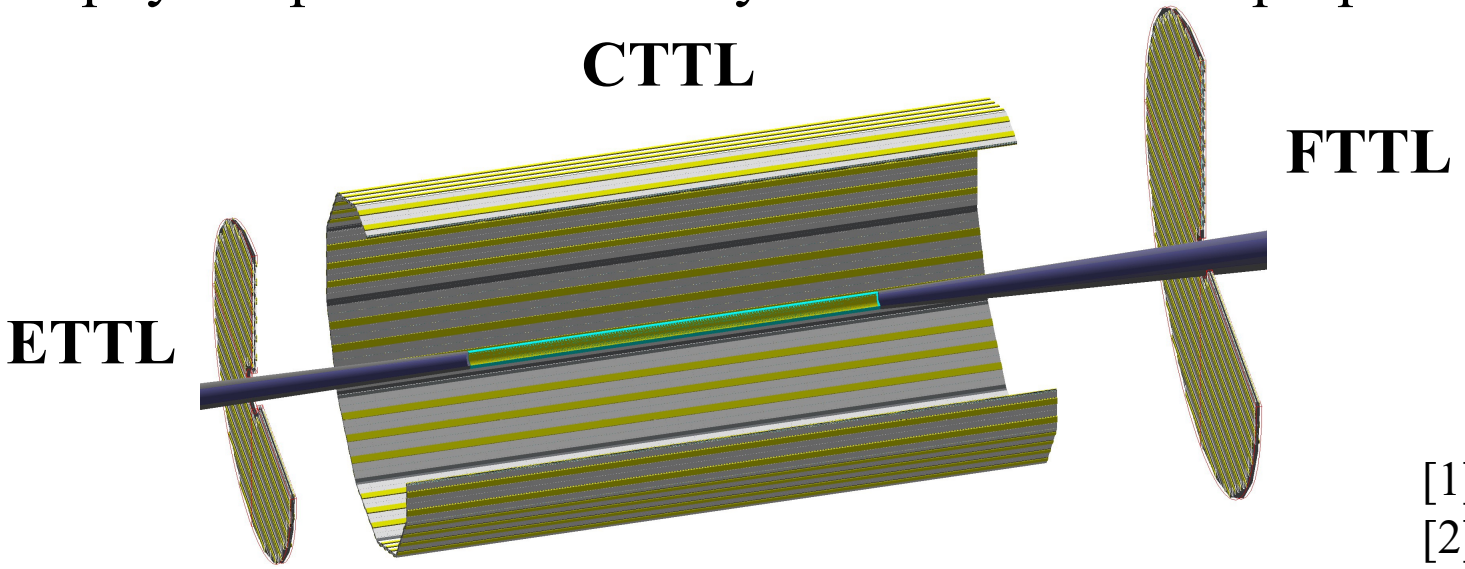
AC-LGAD Layer for TOF PID + Tracking

- The goal is to conceive a reference layout and technical design (v0) as inputs to GD/I group to advance the detector integration (service routing etc.)
- However, there are still on-going studies to investigate the optimal channel granularity based on physics performance so by no means this is a proposal for final design.



For v0 design, we propose:

- **Barrel: 0.5x10 mm² strips [1]**
- **Endcap: 0.5x0.5 mm² pixels [2]**

[1] Z. Ye, TOF-PID WG Meeting Sep 12, 2022
[2] W. Li, TOF-PID WG Meeting Sep 19, 2022

	acceptance	Z (m)	Radius (m)	Area (m²)	Channel size (mm²)	# of Channels	Power (kW)
ETTL	$-3.7<\eta<-1.74$	-1.61 to -1.71	0.12 to 0.63	1.20	0.5*0.5 -> 0.8*0.8	4.8M -> 1.9M	8 -> 3
CTTL	$\|\eta\|<1.4$	-1.2 to 1.5	0.625 to 0.655	10.9	0.5*10	2.4M	4
FTTL	$1.5<\eta<3.5$	1.555 to 1.705	0.12 to 0.85	2.22	0.5*0.5 -> 0.8*0.8	8.8M -> 3.5M	14 -> 6

News

- Discussion about ETTL at **EPIC GD/I Meeting 9/26 and 10/3**
  - LAPPD for RICH detector also provide TOF
  - Too much power close to EEMC Crystals, which are sensitive to temp. change
  - Too much materials in front of EEMC, which degrades EM resolution
  - Tight space constraint in the backward direction
  - Decision is to not include ETTL in the upcoming simulation campaign but perform separate MC studies to understand the requirements on position resolution and material budget
- Meeting with Project office and engineers last Friday to discuss TOF integration
  - Support CTTL at 3-4 points along the staves mounting on DIRC
  - Need to make FTTL smaller to make space for cable routing for inner detectors

  - We want to find out the impact of the ETTL power on EEMC crystal temperature
  - We need to define the service (power/cooling, cables, …)
  - We can ask for project engineering design support

FY23 Planning

[1] https://wiki.bnl.gov/EPIC/index.php?title=TOFPID
[2] https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23

Simulation [1]

- DD4HEP geometry, digitization, reconstruction
- Spatial resolution requirement
- Timing resolution requirement
- Material budget requirement

Project Engineering and Design (PED) - TBD

- Mechanical engineering
  - Endcap TOF
  - Barrel TOF
  - Cooling system
- Electric engineering
  - Prototype readout board, cable
  - Precision clock distribution (<5 ps)

eRD112 [2]

- Sensor (382k$)
  - BNL, HPK/FBK productions
  - Lab/beam test, Irradiation
- Sensor/ASIC integration (45k$)
  - Interposer
- Mechanical structure ($35k)
  - Low-density mechanical structure

eRD109 [2]

- ASIC (148k$)
  - EICROC1, FCFD1, SCIPP
- Frontend electronics (119k$)
  - Timing chips and streaming readout
  - Barrel/Endcap TOF Hybrids