Beam-Hjet breakup tagging: RHIC Run23 tests

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EICUG polarim.
mtg. 05.10.22

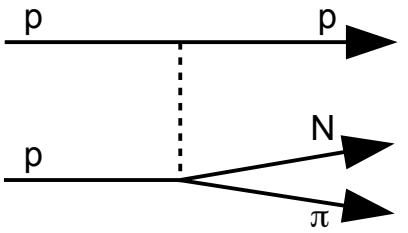
- Motivation
- Run22 tests
  presentation EICUG polar. mtg. 11.05.22*
- Requirements for Run23 tests:
  - Hjet readout extra module ?

  need input from JLab DAQ experts:
  - different readout mode Hjet/tagger modules ?
  - Hjet trigger → tagger module ?
- Extra slides: info on Hjet/JLab readout (A. Poblaguev)

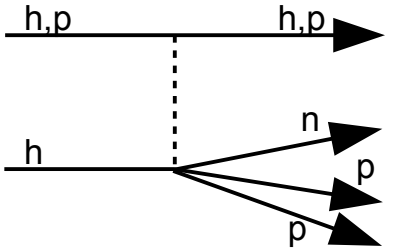
*https://indico.bnl.gov/event/15532/contributions/63237/attachments/40912/68391/EICUG_polarim_11.05.22_ZDCs.pdf

Motivation

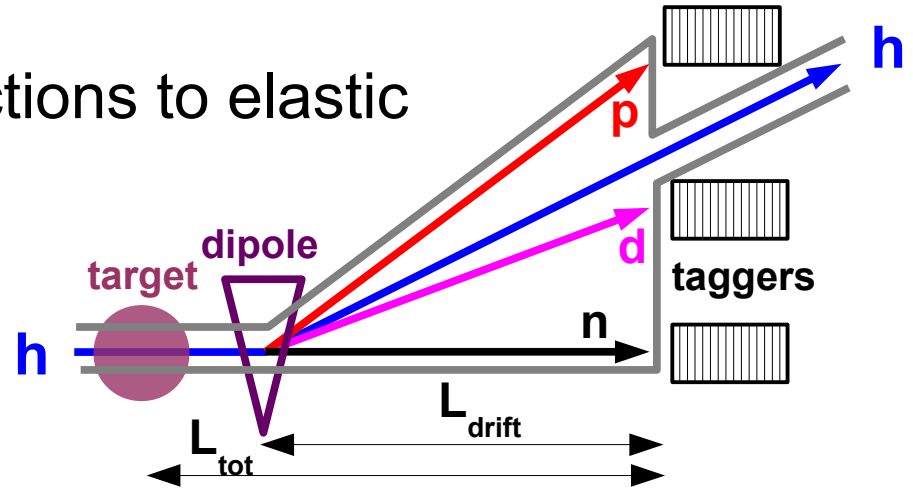
- Absolute polarimetry requires elastic scattering:
  e.g. Hjet @ RHIC pp→pp, ^{3}He @ EIC hh→hh or hp→hp
- Proton can break up e.g. pp→pNπ
  large mass difference (p,pπ) ~100 MeV
  resolved in Hjet recoil detector



- ^{3}He can break up hh→hdp or hh→hnpp
  small mass difference (h,dp) or (h,npp) few MeV
  not resolved in Hjet recoil detector



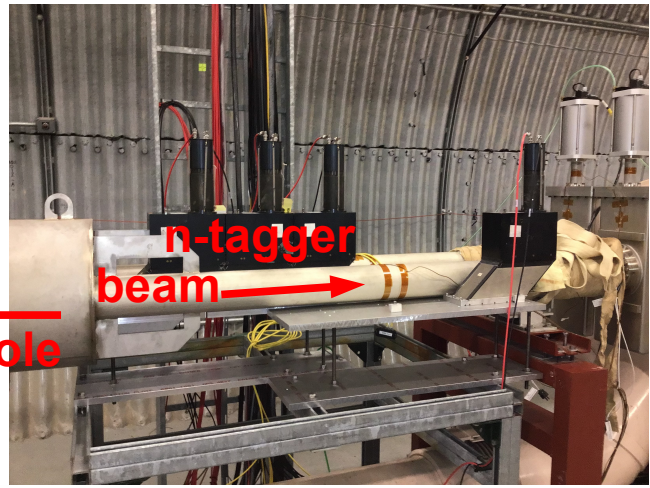
- Can tag ^{3}He breakup fragments,
  reject inelastic events, estimate corrections to elastic
- Implementation might look like:
- EIC IR design group:
  - place @ IR4 defined for polarimeters*
  - with required sequence:
    Hjet→dipole→drift space→n,p taggers (d too close to beam)



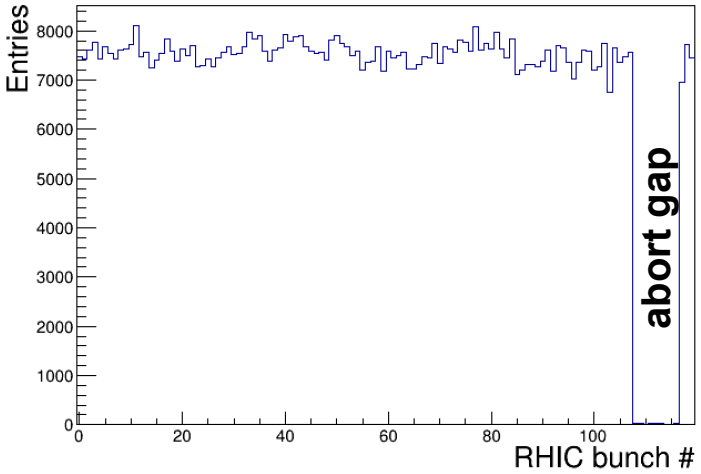
*https://indico.bnl.gov/event/16983/contributions/67945/attachments/43143/72531/EICUG_polarim_07.09.22.pdf

Run22 tests: pp

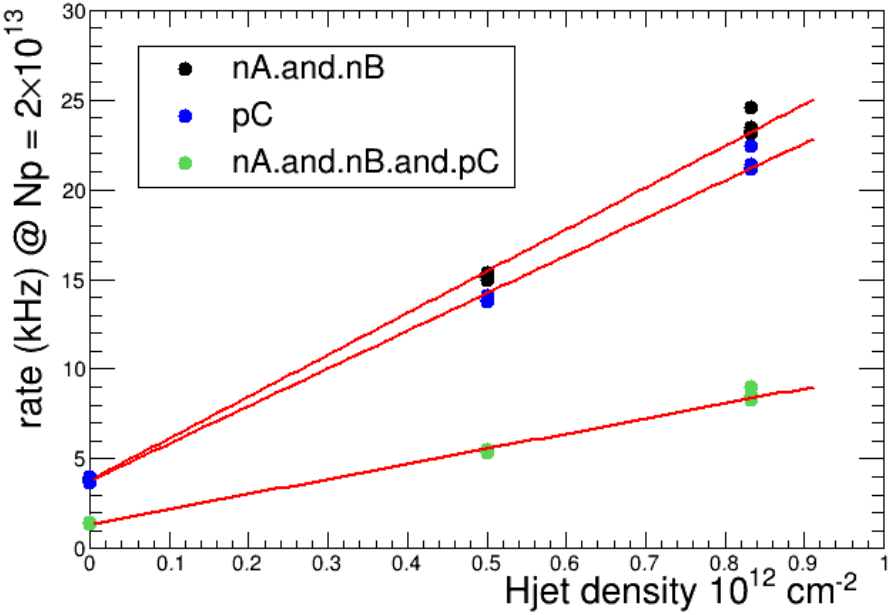
- Spare ZDCs (hadron calorimeters) installed: downstream of Hjet, after dipole bend
- Read out in spare pC polarimeter DAQ channels (easy, run between pC measurements)



- Tagger hits correlated w/ p-beam: hit, p-beam same bunch structure



- Tagger rate ∝ Hjet target density:



Demonstrated:
tagging p-beam breakup in Hjet o target interactions

Run23 tests: ^{3}He p

- 2023: plan to have RHIC APEX* time with ^{3}He beam

*Accelerator Physics EXperiments

- Allow ultimate breakup tagging test:
  hp→pnpp, detect recoil p in Hjet, n in taggers
  estimate breakup rate (expect few %)
- Need to correlate Hjet, tagger hits: same DAQ system

<u>Present Hjet DAQ (96 channels)</u> details extra slides

- each channel autonomous: trig. on pulse > threshold
- saved each channel
  - full wave form, ~80 samples, ~4 nS
  - Amplitude & Time reconstructed from wave form
  - time stamp: RHIC bunch # (0-119)
    RHIC revolution #, incremented every 12.8 μS

  together identify unique bunch ×ing, offline correlate different chan.
- Saved in buffer, read out VME every ?

DAQ: Hjet + taggers

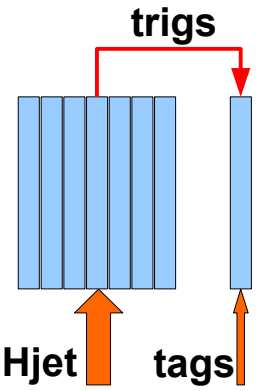
- Present Hjet DAQ has 6 FADC250 modules, 16 chan. each
- Could sacrifice few (4-6) unimportant Hjet chan., plug in taggers
- But rates: Hjet channels ~10 Hz; tagger channels 10's kHz
  taggers would quickly fill module buffers
- Can we add another FADC250 module for tagger chans. ?

<u>If yes:</u>

- Can the tagger module store all but waveform samples ?
  save factor ~20 buffer filling rate. Maybe still too high...

<u>Better solution:</u>

- Can Hjet channel triggers be used to trigger tagger module?
  - tagger rate stored < Hjet rate, no rate problem
  - but no independent measure of tagger rates



Extras

- Andrei's slides on Hjet VME readout @ PSTP 2015:

BROOKHAVEN NATIONAL LABORATORY

New DAQ for the HJET polarimeter at RHIC

Andrei Poblaguev
Brookhaven National Laboratory

The RHIC/AGS Polarimetry Group:
I. Alekseev, E. Aschenauer, G. Atoian, A. Bazilevsky, K.O. Eyser, H. Huang, D.Kalinkin, Y. Makdisi, A.Poblaguev, W. Schmidke, D. Smirnov, D. Svirida, G. Webb, K. Yip, A. Zelenski

New VME based DAQ (2015-…)

- Wiener VME 64x crate + Single Board Computer
- 6 FADC Boards (Jefferson Lab)
  - *16 channels per board*
  - *12 bit*
  - *250 MHz*
  - *General Purp. Firmware*
    - *internal trigger*
    - *deadtime-less*
    - *raw waveform available*
  - *External signals:*
    - *244 MHz Clocks derived from 28.15 MHz RF signal*
    - *Sync Reset (every Jet Cycle, ~5 min)*
- Front Panel Signal Distribution Module (Jefferson Lab)
- BNL V128 Input-register (Jet polarization status)

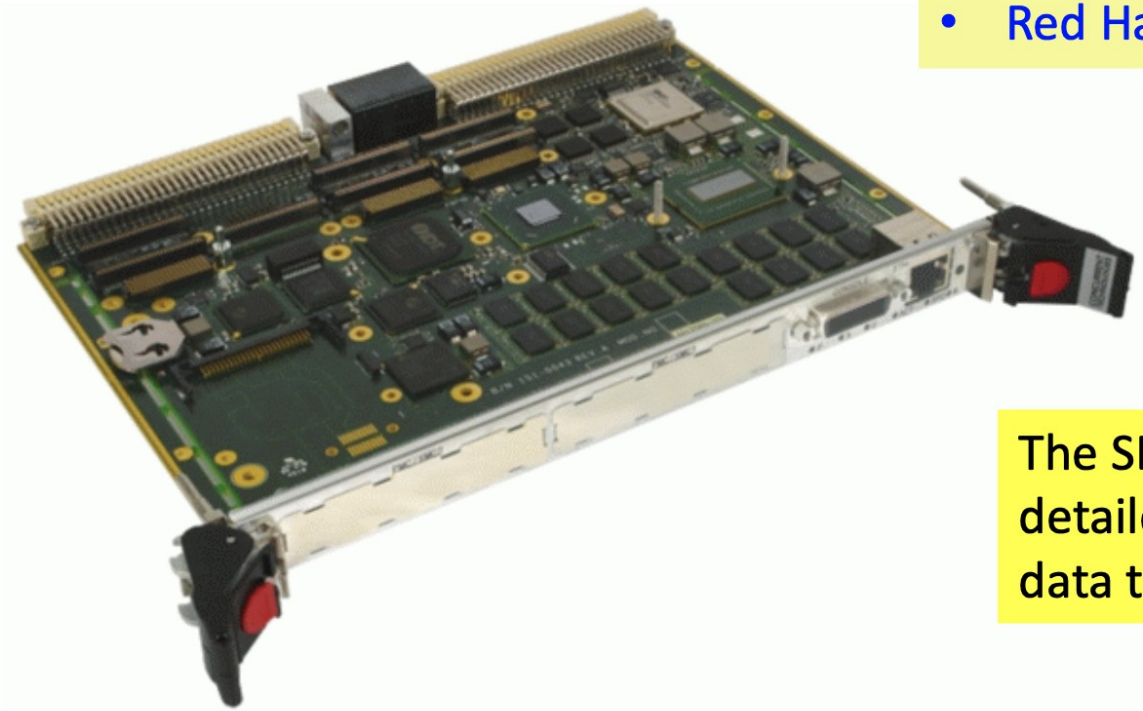
Total Rate in HJET ~ 10 kHz (2 Mbyte/s) allows us to use FADC general purpose firmware and acquire raw waveforms (80 samples -> 328 ns)

- ***The new DAQ was assembled without destroying the old DAQ. The infrastructure of the old DAQ was employed in the new one.***
- ***It takes only about 30 min. to switch between DAQ's (reconnection of 96 signal cables)***
- ***A software interface to use new data format with old analysis was developed.***
- ***This allows us to migrate to new DAQ smoothly.***
- ***New data analysis was also developed.***

Single Board Computer (SBC)

CONCURRENT TECHNOLOGIES

VX 915/011-14

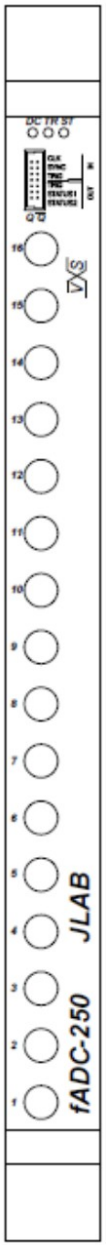


- 4-core 2.1 GHz Intel Core i7-3612QE Processor
- 16 Gbytes DDR3-1600 DRAM with ECC
- VME64 interface supporting A64/A32/A24/A16/D64/D32/D16/D8(E0), MBLT64, 2eSST and 2eVME
- 500 Gbyte Hard Drive
- Red Hat Enterprise 6 Linux

The SBC is powerful enough to provide detailed online analysis in parallel with data taking.

FADC250

The board was designed for the Jlab Hall D.



fADC250

VME64x Flash ADC Module Specifications

Signal Inputs	Number	16 S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable
	Offset	±10% FS per channel via DACs
Clock	Sampling	250 MSPS, Differential
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)
	Source	Internal and External
Control Inputs/Outputs	Clock	IN – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)
	INL	± 0.8 LSB
	DNL	± 0.5 LSB
	SNR	56.8 dB @ 100 MHz Input
	Data Latency	32 nS
Trigger Latency	8 µS	
Data Memory	8 µS	
Data Processing	Sparcification	
	Windowing	
	Charge, Pedestal, Peak	
	Time (Over Threshold, Relative to trigger)	
	Output (Backplane, VXS)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0	
Packaging	6U VME64x	
Power	+3.3V, +5V, +12V, -12V	

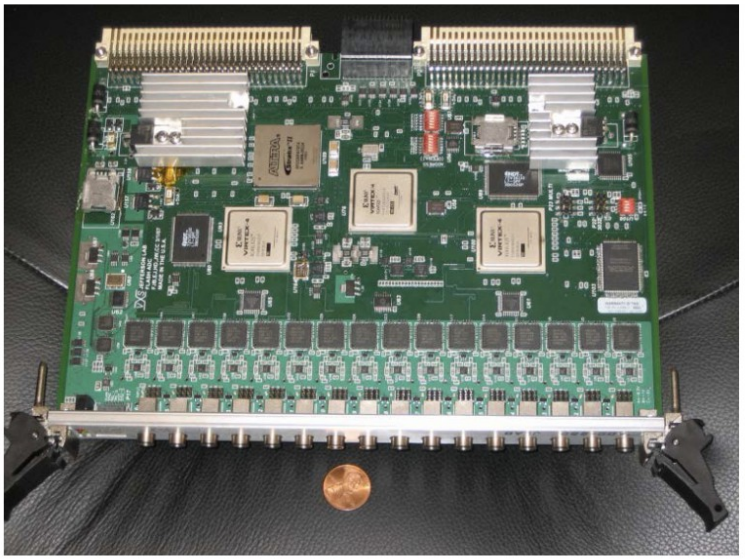
FAB_JLAB_FADC_SPEC.DOC

- ***16 Channel***
- ***12 bit, 250 MHz***
- *Internal Trigger , deadtime free*
- ***Waveform length up to 511 samples (2 µs)***
- ***Dead Time Free***

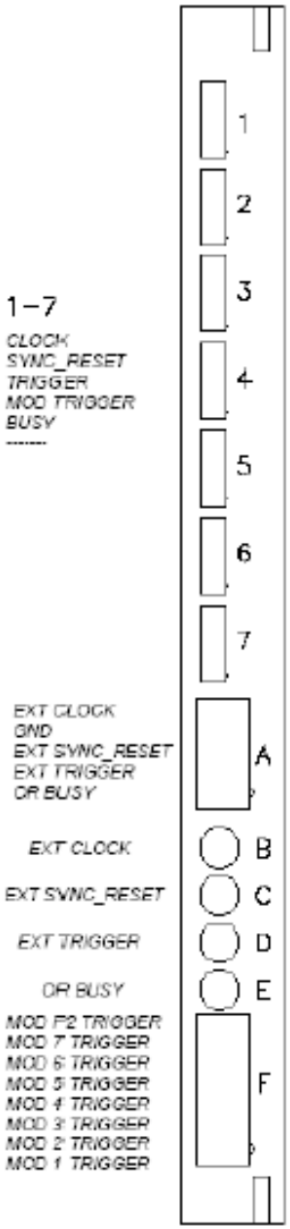
External Inputs:

(from the Signal Distribution Card)

- ***Trigger***
- ***Sync Reset***
- ***Clocks***



Front Panel Signal Distribution Module for the FADC250 (FP-SD)



The board was designed for the Jlab Hall D.

- ***The SD-FP distributes synchronized Clock, Trigger, and Sync Reset signals to up to 7 FADC250 boards.***
- ***Supports external and internally generated signals***

For RHIC Run15 we borrowed 7 FADC 250 boards and FP-SD from JLab.

We have got significant help from Jlab Fast Electronics Group.
FADC Firmware was upgraded in accordance with our requirements.

We acknowledge the outstanding contribution of
Chris Cuevas, Hai Dong, Ed Jastrzembski, and Bryan Moffit
to the development the new DAQ for the Hjet polarimeter at RHIC.