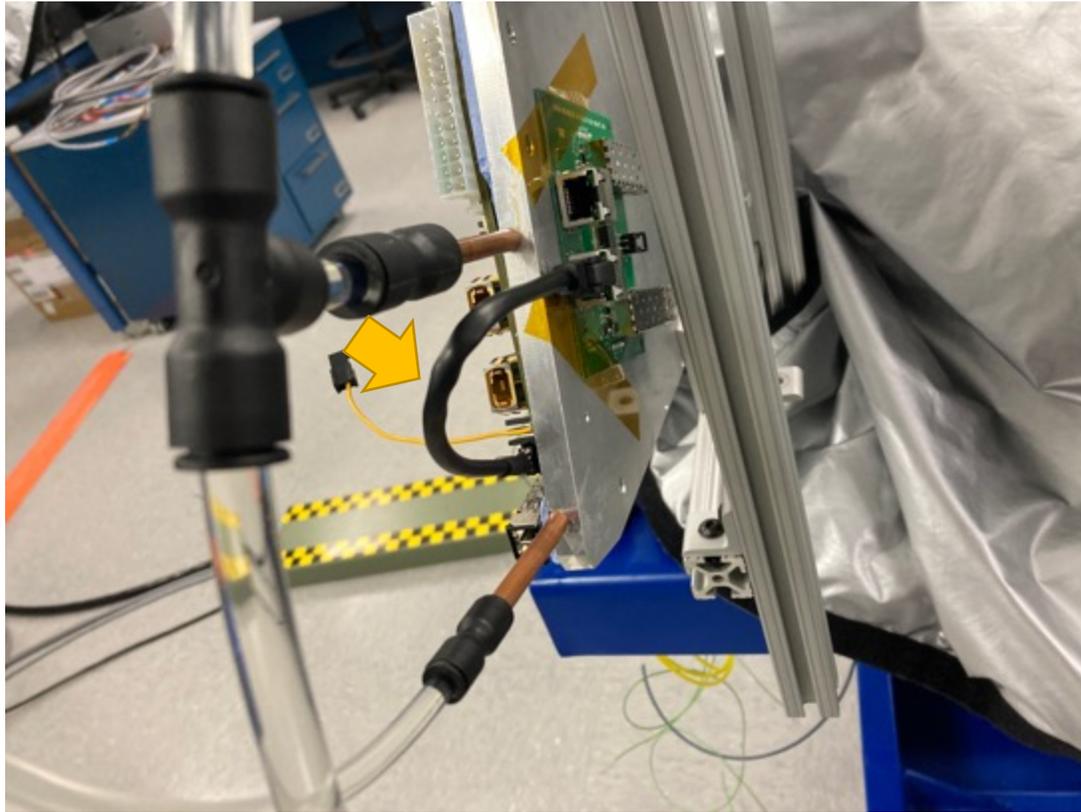


Short Term Plan

RIKEN/RBRC

Itaru Nakagawa

Production Beam Clock Cable



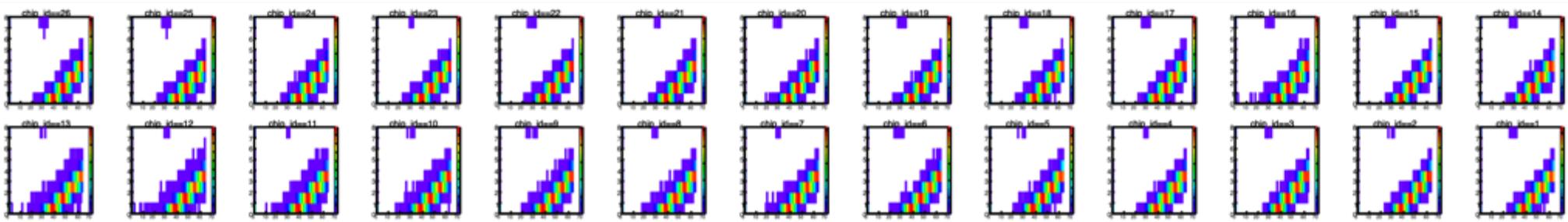
Some minor stress is there at the connector in ROC side though, the connector won't pop-out right away. Leave this cable for a while to monitor. We'll look into details next Tuesday with Dan and Rachid.

RCDAQ

- May 26, 2022 sPHENIX Summer School
 - Martin's slide : <https://indico.bnl.gov/event/15547/>
- RCDAQ documentation:
 - https://www.phenix.bnl.gov/~purschke/rcdaq/rcdaq_doc.pdf

Will have a discussion with Martin in the afternoon next Wednesday.

Optimization of the DAC Setting for Calibration



DAC Setting for the calibration

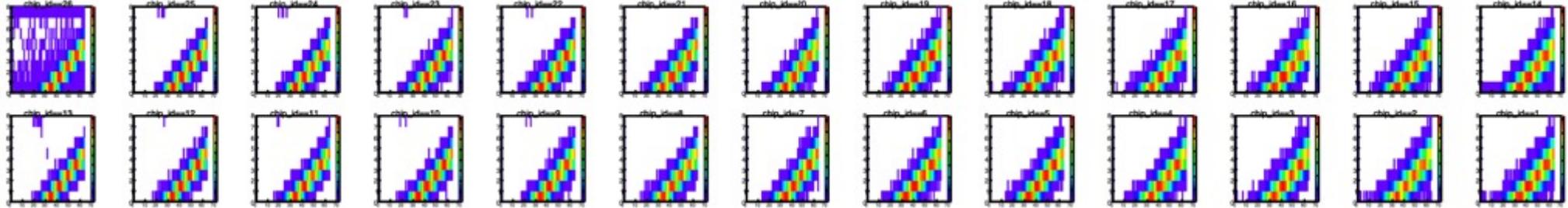
ADC	Calib
0	20
1	25
2	30
3	35
4	40
5	45
6	50
7	55

The screenshot shows the 'FPHX TestStand DAQ' software interface. The main window displays a 'Chip Control' configuration for Chip ID 21, Side 15. A 'Channel Mask' grid is visible, with a 'Beam mask' button below it. The 'Chip Side Enable' grid is also shown. On the right side, there are various control panels including 'Global Chip/DAQ Operations', 'DAQ Configuration', 'Pulsar Configuration', 'Module Enable', and 'Manual Packet Send'. The 'Module Enable' panel shows modules 1 through 15, with 'Module 15' and 'Module 14' highlighted in green, indicating they are enabled. The 'Manual Packet Send' panel shows 'Packet file to send' set to 'ROOT' and 'Module ID' set to 6. The 'Communications' panel shows 'USB' selected and 'Baud Rate' set to 115200. The 'ver7' panel shows 'ROOT' selected and 'Module ID' set to 6.

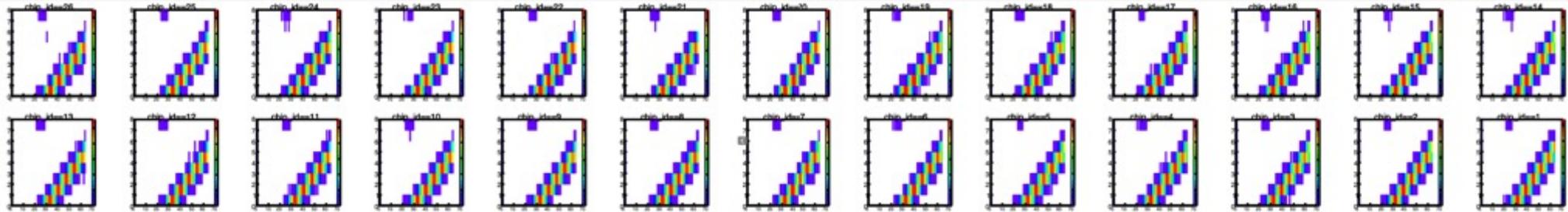
The default DAC setting is succeeded from FVTX.

Calibration Result Comparison

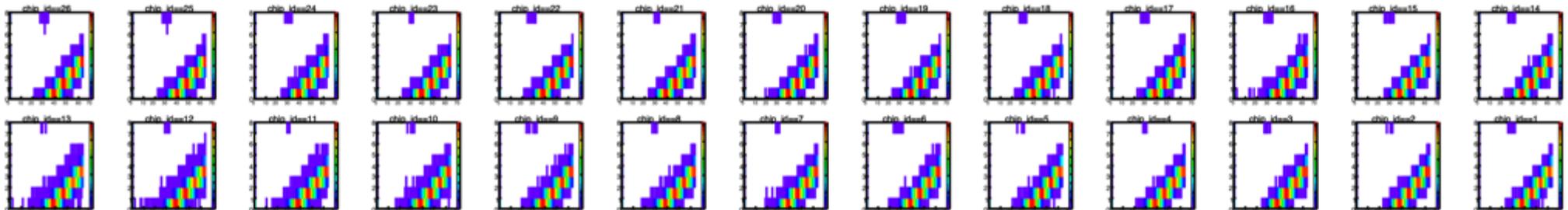
- FVTX



- INTT+ μ -coax Cable

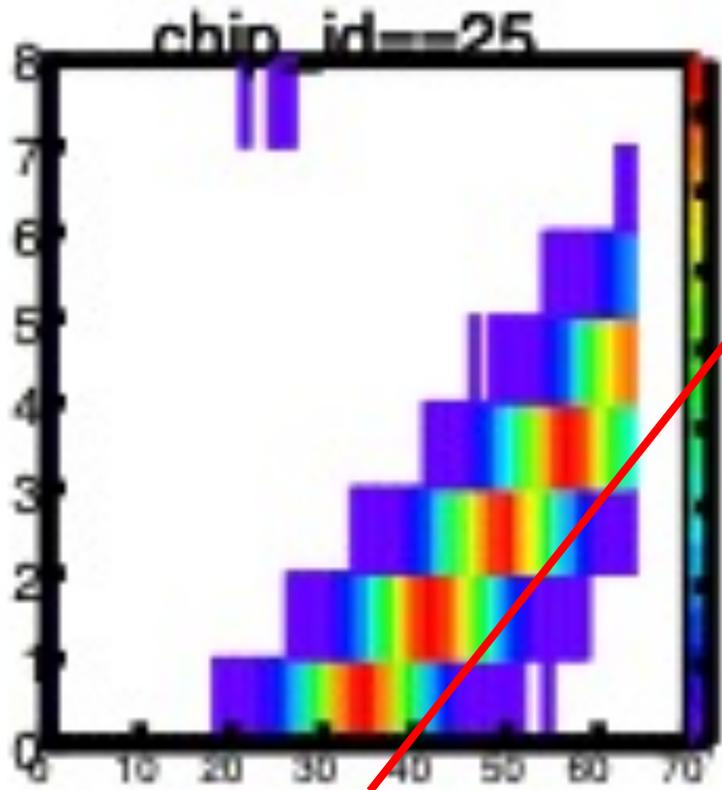


- INTT + BEX + μ -coax Cable

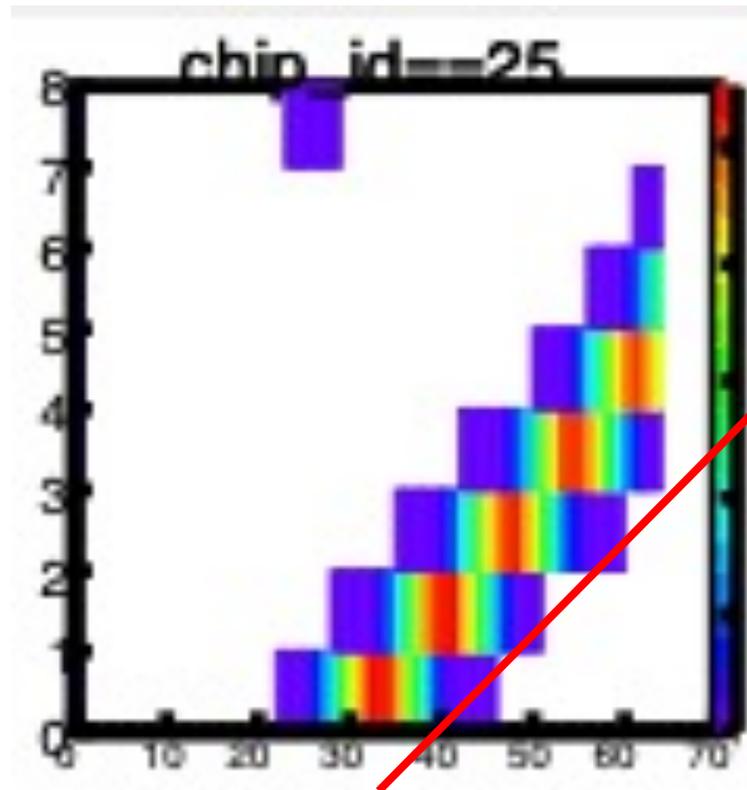


Default DAC Setting Result

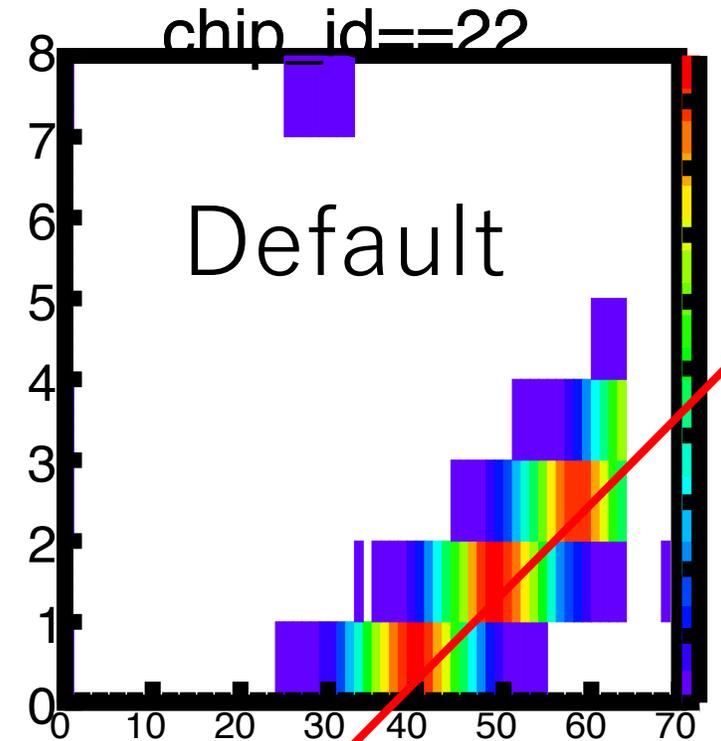
FVTX



INTT+ μ -Coax



INTT+BEX+ μ -Coax



Due to long readout cable path of INTT system, the calibration pulse height is reduced in the long path before it reaches to FPHX chip. Thus we are pulsing only DAC0~DAC4 or 5 in INTT+BEX+ μ -Coax setup. We should reconsider optimized DAC setting for the INTT.

Optimization of Calib DAC setting

DAC	Calib	Beam Test
0	20	15
1	25	30
2	30	60
3	35	90
4	40	120
5	45	150
6	50	180
7	55	210

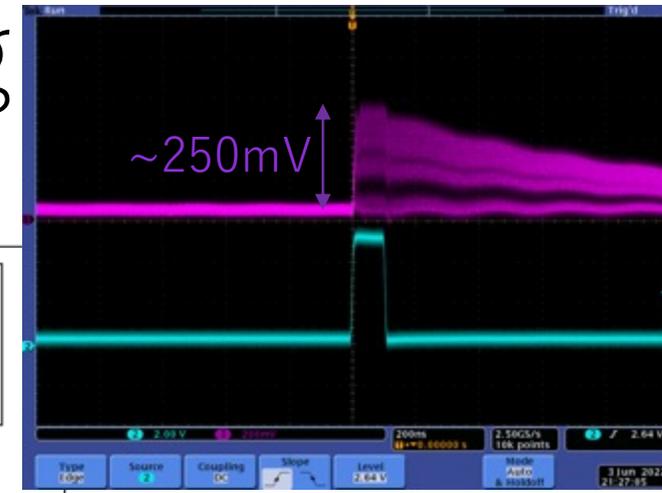
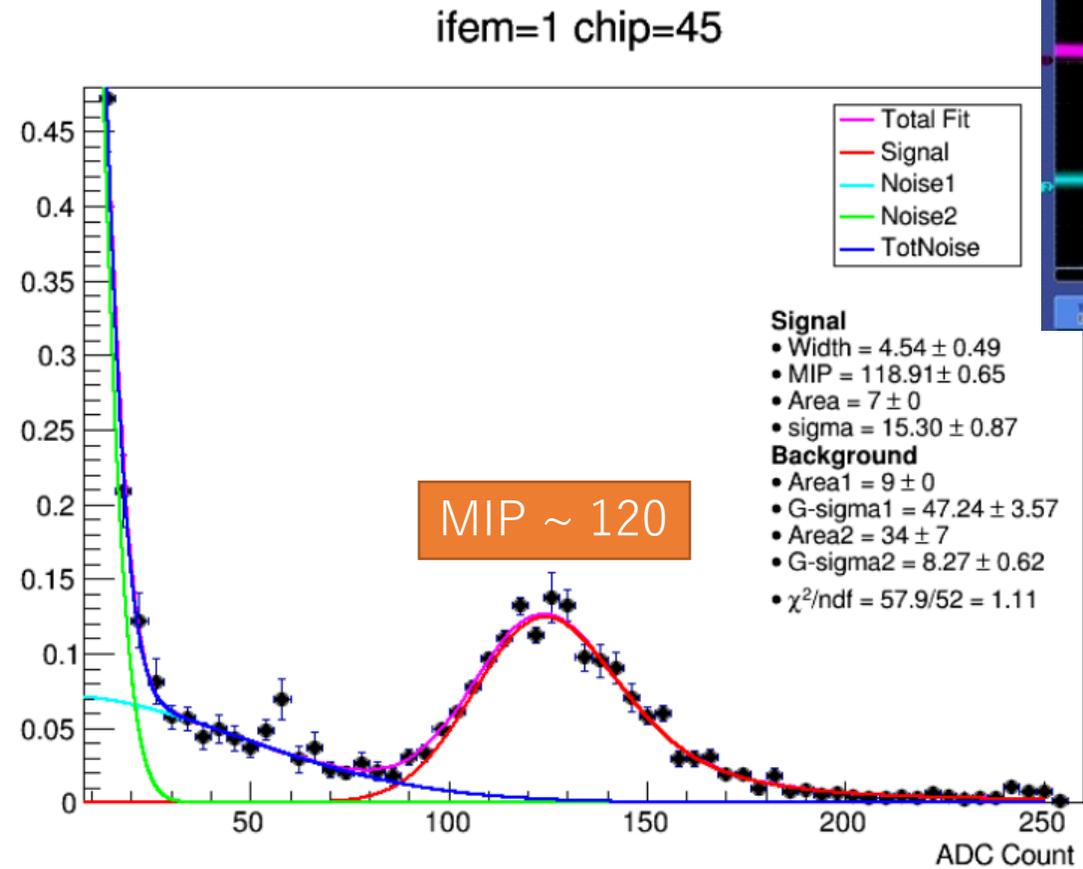


FIGURE 5.24: The energy deposit distributions of testbeam 2019.

The calibration pulse is not sufficiently large to cover MIP signal size. On the other hand, there is no reason to start from DAC0=20 while the beam operation DAC0 starts from 15.

Optimized DAC Setting for INTT Calibration

DAC	Default	New
0	20	15
1	25	19
2	30	23
3	35	27
4	40	31
5	45	35
6	50	39
7	55	43

74 FPHX TestStand DAQ

File

All / D3 | Mod A0 | Mod B0 | Mod C0 | Mod D0 | Mod A1 | Mod B1 | Mod C1 | Mod D1 | Mod A2 | Mod B2 | Mod C2 | Mod D2 | Mod A3 | Mod B3 | Mod C3

Reg	Desc	To Chip	From Chip	Chip Command				
*	Wild	0		Read	Write	Set255	Reset	Default
1	Mask	0		Read	Write	Set255	Reset	Default
2	Dig Ctrl	5		Read	Write	Set255	Reset	Default
3	Vref	1		Read	Write	Set255	Reset	Default
4	DAC0	20		Read	Write	Set255	Reset	Default
5	DAC1	25		Read	Write	Set255	Reset	Default
6	DAC2	30		Read	Write	Set255	Reset	Default
7	DAC3	35		Read	Write	Set255	Reset	Default
8	DAC4	40		Read	Write	Set255	Reset	Default
9	DAC5	45		Read	Write	Set255	Reset	Default
10	DAC6	50		Read	Write	Set255	Reset	Default
11	DAC7	55		Read	Write	Set255	Reset	Default
12	NTSel <3:0>	6		Read	Write	Set255	Reset	Default
	N2Sel <7:4>	4						
13	FB1Sel <3:0>	4		Read	Write	Set255	Reset	Default
	LeakSel <7:4>	0						
14	P3Sel <1:0>	0		Read	Write	Set255	Reset	Default
	P2Sel <7:4>	4						
15	GSel <2:0>	2		Read	Write	Set255	Reset	Default
	BWSel <7:3>	8						
16	P1Sel <2:0>	5		Read	Write	Set255	Reset	Default
	InjSel <5:3>	0						
17	LVDS Current	3		Read	Write	Set255	Reset	Default
18	Resets	n/a		Read	Write	Set255	Reset	Default

Chip Control
Display/Modify Configuration for Chip ID 21 Side 15

Channel Mask [Red = Off, Green = On]

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127

Mask All Unmask All Toggle All Send

Chip Side Enable

0	15	0	1	8	15	0	1	16	15	0	1	24	15	0	1
1	15	0	1	9	15	0	1	17	15	0	1	25	15	0	1
2	15	0	1	10	15	0	1	18	15	0	1	26	15	0	1
3	15	0	1	11	15	0	1	19	15	0	1	27	15	0	1
4	15	0	1	12	15	0	1	20	15	0	1	28	15	0	1
5	15	0	1	13	15	0	1	21	15	0	1	29	15	0	1
6	15	0	1	14	15	0	1	22	15	0	1	30	15	0	1
7	15	0	1	15	15	0	1	23	15	0	1	31	15	0	1

TestStand

Spartan3 ROC ROC+FEM FEM Addr 15 DB Access On Off

Global Chip/DAQ Operations

FFR	Enable RO	Latch FPGA	Core Reset	Start DAQ	Check GLINK	test
Init	Disable RO	Calib	JTAG Sync	Stop DAQ	Check FEM	Mask
FO Sync	Set L1	Delay 5	BCO Start	Global Start	Self Trig	DAC
FPGA RST	Er. EEPROM	Write Page	Read Page	Write All	Cosmic Start	Loop

DAQ Configuration

DAQ Program C:/Users/RIKEN_INTT/D Browse

NI DAQ Sample Rate (MHz) 5

Num of events (0==inf) 0

Duration HH:MM:SS (0:00:00==inf) HH:MM:SS

Print Output Print Off

FPHX version (for Print) 2

Run Number

Filename

Beam Species None

Beam Energy 0

Pulsar Configuration

Pulse amplitude (10 bits max) 255 Config Amp Pulse

Num of Pulses 1 Pulse Train

BCOs between pulses 1023 Wedge 0 Module 0 Set Module

Module Enable

Module 15 On Off Both Side 0 Side 1 Module 7 On Off Both Side 0 Side 1

Module 0 On Off Both Side 0 Side 1 Module 8 On Off Both Side 0 Side 1

Module 1 On Off Both Side 0 Side 1 Module 9 On Off Both Side 0 Side 1

Module 2 On Off Both Side 0 Side 1 Module 10 On Off Both Side 0 Side 1

Module 3 On Off Both Side 0 Side 1 Module 11 On Off Both Side 0 Side 1

Module 4 On Off Both Side 0 Side 1 Module 12 On Off Both Side 0 Side 1

Module 5 On Off Both Side 0 Side 1 Module 13 On Off Both Side 0 Side 1

Module 6 On Off Both Side 0 Side 1 Module 14 On Off Both Side 0 Side 1

Manual Packet Send

Packet file to send Browse Send Read

Communications

USB None Ethernet IP Addr 192.168.60.2 Port 9900

Baud Rate 115200

ver7

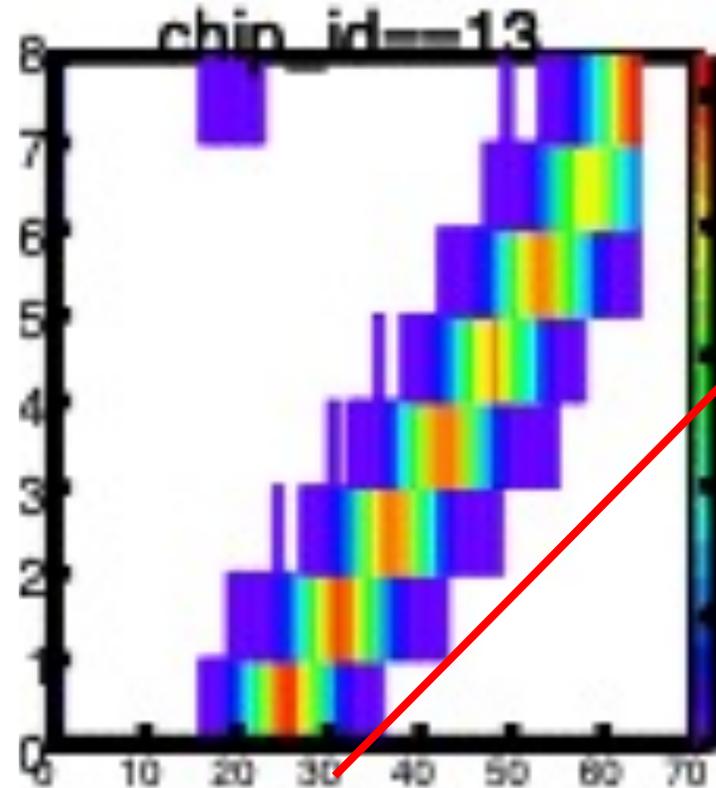
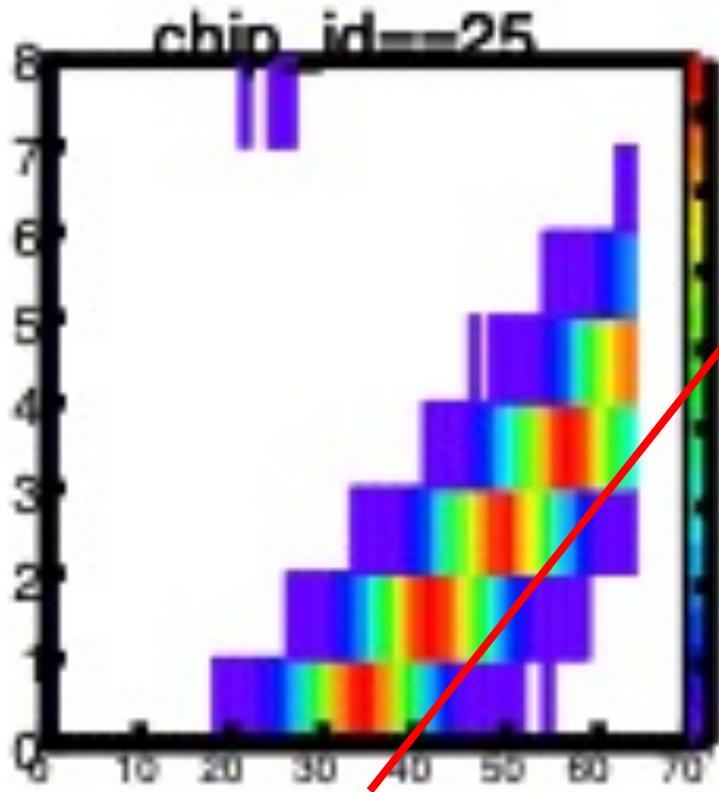
ROOT Module ID 6 Calib External camac ROOT_imp

New DAC Setting Result

FVTX

INTT+ μ -Coax

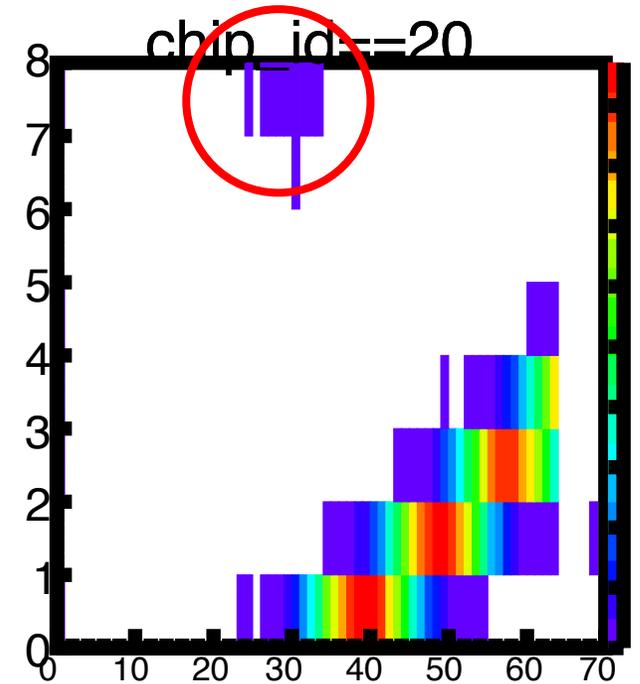
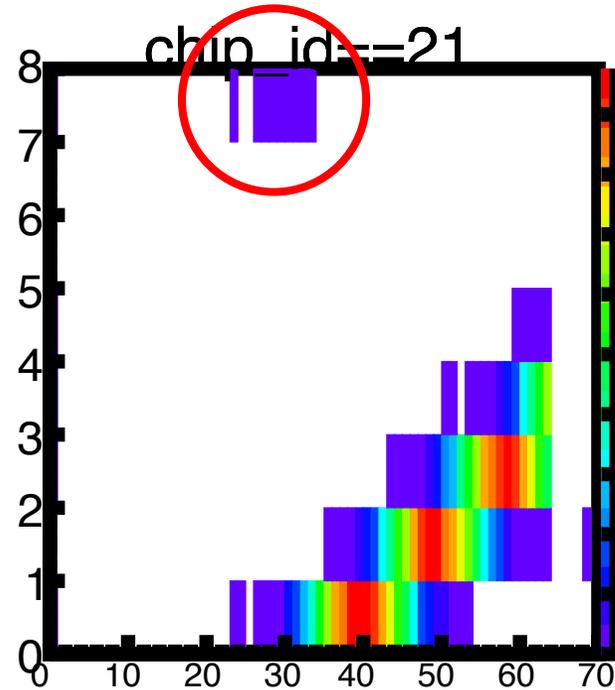
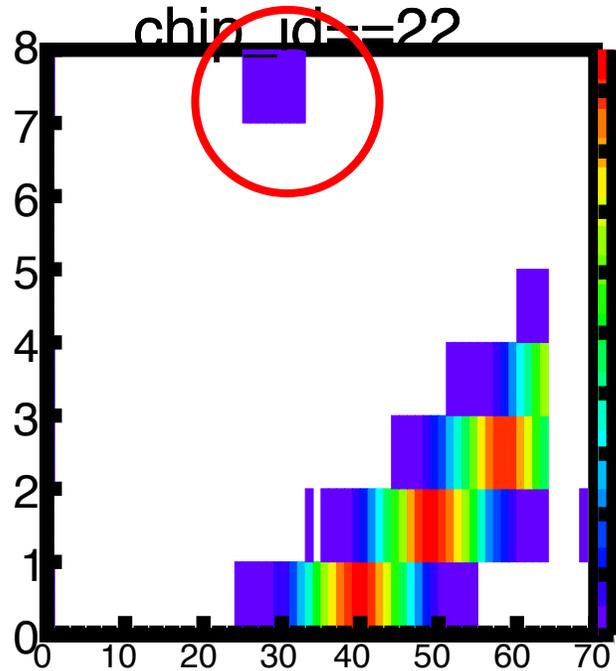
INTT+BEX+ μ -Coax



Measurements by Rikkyo Undergraduates

Mysterious ADC=7 Entry

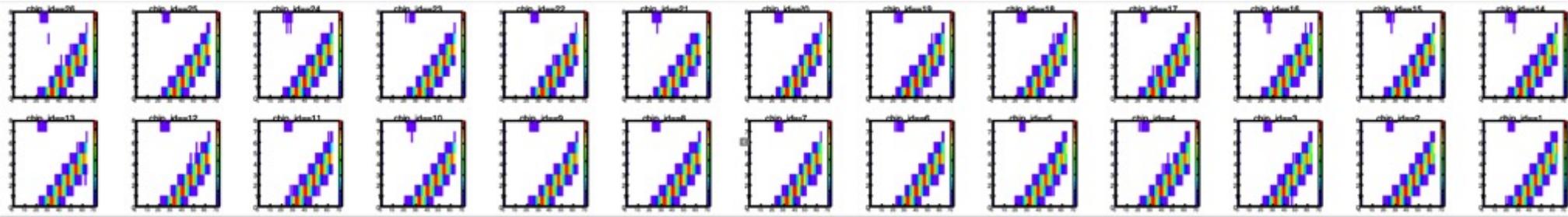
ADC=7 Entry



We have been observing <10 entries in $\text{ADC}=7$ around $\text{amp}=30$. The origin of these entries have never been investigated.

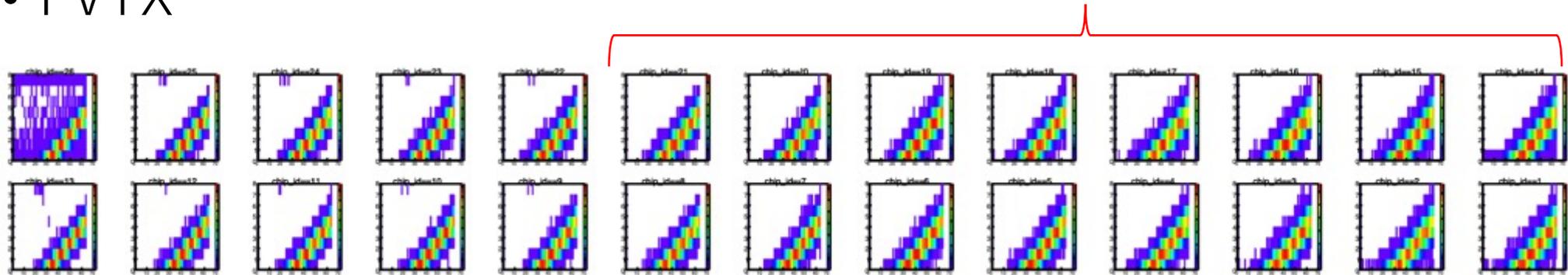
FVTX Calibration

- INTT+ μ -coax



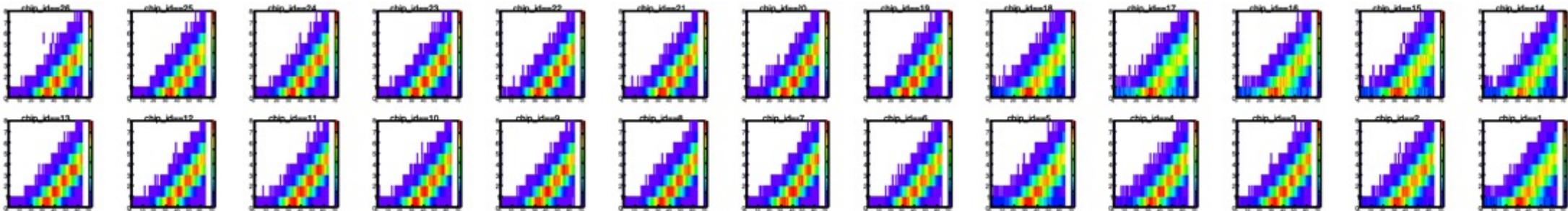
- FVTX

No entry in ADC=7 around amp=30 in FVTX in these chips



Without Bias

- INTT + μ -coax without Bias



Somehow ADC=7, amp~30 entries are gone without bias.

Will investigate more.