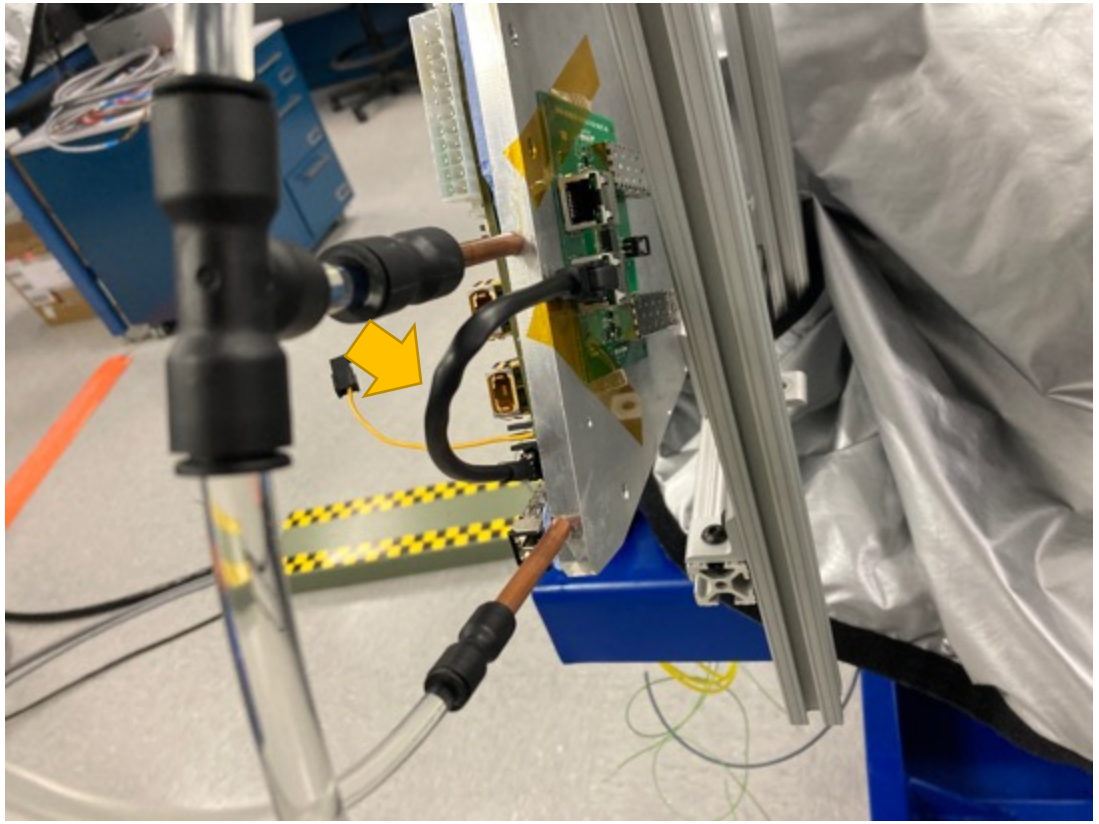
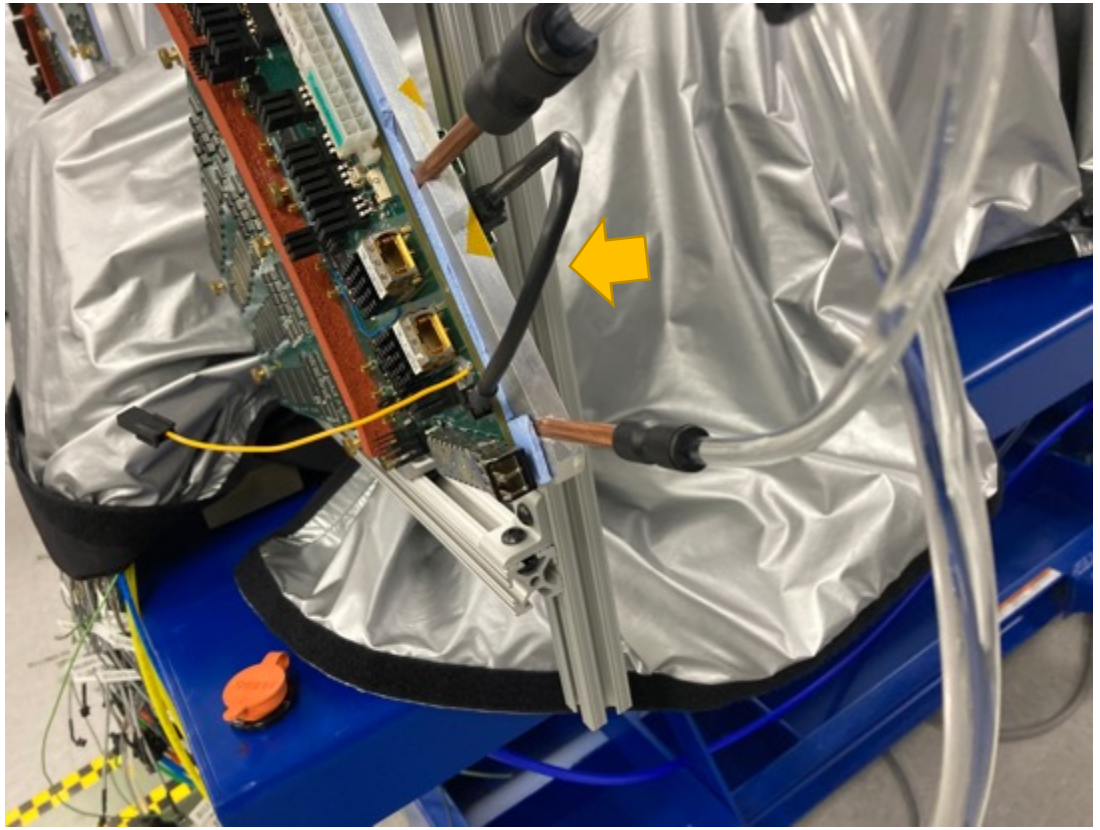
Short Term Plan

RIKEN/RBRC

Itaru Nakagawa

Production Beam Clock Cable





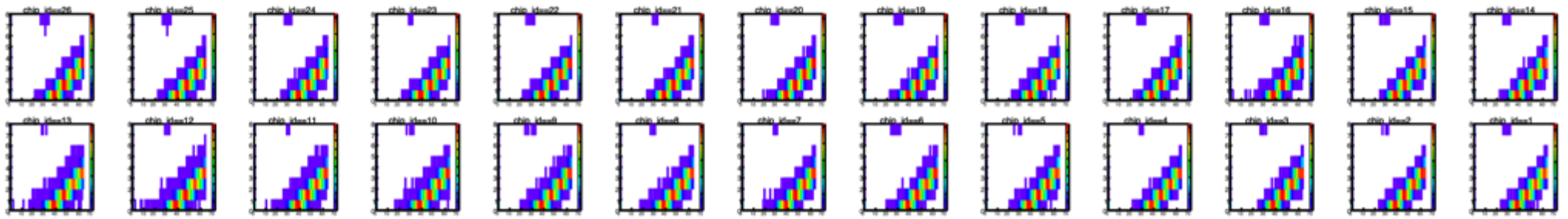
Some minor stress is there at the connector in ROC side though, the connector won't pop-out right away. Leave this cable for a while to monitor. We'll look into details next Tuesday with Dan and Rachid.

RCDAQ

- May 26, 2022 sPHENIX Summer School
  - Martin's slide : https://indico.bnl.gov/event/15547/
- RCDAQ documentation:
  - https://www.phenix.bnl.gov/~purschke/rcdaq/rcdaq_doc.pdf

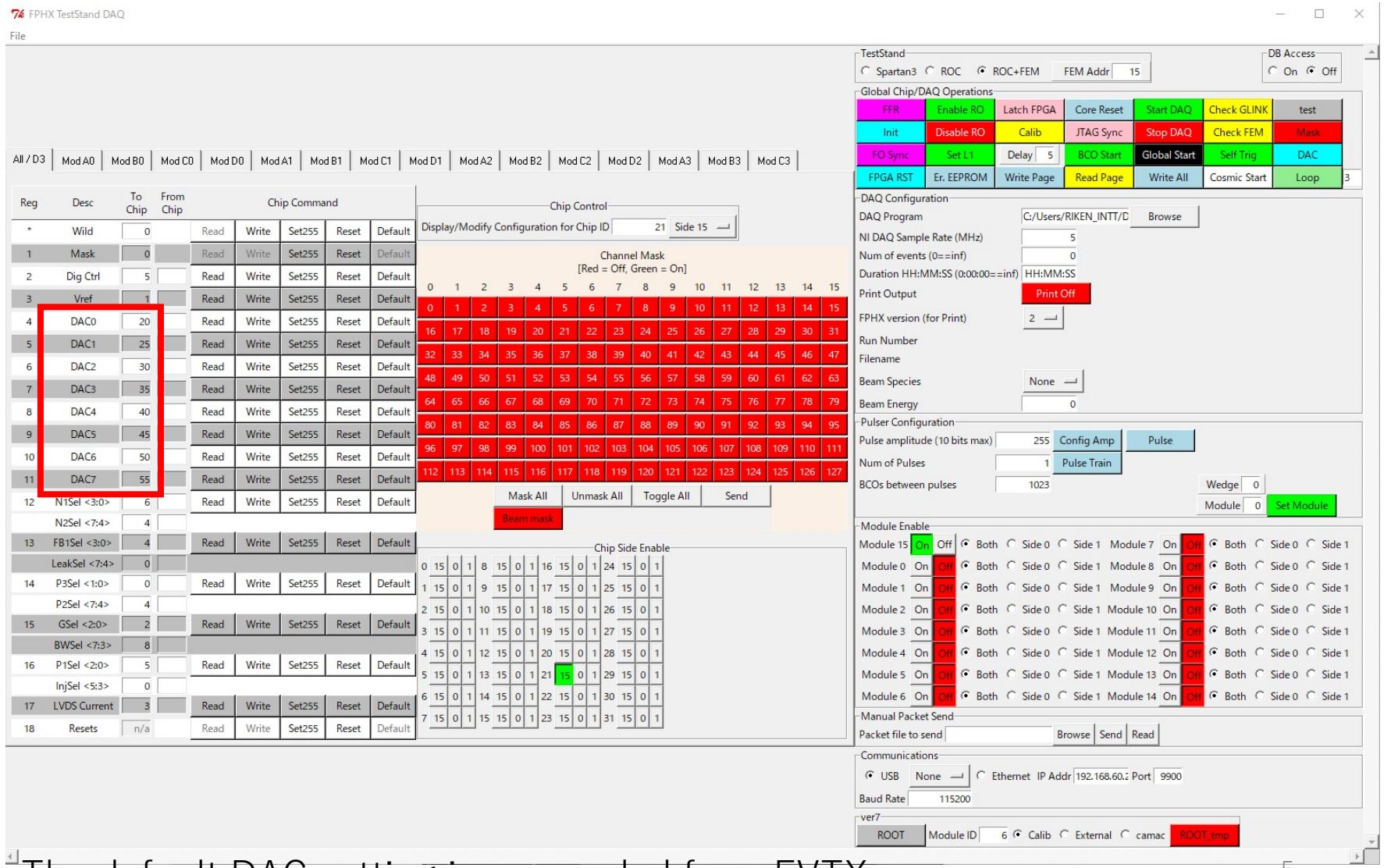
Will have a discussion with Martin in the afternoon next Wednesday.

Optimization of the DAC Setting for Calibration



DAC Setting for the calibration

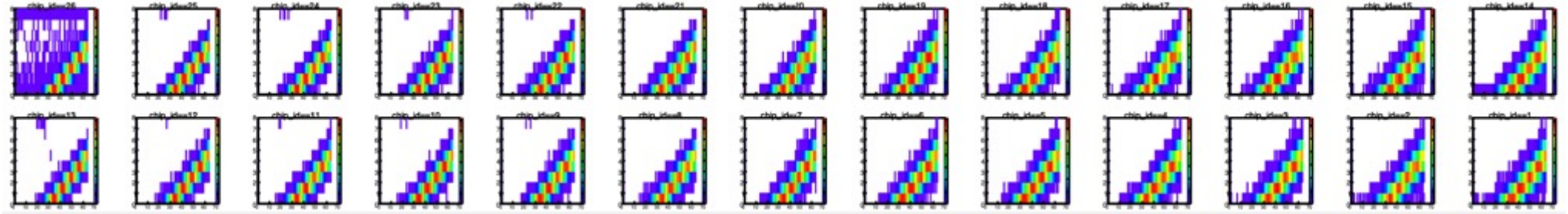
ADC	Calib
0	20
1	25
2	30
3	35
4	40
5	45
6	50
7	55



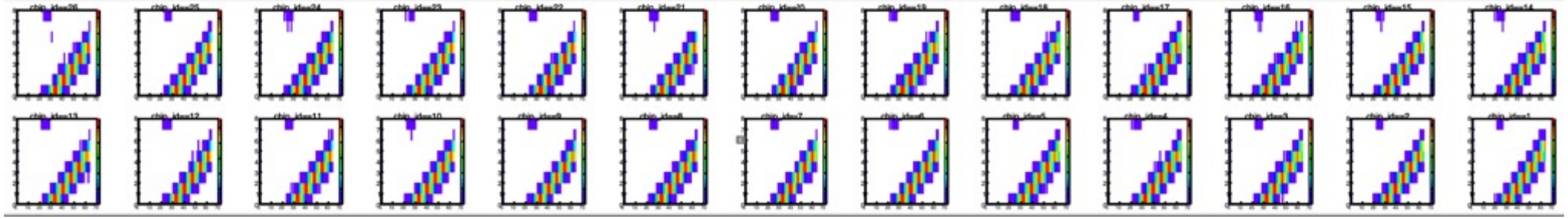
The default DAC setting is succeeded from FVTX.

Calibration Result Comparison

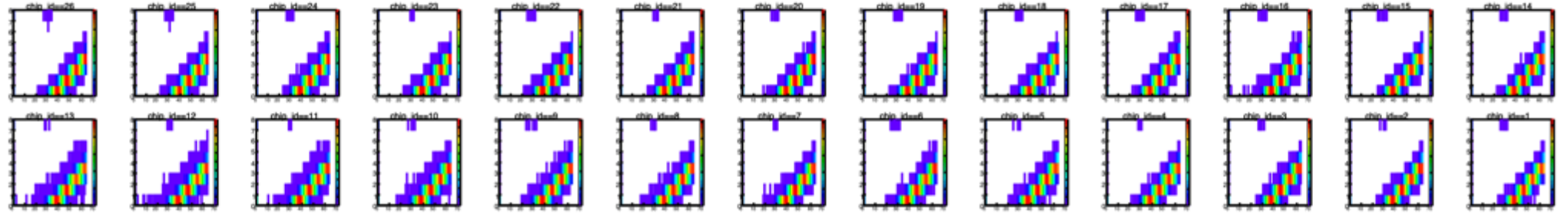
- FVTX



- INTT+μ-coax Cable

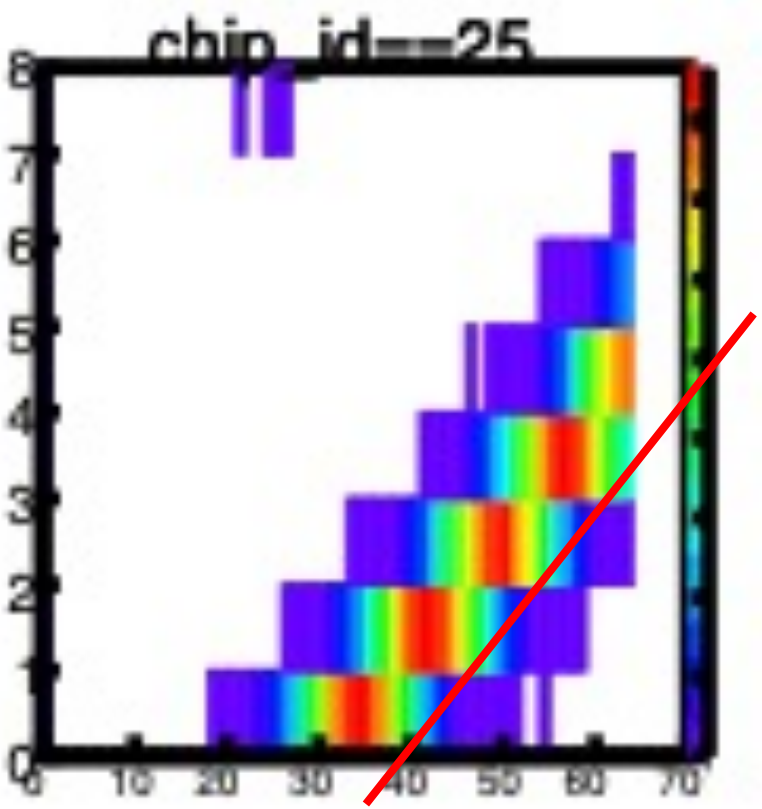


- INTT + BEX +μ-coax Cable

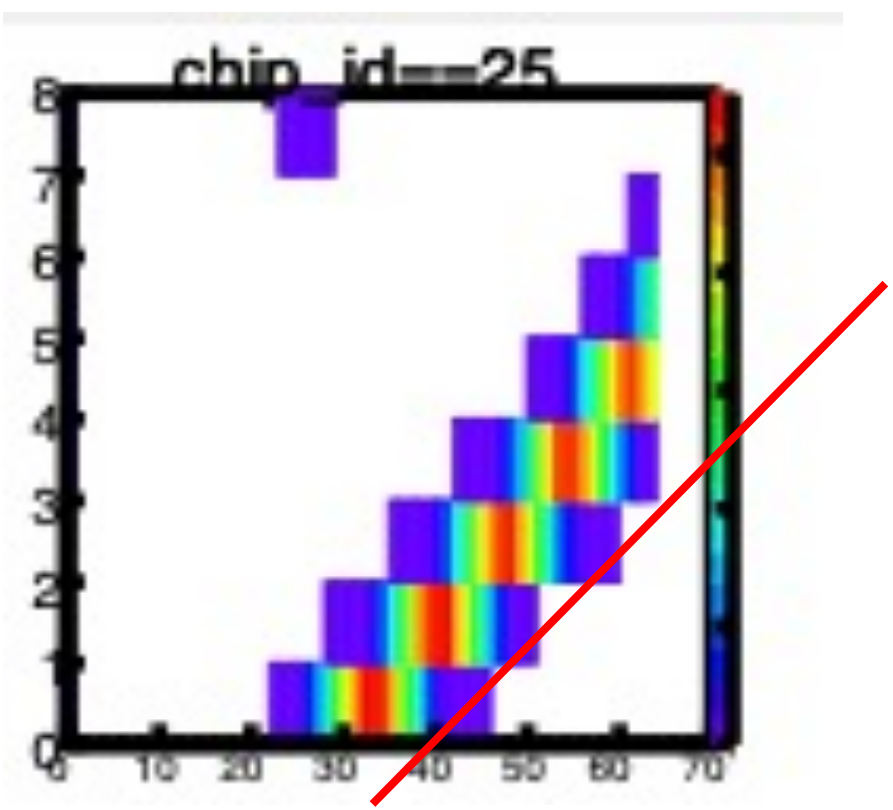


Default DAC Setting Result

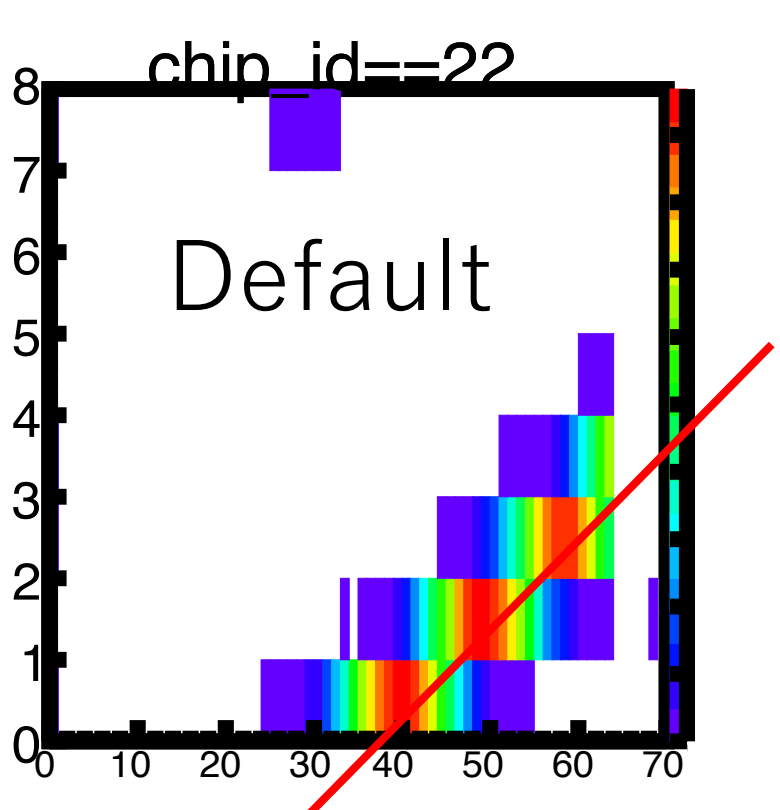
FVTX



INTT+μ-Coax



INTT+BEX+μ-Coax



Due to long readout cable path of INTT system, the calibration pulse height is reduced in the long path before it reaches to FPHX chip. Thus we are pulsing only DAC0~DAC4 or 5 in INTT+BEX+ μ-Coax setup. We should reconsider optimized DAC setting for the INTT.

Optimization of Calib DAC setting

DAC	Calib	Beam Test
0	20	**15**
1	25	30
2	30	60
3	35	90
4	40	**120**
5	45	150
6	50	180
7	55	210

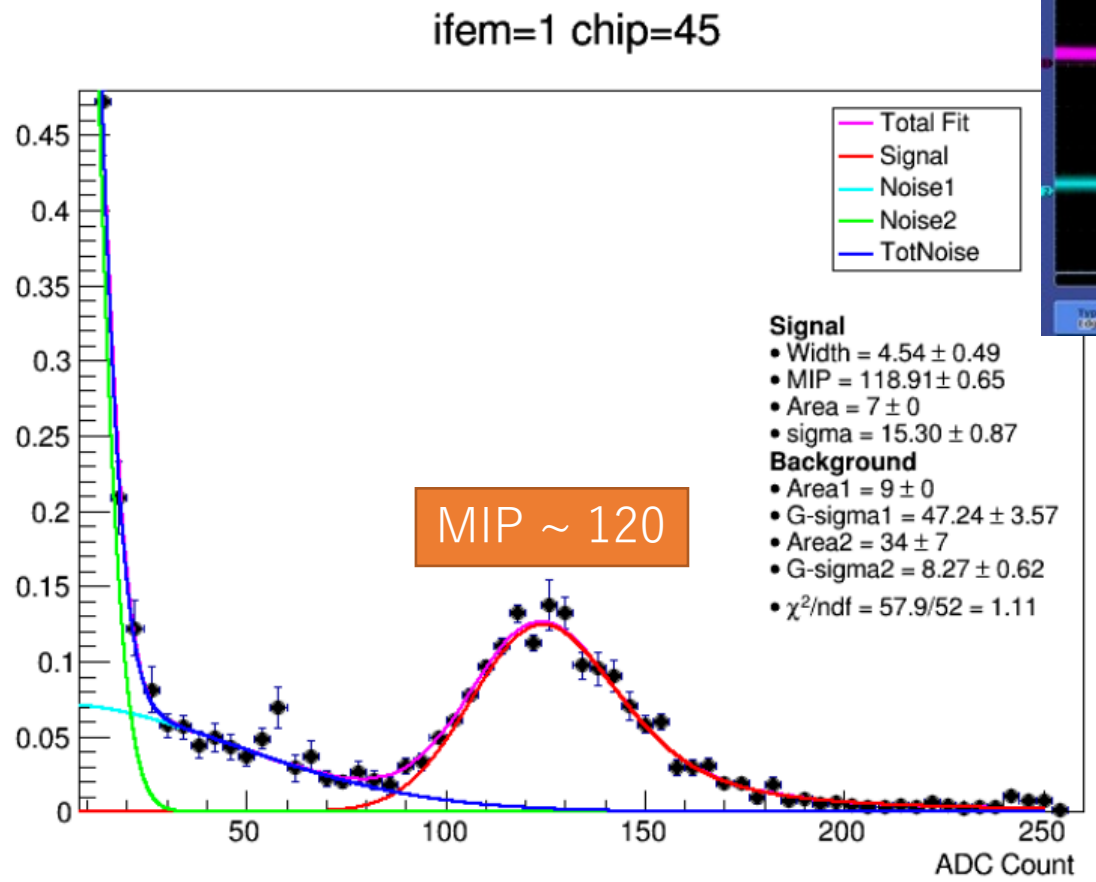
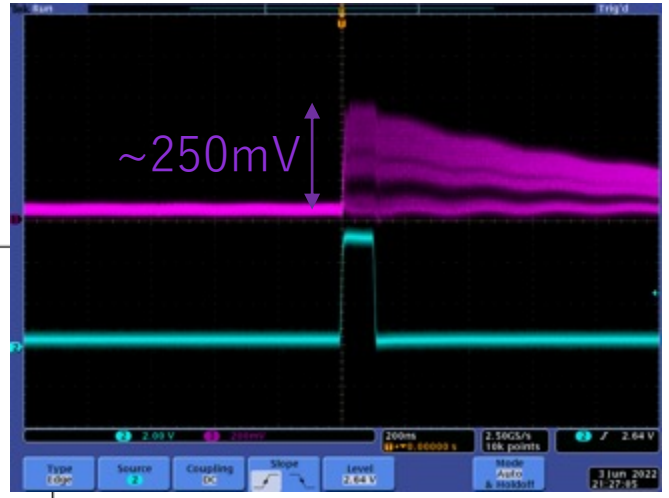


FIGURE 5.24: The energy deposit distributions of testbeam 2019.

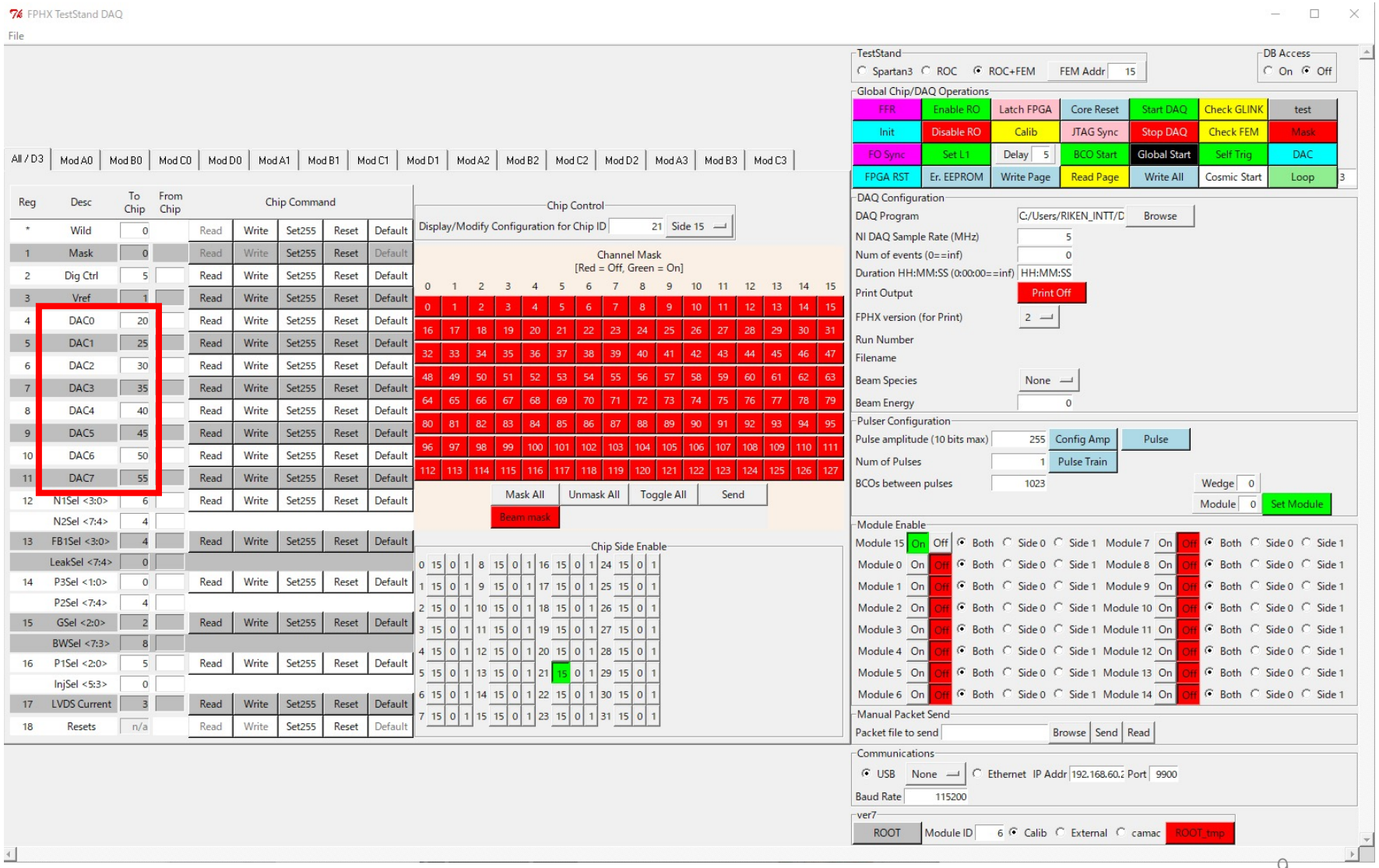
Calibration Pulse @ ROC



The calibration pulse is not sufficiently large to cover MIP signal size. On the other hand, there is no reason to start from DAC0=20 while the beam operation DAC0 starts from 15.

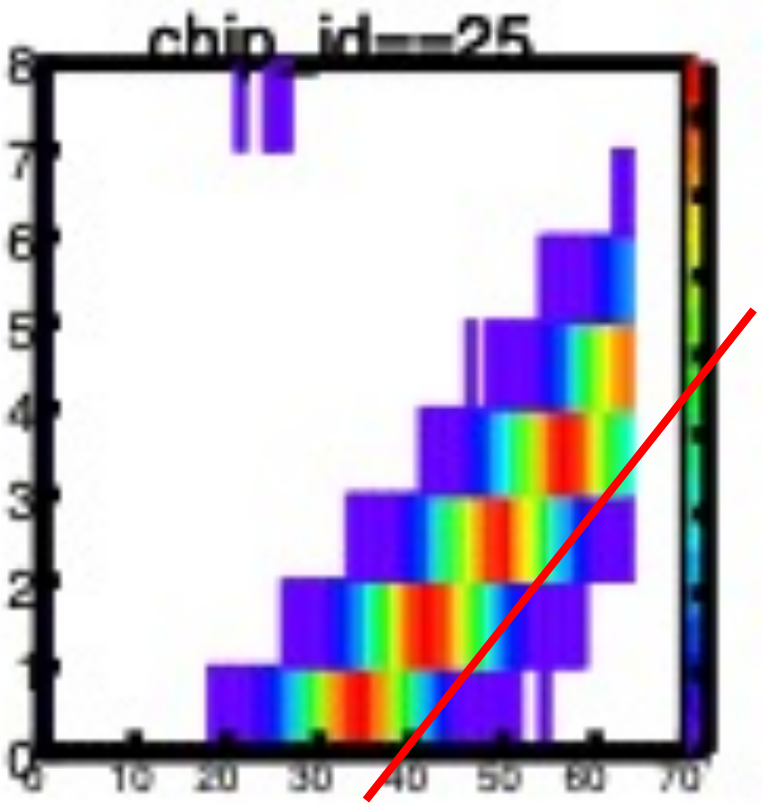
Optimized DAC Setting for INTT Calibration

DAC	Default	New
0	20	15
1	25	19
2	30	23
3	35	27
4	40	31
5	45	35
6	50	39
7	55	43

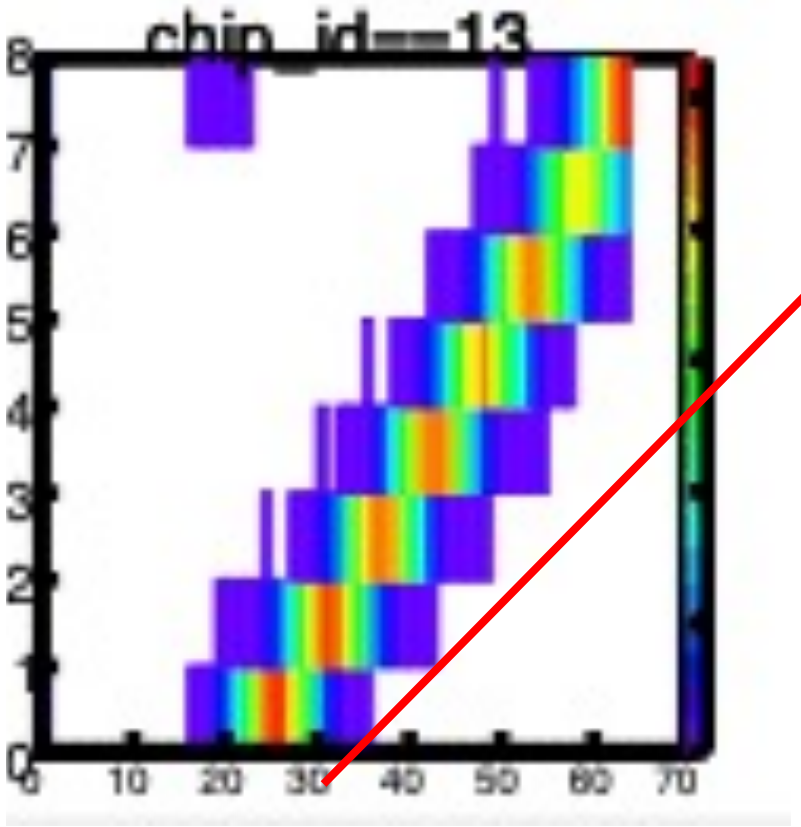


New DAC Setting Result

FVTX



INTT+μ-Coax

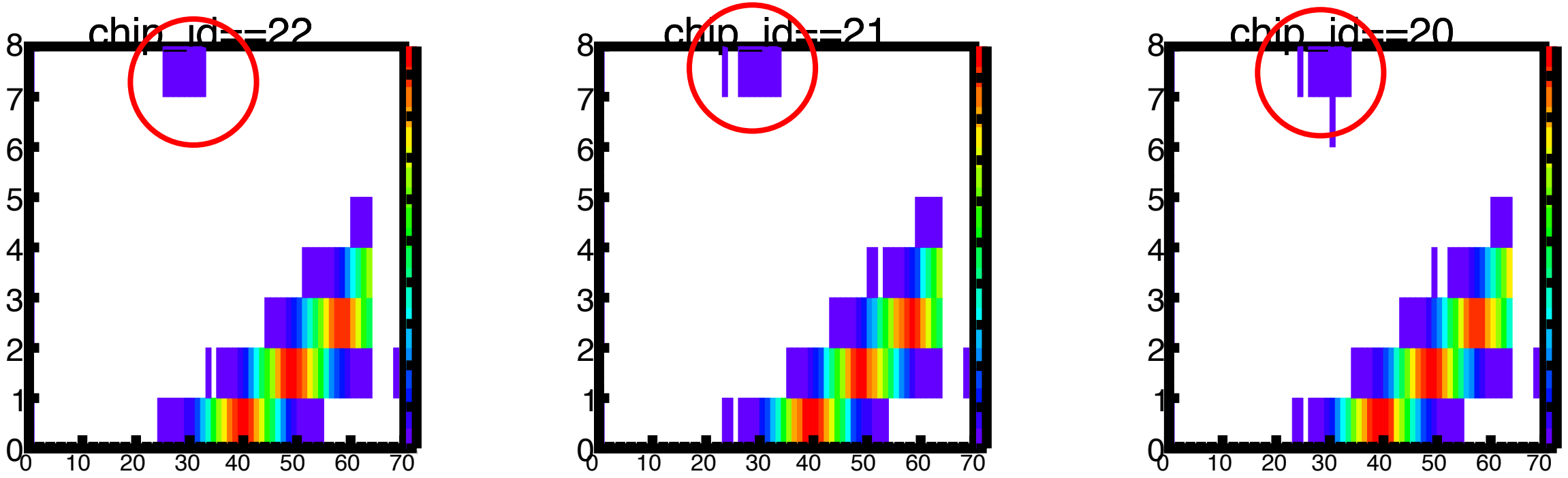


INTT+BEX+μ-Coax

Measurements by Rikkyo Undergraduates

Mysterious ADC=7 Entry

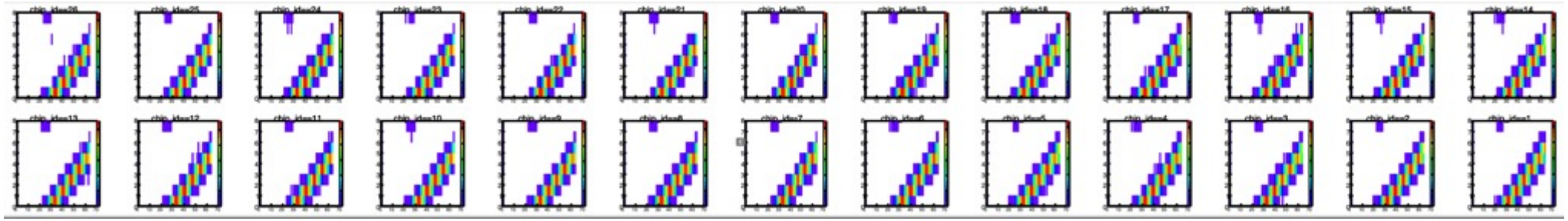
ADC=7 Entry



We have been observing <10 entries in ADC=7 around amp==30. The origin of these entries have never been investigated.

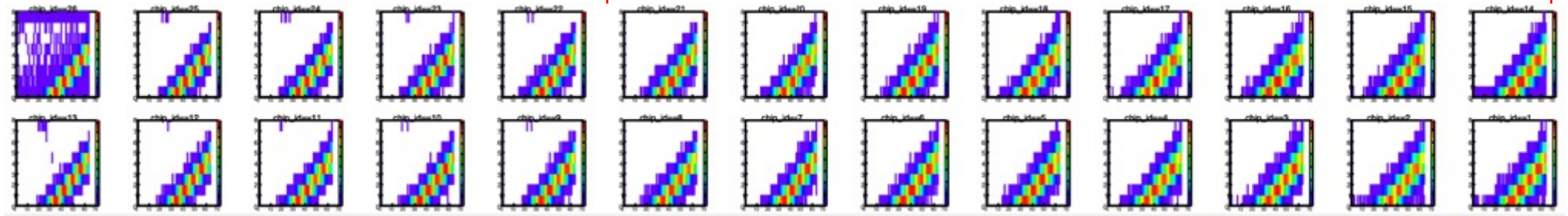
FVTX Calibration

- INTT+μ-coax



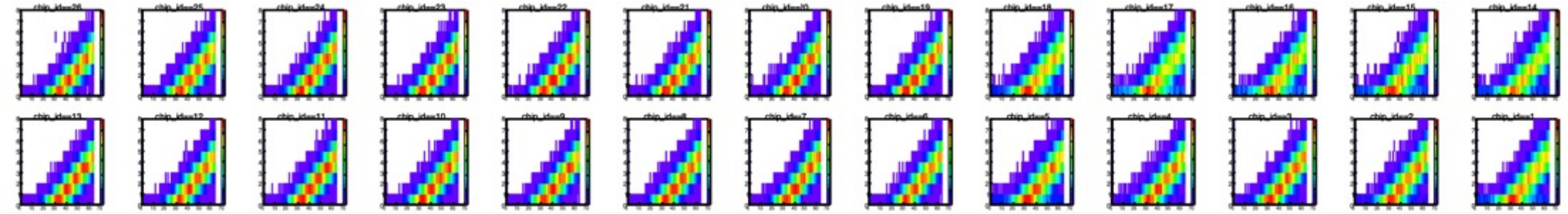
- FVTX

No entry in ADC=7 around amp=30 in FVTX in these chips



Without Bias

- INTT + μ-coax without Bias



Somehow ADC=7, amp~30 entries are gone without bias.

Will investigate more.