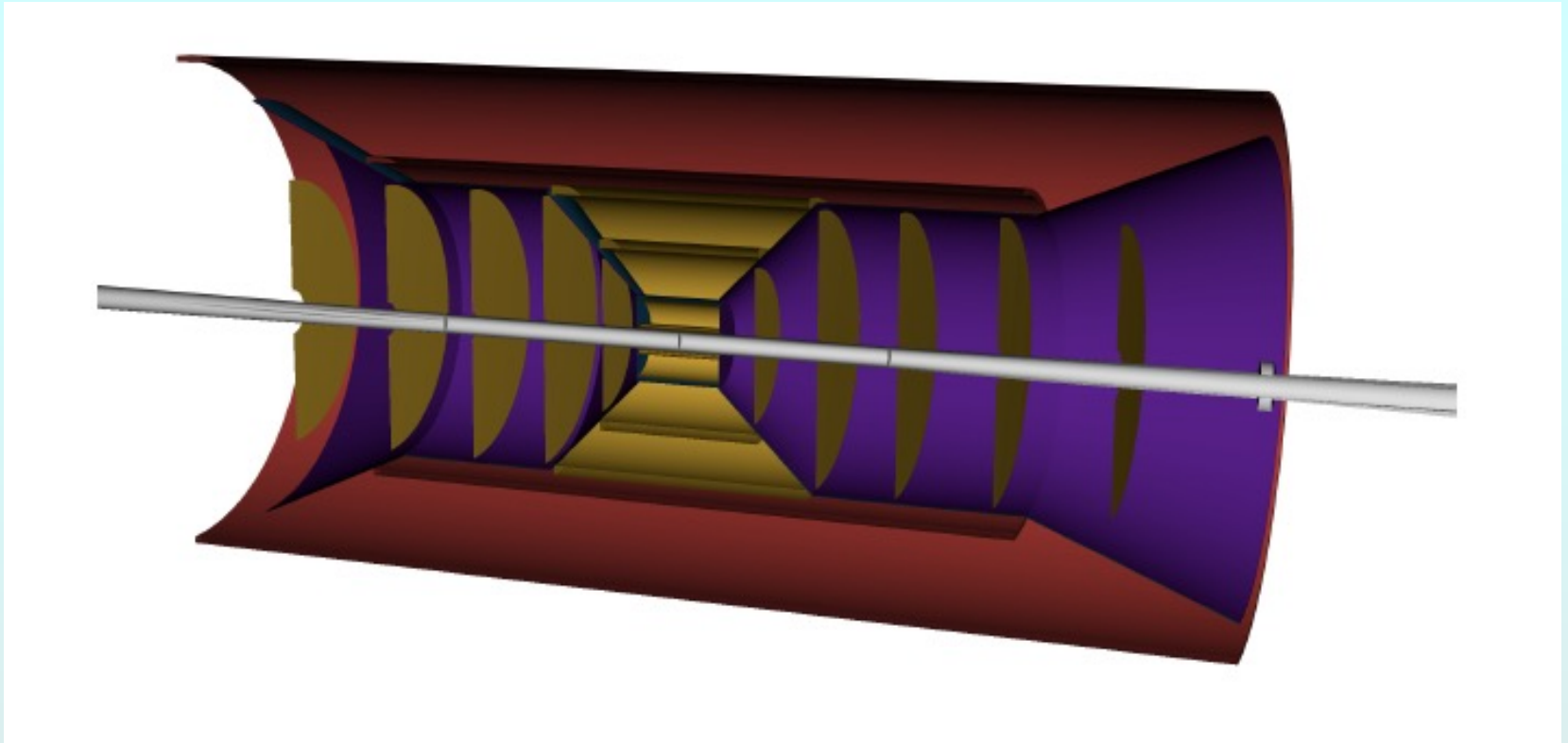


Towards Construction



Berkeley

*Barbara Jacak &
Ernst Sichtermann
UC Berkeley + LBNL
Oct. 10, 2022*



A silicon tracker needs:

Barrel tracker & Endcap discs each need:

- sensors (vertex layers & sagitta layers may differ)

- mechanical design (vertex layers & sagitta layers will differ)

- cooling

- power interface

- cabling strategy

- electrical integration (Flex PCB, power gen config, etc. to end of staves/discs)

Overall mechanical support & integration of subsystems

Services (cooling, power cables, RDO/config cables)

- barrel (vertex & tracker layers the same?); disks

Readout electronics (no FEE as this is built into MAPS)

Interlocks

Slow controls & run control interface (usually these are a separate subsystem)

Power distribution system

DAQ interface

Each sub-system (vertex, sagitta/stave, disc) will have its own assembly structure

We know

- **Silicon barrel layout**
 - Should still investigate option of outer silicon layer
- **Basic endcap disk positions**
 - Some optimization still underway
 - Sensor tiling strategy being actively investigated
 - ITS2 stave structure is a starting point
 - Bakeout effects need investigation
 - Commissioning plan is needed – split assembly?
- **Minimizing material is paramount!**
 - Must optimize mechanical supports & cones
 - Need ultrathin supports for ultrathin sensors
 - Air cooling highly desirable
 - Does it need to be insulated from outside heat sources?
- **Need hermetic acceptance**
 - Integration with beam pipe is complicated

Interests expressed

- **Sensor design**
RAL, BNL, LBNL
- **Sensor assembly & testing**
INFN (Bari, Trieste, Padua), UK, LBNL, LANL, Wuhan, Korean groups?
- **Mechanical support**
 - Vertex layers**
LBNL, INFN(Trieste, Bari, Padua), UK
 - Sagitta layers**
ORNL, LBNL, UK
 - Disks**
LANL, LBNL, UK
- **Cooling**
LBNL, LANL, ORNL
- **Data Cabling**
BNL, ORNL
- **Power distribution**
UK, ORNL, LANL, BNL, JLab?

Interests, continued

- **Readout**
ORNL
- **DAQ interface**
BNL, ORNL
- **Slow controls**
- **Interlocks**
BNL
- **Integration**
JLab, BNL