2022 EIC DAC Meeting on October 19-21, 2022

Indico page: https://indico.bnl.gov/event/17159/

- EIC project update on Oct 19 9:30-10:15am EDT
- Update on EPIC on Oct 19 10:15-11:15am EDT
- eRD112 presentation (20+10') on **Oct 20 10:10-10:40am EDT**
  - open R&D questions to be complete the R&D program before CD-3
  - milestones for FY2022
  - results from FY2022
  - plans/proposals for FY2023.
- eRD109 presentation (20+10') on **Oct 21 10:00-10:30am EDT**
- Close-Out on Oct 21 12:30-13:15pm EDT

EIC R&D Detector Advisory Committee:

Marcel Demarteau (ANL, chair), Carl Haber (LBNL), Ian Shipsey (Oxford), Rick VanBerg (Penn), Jerry Va'vra (SLAC), Glenn Young (JLab), Peter Krizan (University of Ljubljana, Ljubljana), Blair N. Ratcliff (SLAC)

EIC AC-LGAD R&D FY22 Report and FY23 Proposal

Brookhaven National Laboratory: E.C. Aschenauer, G. Giacomini, A. Jentsch, A. Kiselev, P. Shanmuganathan, P. Tribedy, A. Tricolli, T. Ljubicic, Z. Xu
Fermi National Accelerator Laboratory: A. Apresyan, R. E. Heller, C. Madrid, C. Pena, S. Xie, T. Zimmerman
Los Alamos National Laboratory: Xuan Li
Oak Ridge National Laboratory: O. Hartbrich, K. F. Read, C. Loizides
Purdue University: A. Jung
Rice University: Frank Geurts, Wei Li
University of California, Santa Cruz: S. Mazza, J. Ott, A. Seiden, S.H. Sadrozinski, B. Schumm
University of Illinois at Chicago: Olga Evdokimov, Shirsendu Nanda, Zhenyu Ye
IJCLAB/OEMGA/CEA Irfu (France): R. Dupré, D. Marchand, C. Munoz Camacho, L. Serin, C. de La Taille, M. Morenas
National Cheng Kung University/Academia Sinica (Taiwan): P.-J. Lin, Y. Yang

Institutions have expressed interests and plan to join future efforts:
Massachusetts Institute of Technology, Ohio State University
National Institute of Science Education and Research (India)
Hiroshima University (Japan), Nara Women's University (Japan), RIKEN (Japan)
South China Normal University, University of Science and Technology of China (China)

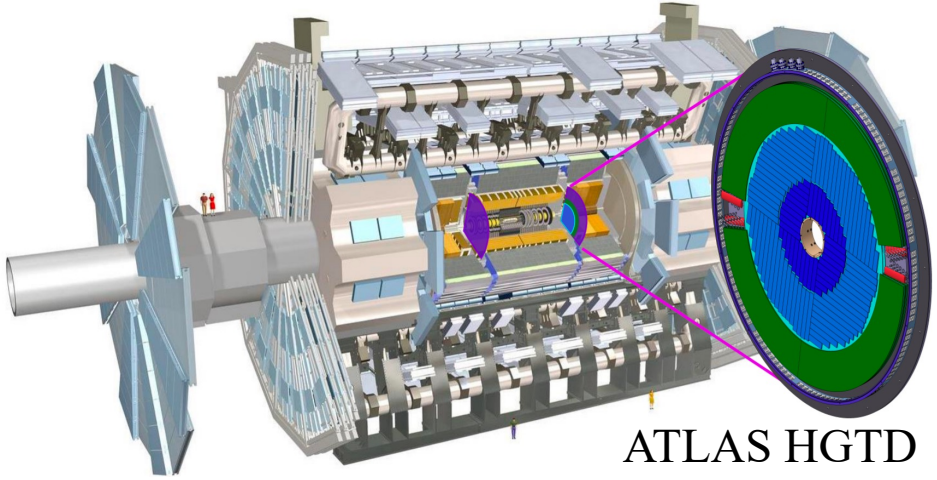
AC-Coupled LGAD Technology

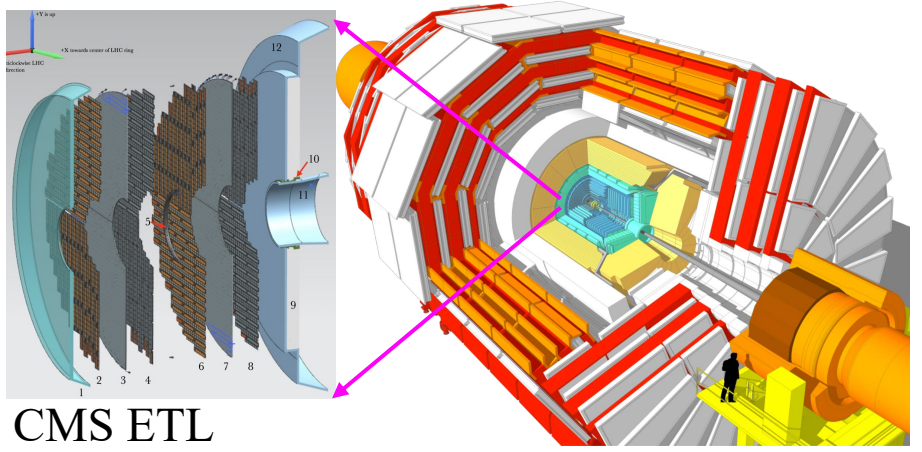
- Precise timing detectors based on DC-LGAD being built by ATLAS (6.4 m^2) and CMS (14 m^2) for data taking in 2028+.

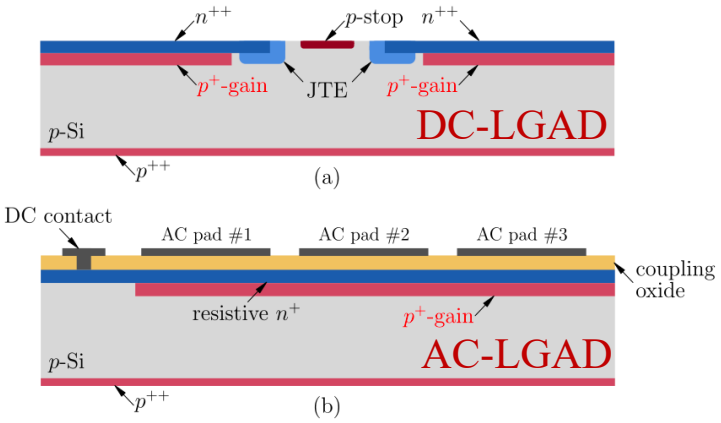
- AC-LGAD can not only provide precise timing resolution similar to DC-LGAD, but also 100% fill factor and much better spatial resolution thanks to charge sharing.

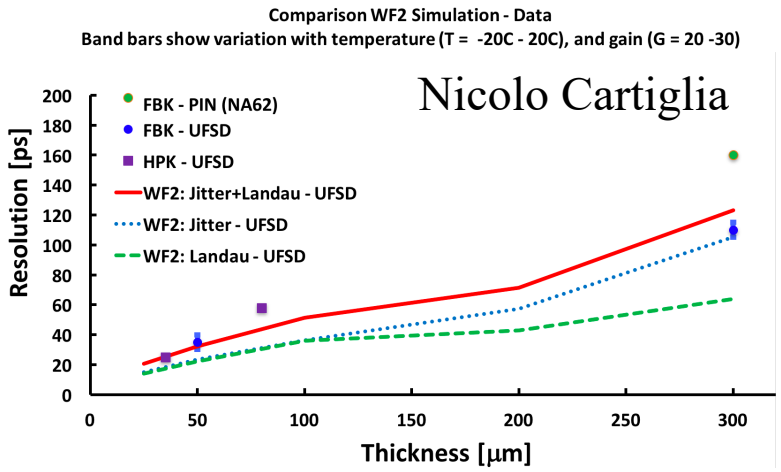
- AC-LGAD proposed for EIC experiments
  - TOF PID and tracking for central detectors
  - timing and tracking for forward detectors

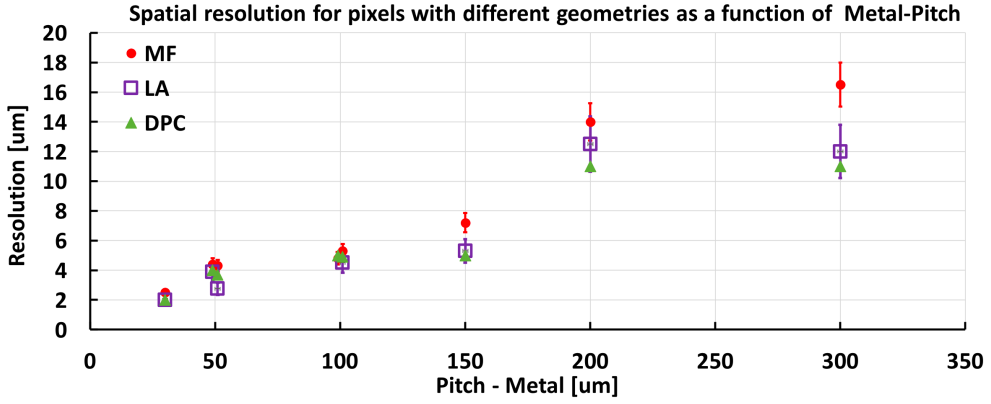
  with common designs in sensor, ASIC etc. where possible.



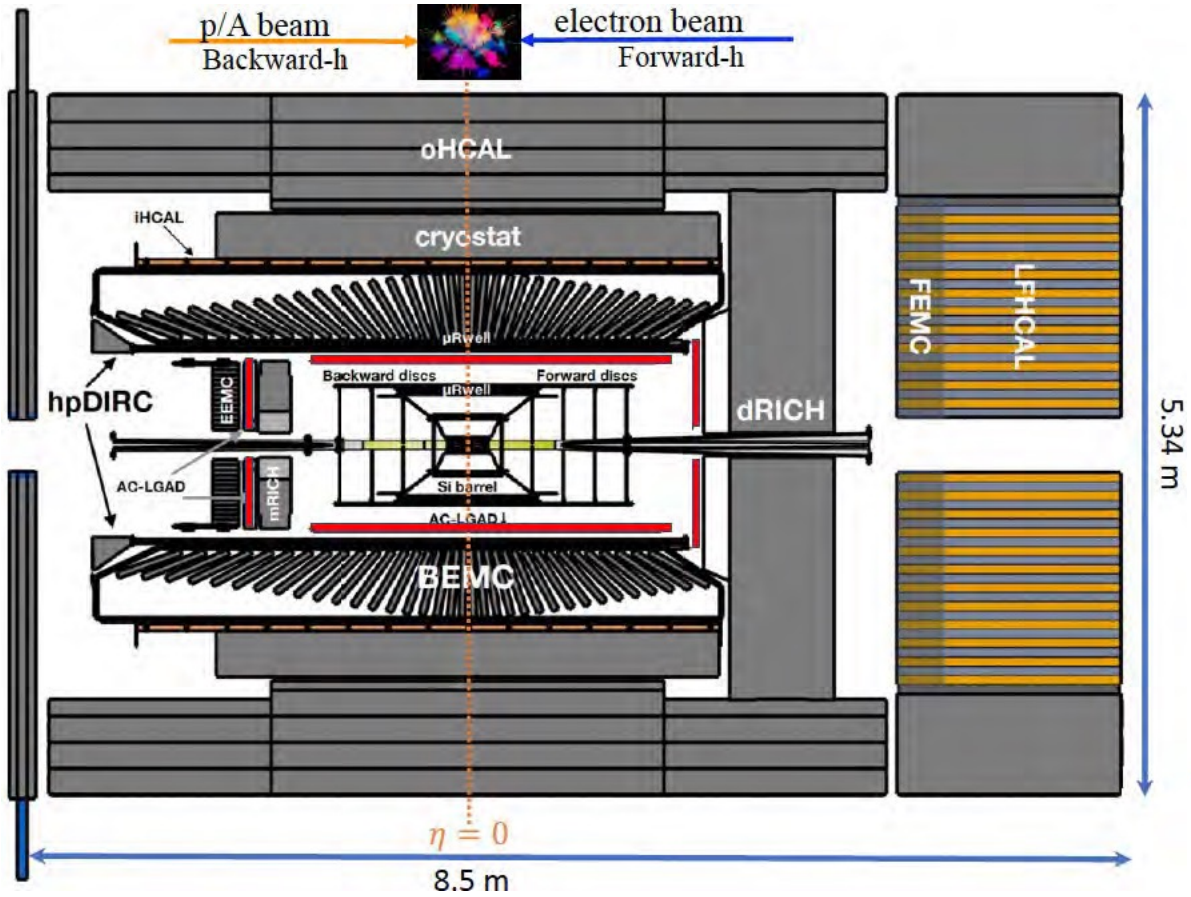


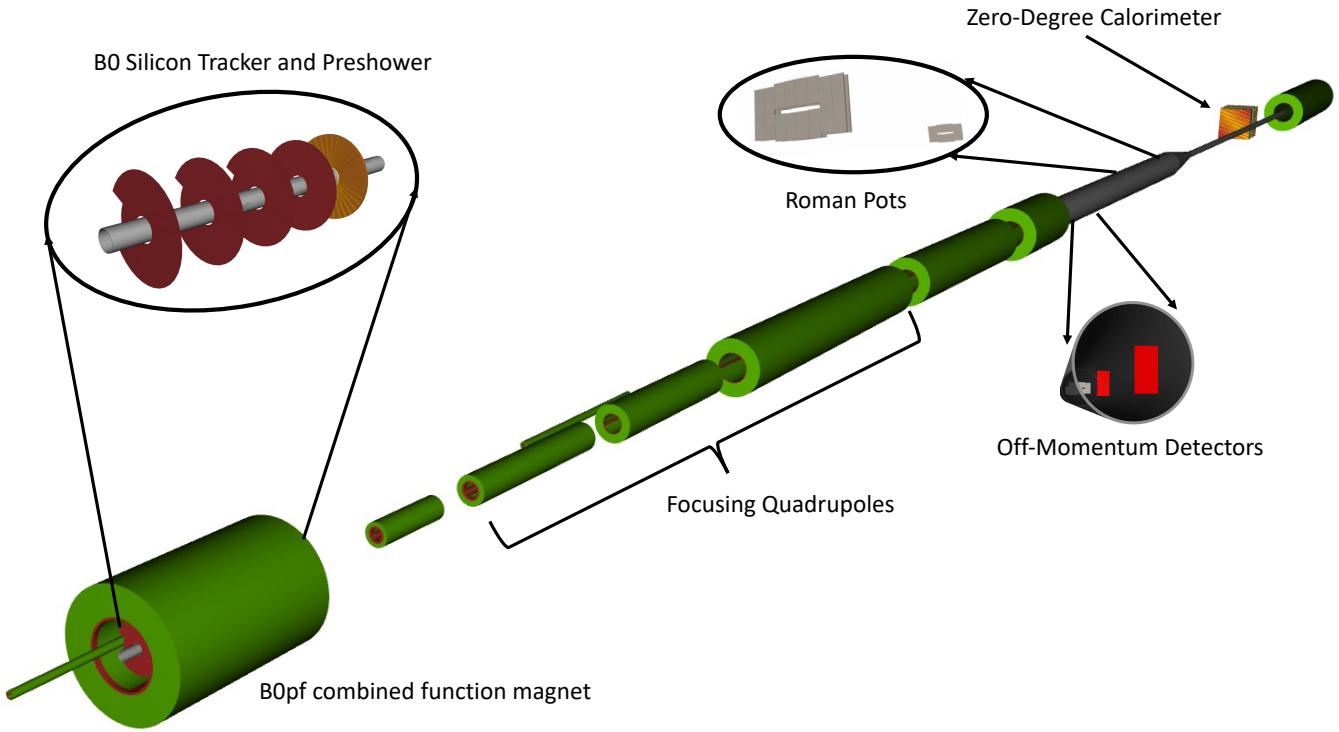






AC-LGAD Detectors for EPIC





	Area (m^2)	Time resolution	Spatial resolution	Material budget
Barrel Timing Tracking Layer	11	30 ps	30 μm in $r \cdot \phi$	0.01 X_0
Endcap Timing Tracking Layers	1.2+2.2	25 ps	30 μm in x and y	0.08 X_0
B0 Tracker	0.07	30 ps	$500/\sqrt{12}$ μm	0.01 X_0
Roman Pots	0.14	30 ps	$500/\sqrt{12}$ μm	no strict req.
Off-Momentum Detectors	0.08	30 ps	$500/\sqrt{12}$ μm	no strict req.

Table 1: Specifications of AC-LGAD detectors for EPIC, the EIC project detector. The timing and spatial resolutions are given for single hits, while the material budgets are given per detector layer.

Requirements on the timing and spatial resolutions and material budget are still being evaluated and are subject to changes as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

Open R&D questions to be addressed before CD-3

- **AC-LGAD sensor:**
  - Goal: large area sensors that meet timing/spatial resolution requirements with minimal # channels
  - Approach: utilize BNL IO to optimize the sensor design (pitch, electrode width, n-layer doping density, active volume thickness); engage commercial vendors to verify sensor quality and production cost/yield.
- **Frontend readout ASIC:**
  - Goal: low jitter (15-20ps) and low power (1 mW/channel), streaming readout with TDC and ADC output
  - Approach: custom-designed EICROC and FCFD, ASICs from 3rd party institutions
- **Sensor/ASIC integration**
  - Goal: reliable and cost-effective way to establish connections between sensor/ASIC
  - Approach: bump-bonding, wire-bonding, interposer
- **Mechanical structure with cooling:**
  - Goal: light-weight structure with cooling that meet the material budget, thermal and mechanical requirements
  - Approach: using carbon-fiber composite and PEEK materials with finite element analysis and prototyping
- **Flex and frontend electronics:**
  - Goal: low jitter clock to frontend ASICs (<5 ps), low X_0 flexible PCB distributing power/signal to sensor/ASIC
  - Approach: design a precise clock distribution system with timing chips from the market, design and prototype flexible PCB that meet the requirements; work with EPIC DAQ to define streaming readout scheme

FY22 Deliverables in FY22 Proposal

- High-level strawman layout design and requirements for sub-systems using AC LGADs.

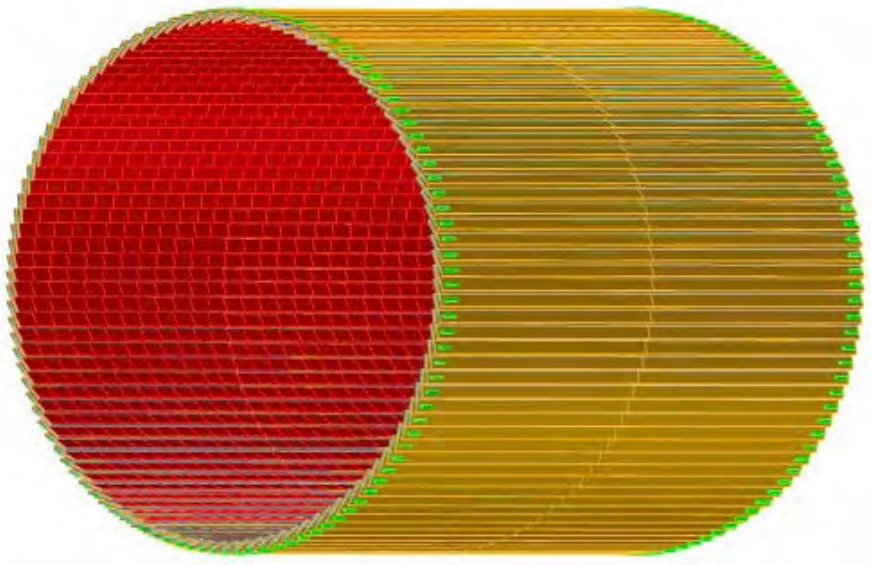
- Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes to optimize performance by BNL Instrumentation and HPK.

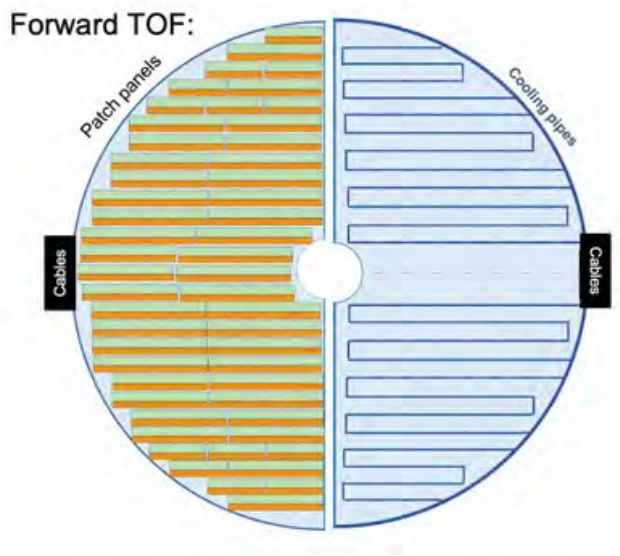
- Start production of sensors of small thickness (20, and 30 microns) for ToF applications with time resolution 20 ps by BNL Instrumentation.

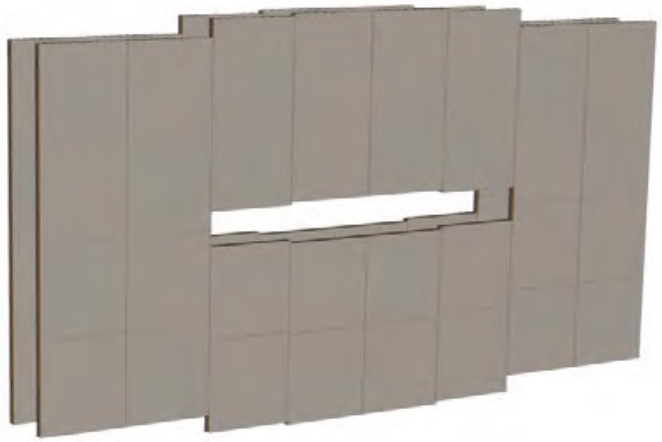
- A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 μm pitch and 20 ps time resolution.

FY22 Milestone #1

1. High-level strawman layout design and requirements for sub-systems using AC LGADs.







	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
E/FTTL	1.20/2.22	0.5*0.5	4.8/8.8M	25 ps	30um in x and y	0.08 X0
CTTL	10.9	0.5*10	2.4M	30 ps	30um in r*phi	0.01 X0
B0 tracker	0.07	0.5*0.5		30 ps	140um in x and y	0.01 X0
RP/OMD	0.14/0.08	0.5*0.5		30 ps	140um in x and y	no strict req.

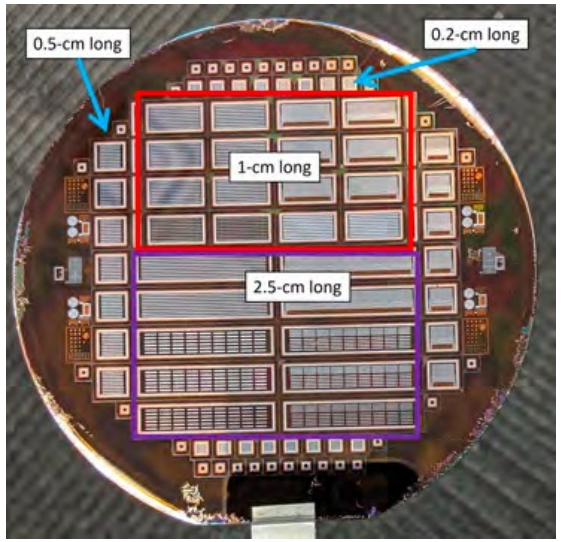
Requirements on the timing and spatial resolutions and material budget are still being evaluated and are subject to changes as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

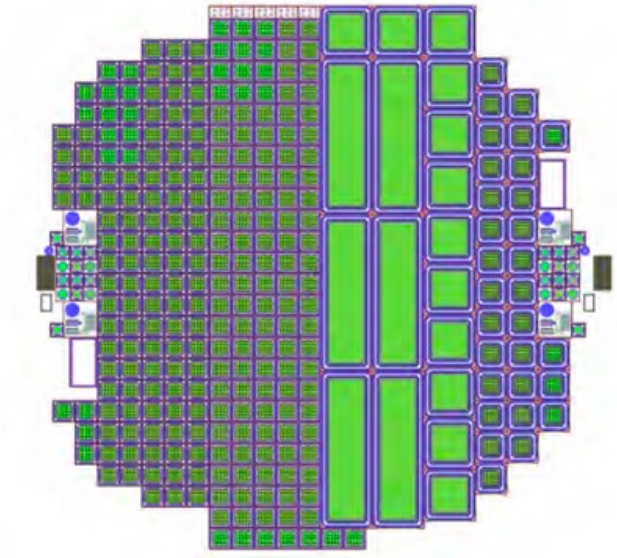
FY22 Milestone #2 and #3

2. Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes to optimize performance by BNL IO and HPK.

3. Start production of sensors of small thickness (20, and 30 microns) for ToF applications with time resolution 20 ps by BNL Instrumentation.

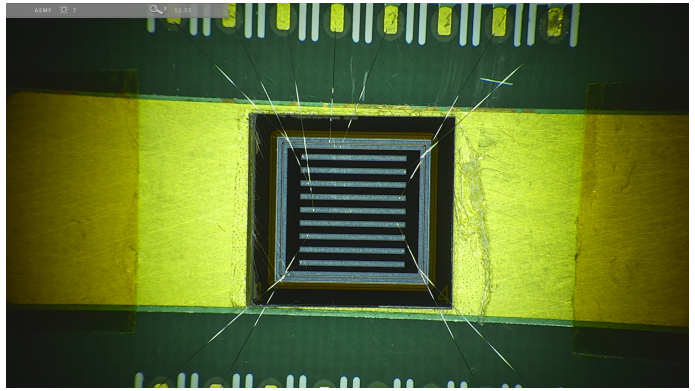
- 1st BNL IO (6-11/2021): 5-25mm strips with 500 um pitch, 100-300um electrode width, 50 um Si
- 2nd BNL IO (6-10/2022): strips with 500-700 um pitch, 50-100 um electrode width, 20-50 um Si
- 3rd BNL IO (8-12/2022): pixels with 500 um pitch, 20-50 um active Si
- Joint HPK production with US-Japan (6/2022-2/2023): strips and pixels with different pitch, electrode width, active Si thickness and n-layer doping



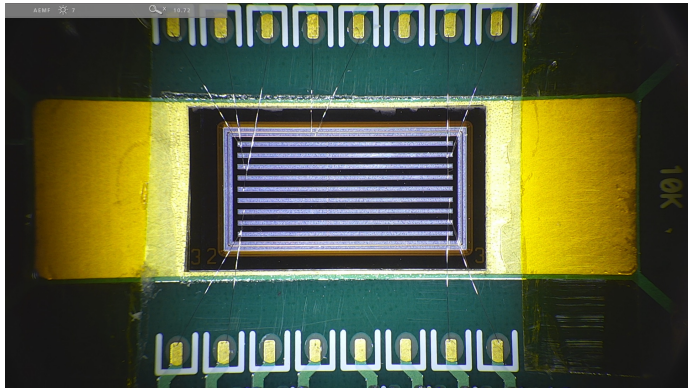


Placeholder for HPK

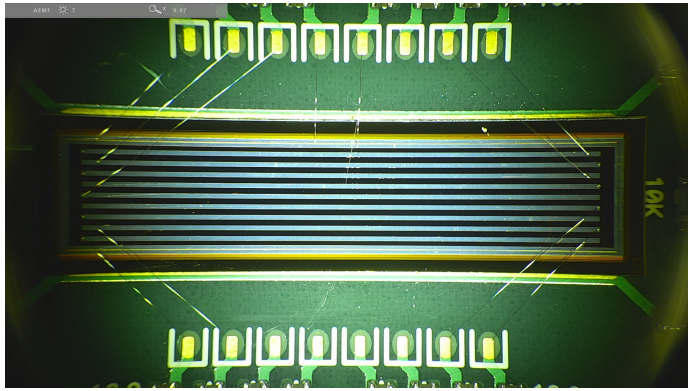
FY22 Milestone #2 and #3



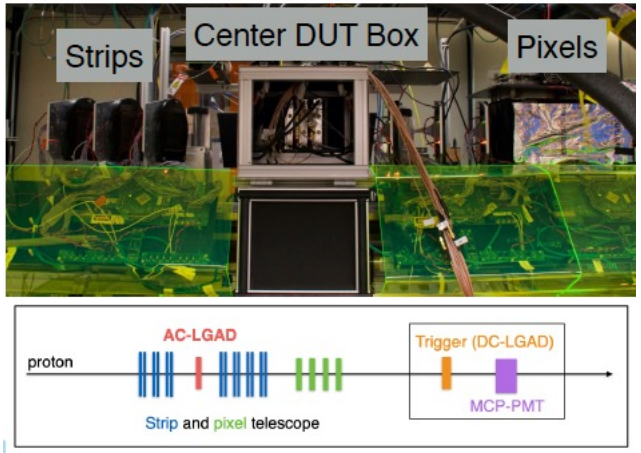
0.5*5 mm^2



0.5*10 mm^2



0.5*25 mm^2



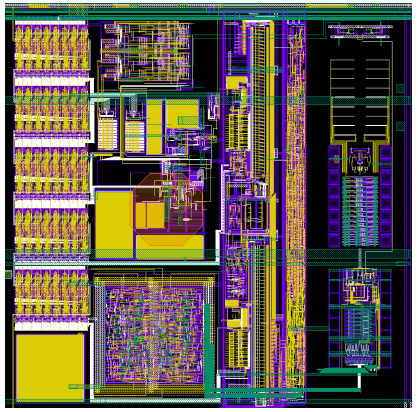
Preliminary Results	Time Resolution / hit	Position Resolution / hit
HPK-C2 Pixels 500 x 500 μm²	30 ± 1 ps	22 ± 1 μm
BNL Strips 500 μm x 5 mm	~ 30 ps (Hot spots)	< 15 μm
BNL Strips 500 μm x 10 mm	~ 32 ps (Hot spots)	< 20 μm
BNL Strips 500 μm x 25 mm	~ 53 ps (Hot spots)	< 40 μm

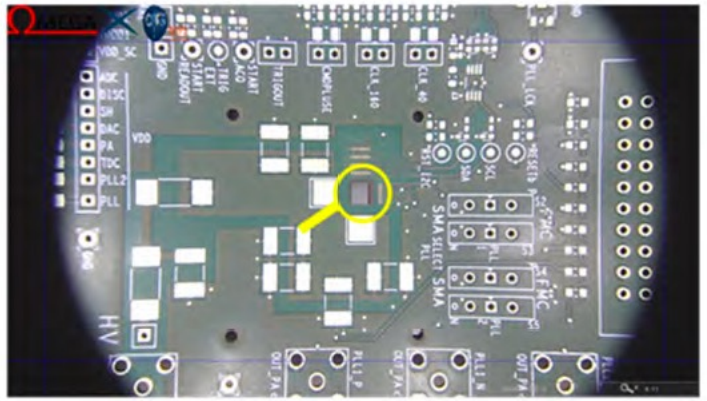
FY22 Milestone #4

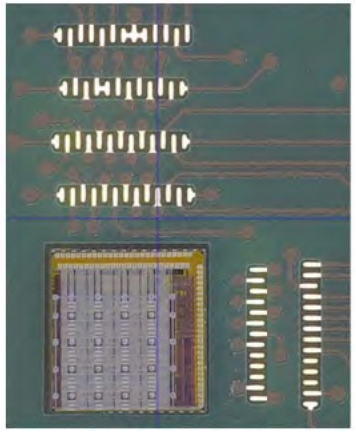
4. A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 µm pitch and 20 ps time resolution.

EICROC0 (submitted in 3/2022 and received in 7/2022) by IJCLab/OMEGA/CEA Irfu/AGH

- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)





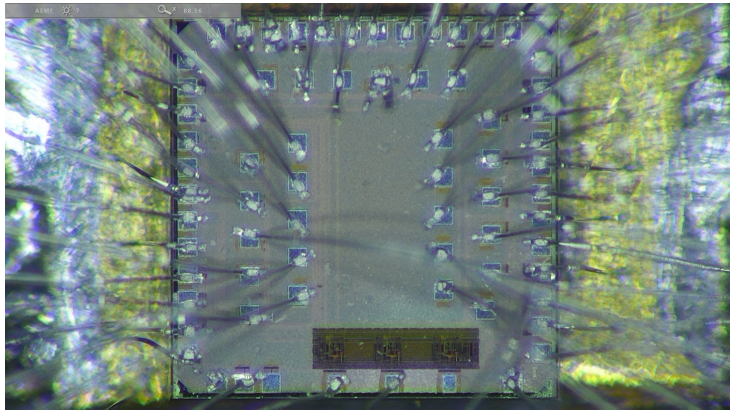


EICROC0

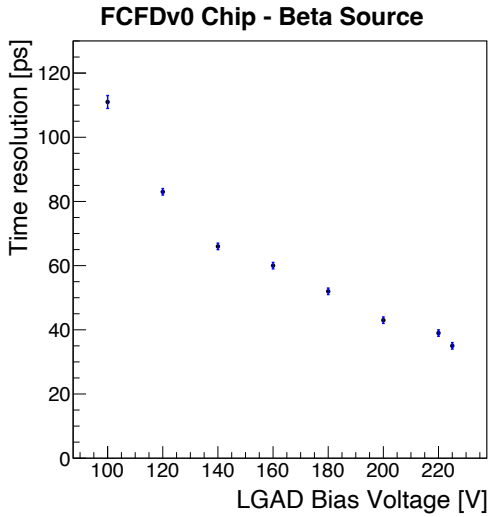
FY22 Milestone #4

FCFD0 (submitted in 2021) at Fermilab

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel when a CFD is paired with a TDC, one time measurement gives the final answer.
- Charge injection and beta source test consistent with expectation. Tests with beam are planned

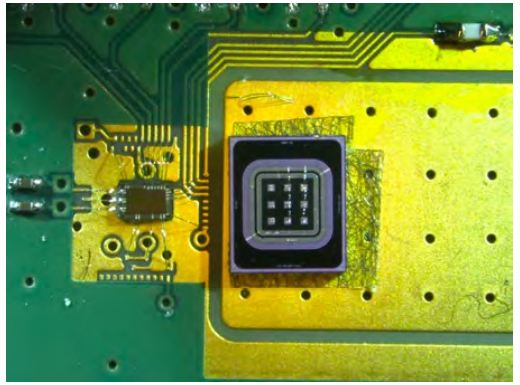


FCFD0

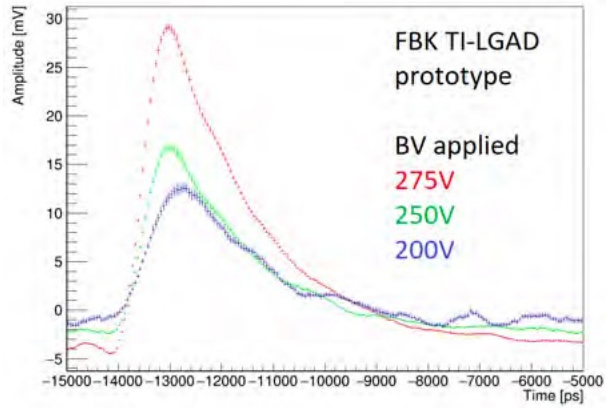


ASIC Efforts at UC Santa Cruz

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations, final Layout, Board design



HPSoC



FY23 Plan/Proposal

- Sensor R&D:
  - Productions by BNL IO and HPK/FBK
  - TCAD simulation, sensor characterization in the lab/beam, irradiation test
- Sensor/ASIC integration
  - Interposer to connect pixelated ASICs with strip sensors, or pixel sensors with various pitch
- Mechanical structure
  - Light-weight structure made from carbon-fiber composite materials and PEEK

- Frontend readout ASIC
  - EICROC0 test in the lab/beam, EICROC1 submission
  - FCFD0 beam test, FCFD1 submission
  - Characterization of ASICs from 3rd party institutions
- Frontend electronics
  - Timing chip, streaming readout, low-density flexible PCB, service hybrids

FY23 Deliverables

- Sensor prototype with 30 ps time and space resolution match RPs and Tracker;
  Sensor prototype with 20 ps time resolution for ToF
- 1st sensor + ASIC demonstrator for EIC applications and testing with particle beam.
- 2nd ASIC prototype submissions with better performance and extended features.
- Irradiation campaign for sensor and ASIC prototypes.
- Design and prototype of light-weight structure with cooling
- Design of flexes, interconnects and off-detector electronics.

eRD112
- Sensor R&D (382k$)
  - BNL, HPK/FBK productions
  - Lab/beam test, irradiation test
- Sensor/ASIC integration (45k$)
  - Interposer
- Mechanical structure ($35k)
  - Light-weight structure with cooling

eRD109
- ASIC (148k$)
  - EICROC1, FCFD1, SCIPP
- Frontend electronics (119k$)
  - Timing chips and streaming readout
  - TOF flex/service hybrids

EPIC Simulation
- Geometry model, digitization and reconstruction
- Requirements on spatial and timing resolutions, and material budget.

FY23 Resource Requests by eRD112

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Sensor Production				**175**
BNL IO	Sensor fabrication (incl. labor)	50 (10 wafers)	1.5	75
HPK/FBK	Sensor fabrication	75+3-5/wafer	1	100
Sensor Characterization				**13.7**
UIC	M&S for test beam setup	-	-	5
LANL	M&S for irradiation test	-	-	5
SCIPP	Fermilab 16-channel boards	-	-	3.7
Sensor/ASIC Integration				**30**
UIC	Interposer fabrication and bump-bonding	30	1	30
Mechanical Structure				**15**
NCKU	Material for light-weight support structure	-	-	10
Purdue	Material for light-weight support structure	-	-	5
Travel				**21**
BNL	Trips to Fermilab testbeam	2	2	4
UIC	Trips to Fermilab testbeam	1	5	5
ORNL	Trips to Fermilab testbeam	3	2	6
Rice	Trips to Fermilab testbeam	3	2	6
TOT.				**254.7**

Table 8: eRD112 resource request for M&S costs in FY23, excluding frontend ASIC and electronics.

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Sensor R&D				**172.3**
BNL	Sensor+ASIC and test board assembly	El. Tech.	10	20
UIC	Sensor+ASIC and test board assembly	El. Tech.	10	15
	lab/beam test for sensors and ASICs	Research Sp.	50	45
LANL	Sensor irradiation test	Scientist	2.5	10
	Sensor irradiation test	Student	5	5
Rice	pixel sensor test	Postdoc	40	40
SCIPP	Oversight and coordination	Project Scientist	5	9
	TCAD sim. and sensor design	El. Design Specialist	10	16.5
	Prototype Assembly	EM Engineer	5	11.8
Sensor/ASIC Integration				**15**
UIC	interposer design and testing	El. Engineer	10	15
Mechanical Structure				**20**
NCKU	light-weight support structure R&D	Mech. Engineer	10	5
Purdue	light-weight support structure R&D	Mech. Engineer	10	15
TOT.				**207.3**

Table 9: eRD112 budget request for labor costs in FY23, excluding frontend ASIC and electronics.

FY23 Resource Requests by eRD112

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Frontend ASIC				**118.3**
IJCLAB	EICROC1 submission	65	1	65
	EICROC test boards	-	-	10
FNAL	FCFDv1 submission	25	1	25
	FCFD test boards	-	-	15
SCIPP	ASIC service boards	-	-	3.3
Frontend Readout Electronics				**31**
BNL	Xilinx Dev Kit	4	1	4
	Timing cihps and boards	15	-	15
ORNL	Xilinx Dev Kit	4	1	4
	M&S	8	-	8
TOT.	-	-	-	**149.3**

Table 10: eRD109 budget request for M&S costs in FY23 on frontend ASIC and electronics.

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Frontend ASIC				**29.7**
SCIPP	Service board design layout	Electronic Design Specialist	7.5	12.4
	Board Assembly	Electro-Mechanical Engineer	5	11.8
	Board loading and lab msmt	Assistant specialist	5	5.5
Frontend Readout Electronics				**88**
BNL	Readout and Timing Distribution	Research Associate	20	38
ORNL	Barrel TOF Low-Mass Service Hybrid	Electric Engineer	10	32
Rice	Endcap TOF Service Hybrid	Electric Engineer	15	18
TOT.	-	-	-	**117.7**

Table 11: eRD109 budget request for labor costs in FY23 on frontend ASIC and electronics.