

Status and Schedule



RBRC

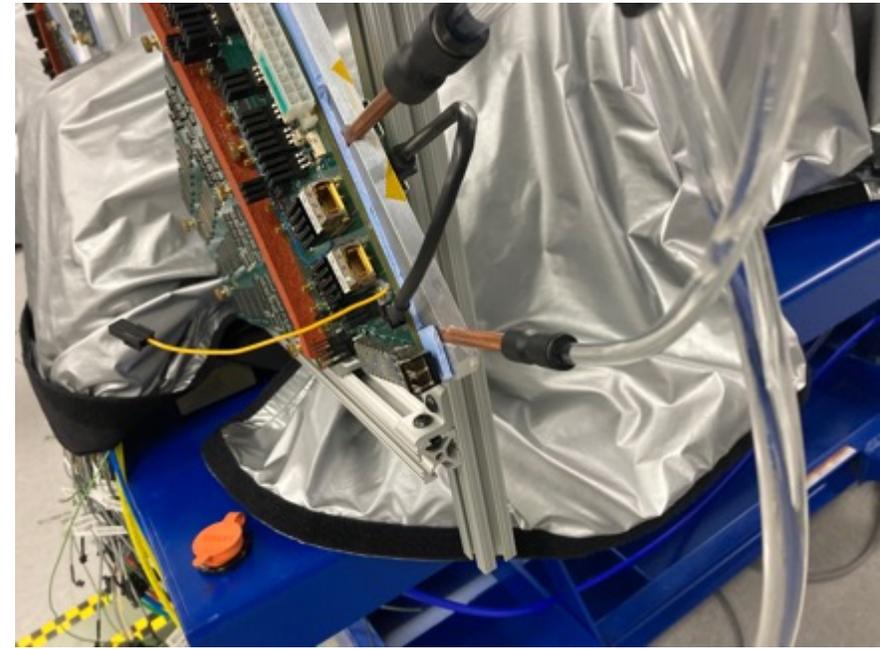
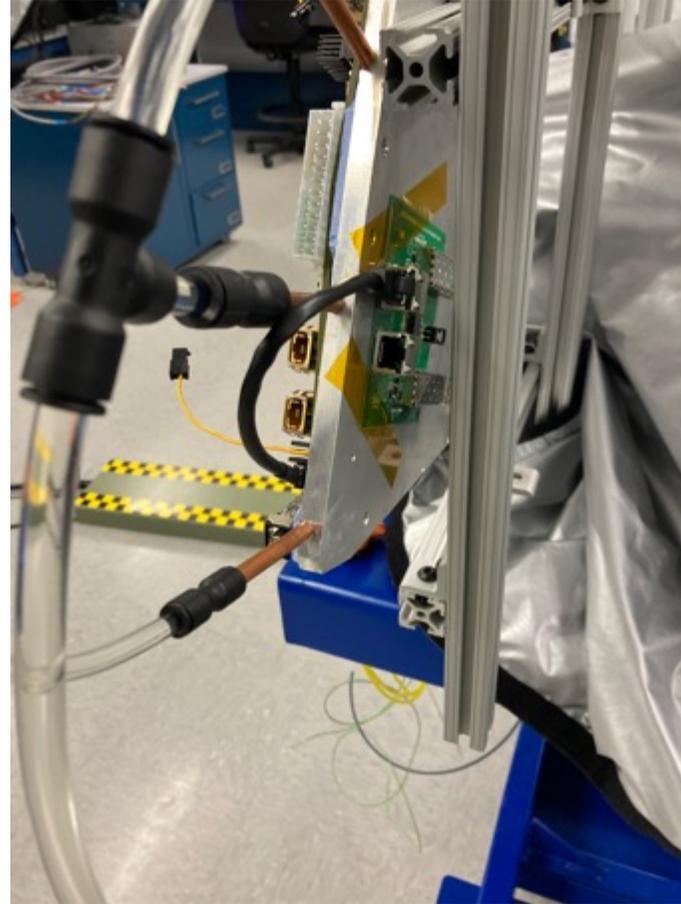
Itaru Nakagawa

Production Conversion Cables



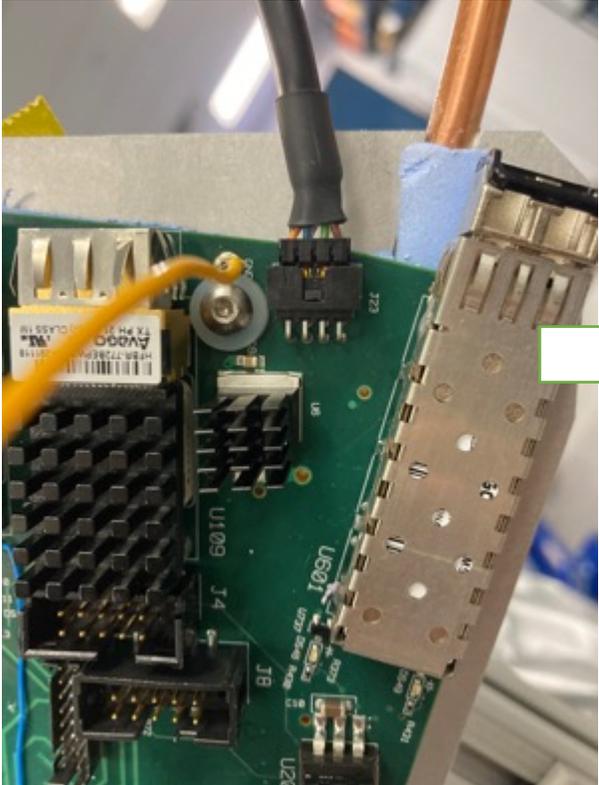
- Final checkout of assembled cables in Hayashi-REPIC and they are to be delivered to RIKEN next week on schedule.
- Itaru started exporting paper works so that cables are forwarded to BNL.

Beam Clock Cables

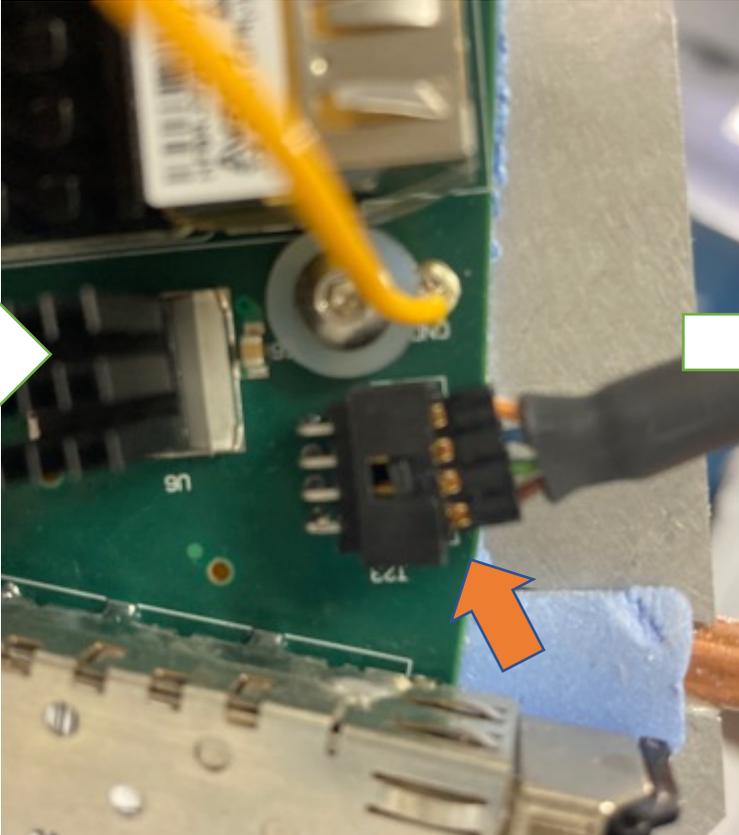


Installation test pursued with Dan Cacace. The cable length is confirmed to be OK. Stress is reasonably minor.

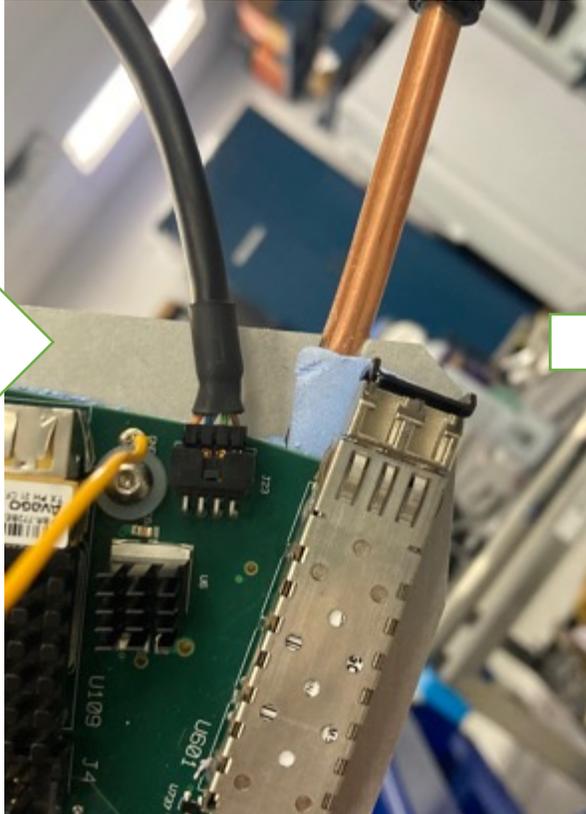
Beam Clock Cable Stress Test



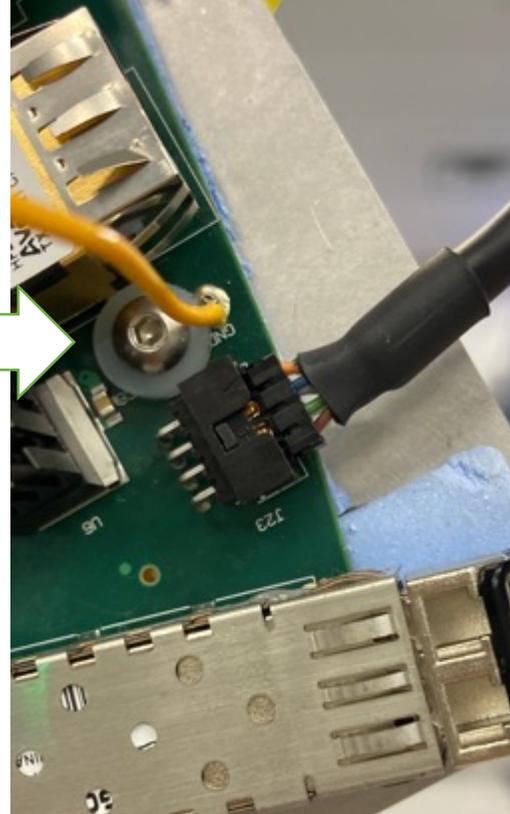
Day-0



Day-1 (22hours later) became loose. Pushed the connector all the way in.



Day-5



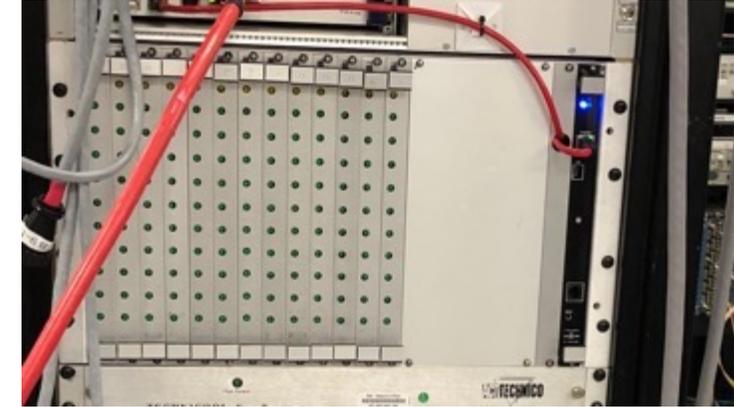
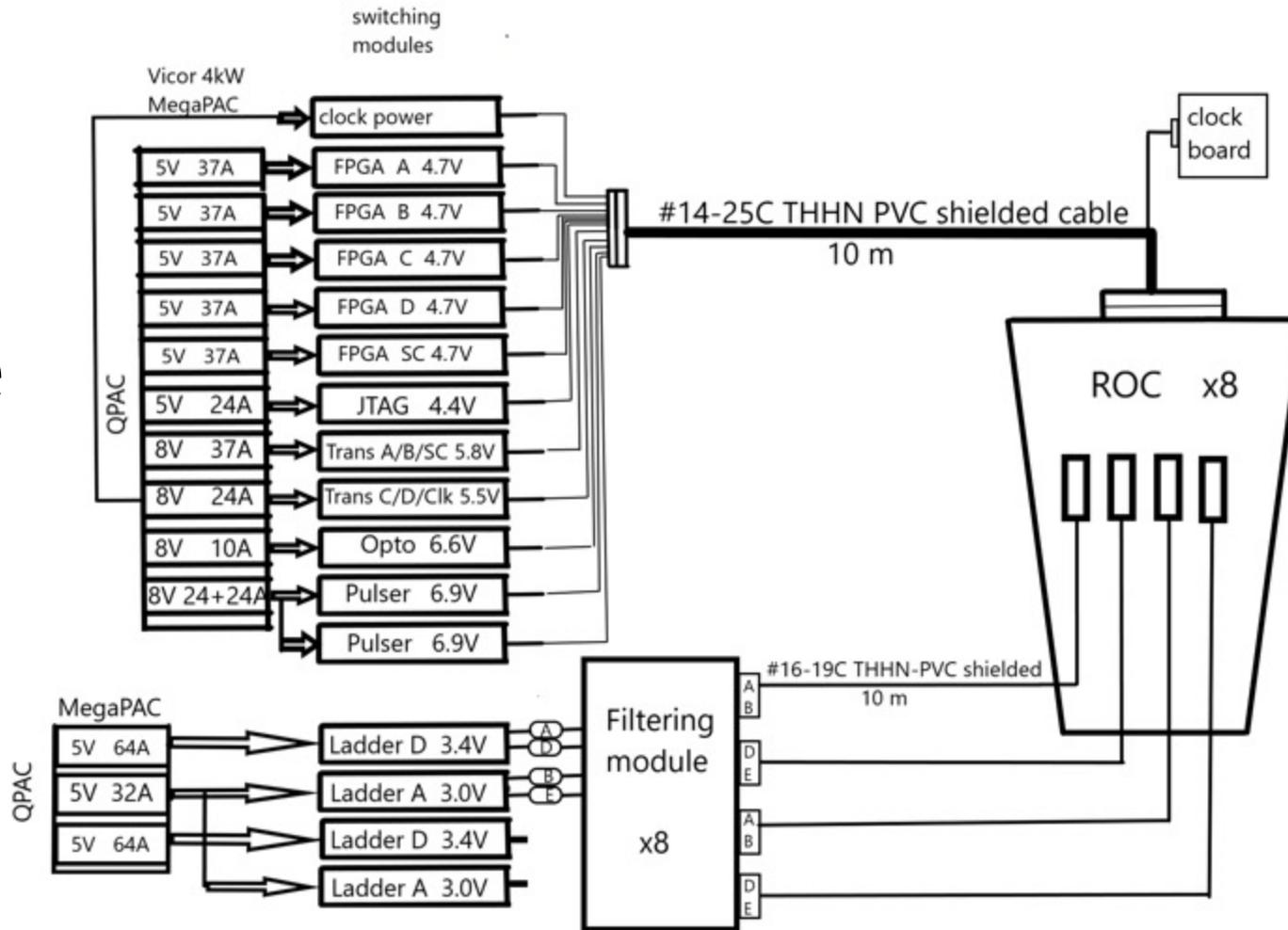
Day-6

The connector became loose on the next day though, the stress seems to be relaxed as the time goes by. Dan may consider encapsule the connector area with a kind of glue.

LV System Development

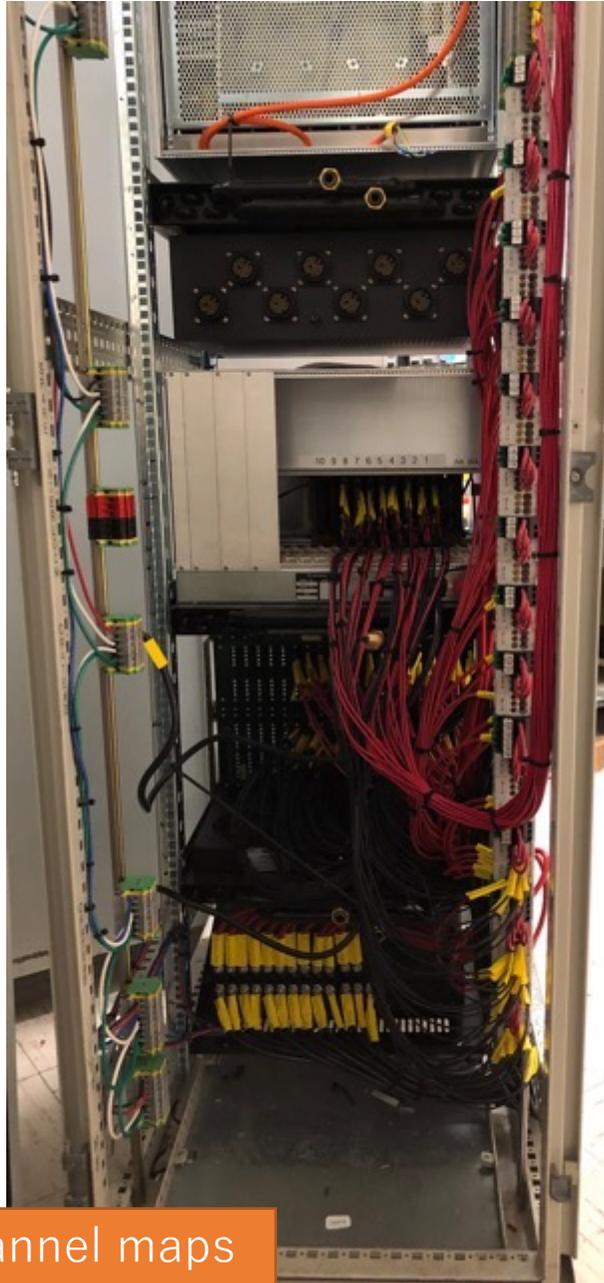
Need to turn on 11 channels/ROC&BCB

ROC power scheme



Switching Module

INTT racks, rack #1 front and back and rack #2 front and back (left to right)



Bias crate

Bias Filter
box is in →
construction

LV filter
crate

Switching
crate

Vicor
MegaPACs



Need to develop channel maps

New DAC Setting

Optimized DAC Setting for INTT Calibration

DAC	Default	New
0	20	15
1	25	19
2	30	23
3	35	27
4	40	31
5	45	35
6	50	39
7	55	43

74 FPHX TestStand DAQ

File

All / D3 | Mod A0 | Mod B0 | Mod C0 | Mod D0 | Mod A1 | Mod B1 | Mod C1 | Mod D1 | Mod A2 | Mod B2 | Mod C2 | Mod D2 | Mod A3 | Mod B3 | Mod C3

Reg	Desc	To Chip	From Chip	Chip Command				
*	Wild	0		Read	Write	Set255	Reset	Default
1	Mask	0		Read	Write	Set255	Reset	Default
2	Dig Ctrl	5		Read	Write	Set255	Reset	Default
3	Vref	1		Read	Write	Set255	Reset	Default
4	DAC0	20		Read	Write	Set255	Reset	Default
5	DAC1	25		Read	Write	Set255	Reset	Default
6	DAC2	30		Read	Write	Set255	Reset	Default
7	DAC3	35		Read	Write	Set255	Reset	Default
8	DAC4	40		Read	Write	Set255	Reset	Default
9	DAC5	45		Read	Write	Set255	Reset	Default
10	DAC6	50		Read	Write	Set255	Reset	Default
11	DAC7	55		Read	Write	Set255	Reset	Default
12	NTSel <3:0>	6		Read	Write	Set255	Reset	Default
	N2Sel <7:4>	4						
13	FB1Sel <3:0>	4		Read	Write	Set255	Reset	Default
	LeakSel <7:4>	0						
14	P3Sel <1:0>	0		Read	Write	Set255	Reset	Default
	P2Sel <7:4>	4						
15	GSel <2:0>	2		Read	Write	Set255	Reset	Default
	BWSel <7:3>	8						
16	P1Sel <2:0>	5		Read	Write	Set255	Reset	Default
	InjSel <5:3>	0						
17	LVDS Current	3		Read	Write	Set255	Reset	Default
18	Resets	n/a		Read	Write	Set255	Reset	Default

Chip Control
Display/Modify Configuration for Chip ID Side

Channel Mask
[Red = Off, Green = On]

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127

Mask All Unmask All Toggle All Send

Beam mask

Chip Side Enable

0	15	0	1	8	15	0	1	16	15	0	1	24	15	0	1
1	15	0	1	9	15	0	1	17	15	0	1	25	15	0	1
2	15	0	1	10	15	0	1	18	15	0	1	26	15	0	1
3	15	0	1	11	15	0	1	19	15	0	1	27	15	0	1
4	15	0	1	12	15	0	1	20	15	0	1	28	15	0	1
5	15	0	1	13	15	0	1	21	15	0	1	29	15	0	1
6	15	0	1	14	15	0	1	22	15	0	1	30	15	0	1
7	15	0	1	15	15	0	1	23	15	0	1	31	15	0	1

TestStand

Spartan3 ROC ROC+FEM FEM Addr 15 DB Access On Off

Global Chip/DAQ Operations

FFR	Enable RO	Latch FPGA	Core Reset	Start DAQ	Check GLINK	test
Init	Disable RO	Calib	JTAG Sync	Stop DAQ	Check FEM	Mask
FO Sync	Set L1	Delay 5	BCO Start	Global Start	Self Trig	DAC
FPGA RST	Er. EEPROM	Write Page	Read Page	Write All	Cosmic Start	Loop

DAQ Configuration

DAQ Program C:/Users/RIKEN_INTT/D Browse

NI DAQ Sample Rate (MHz) 5

Num of events (0==inf) 0

Duration HH:MM:SS (0:00:00==inf) HH:MM:SS

Print Output Print Off

FPHX version (for Print) 2

Run Number

Filename

Beam Species None

Beam Energy 0

Pulsar Configuration

Pulse amplitude (10 bits max) 255 Config Amp Pulse

Num of Pulses 1 Pulse Train

BCOs between pulses 1023 Wedge 0 Module 0 Set Module

Module Enable

Module 15 On Off Both Side 0 Side 1 Module 7 On Off Both Side 0 Side 1

Module 0 On Off Both Side 0 Side 1 Module 8 On Off Both Side 0 Side 1

Module 1 On Off Both Side 0 Side 1 Module 9 On Off Both Side 0 Side 1

Module 2 On Off Both Side 0 Side 1 Module 10 On Off Both Side 0 Side 1

Module 3 On Off Both Side 0 Side 1 Module 11 On Off Both Side 0 Side 1

Module 4 On Off Both Side 0 Side 1 Module 12 On Off Both Side 0 Side 1

Module 5 On Off Both Side 0 Side 1 Module 13 On Off Both Side 0 Side 1

Module 6 On Off Both Side 0 Side 1 Module 14 On Off Both Side 0 Side 1

Manual Packet Send

Packet file to send Browse Send Read

Communications

USB None Ethernet IP Addr 192.168.60.2 Port 9900

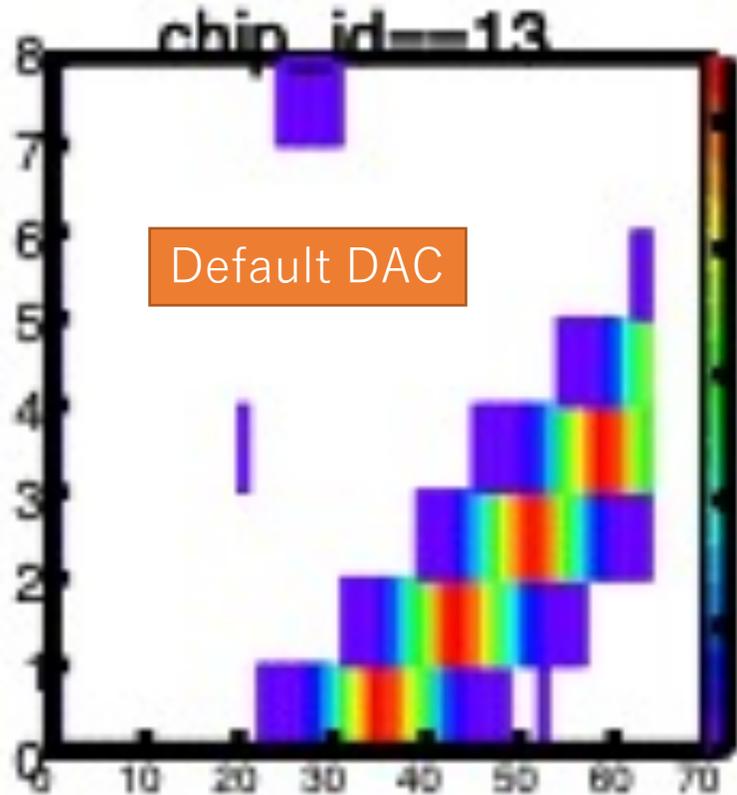
Baud Rate 115200

ver7

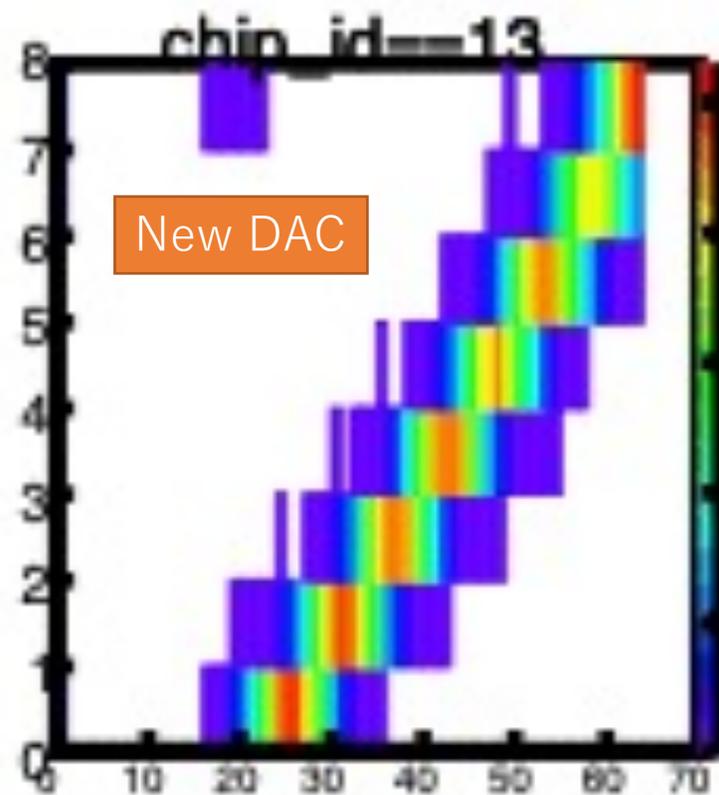
ROOT Module ID 6 Calib External camac ROOT_imp

New DAC Setting Result

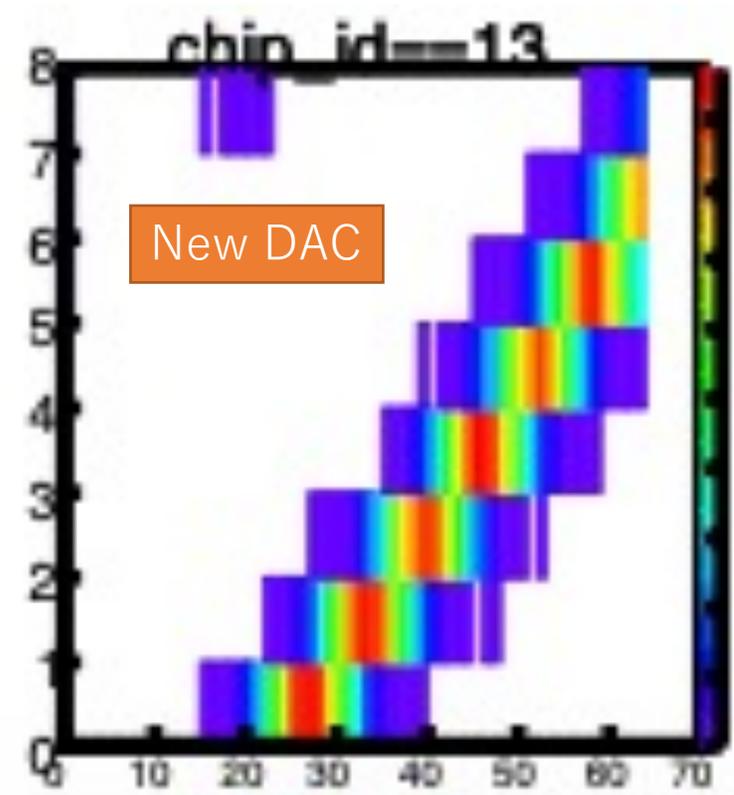
INTT+BEX+ μ -Coax



INTT+ μ -Coax

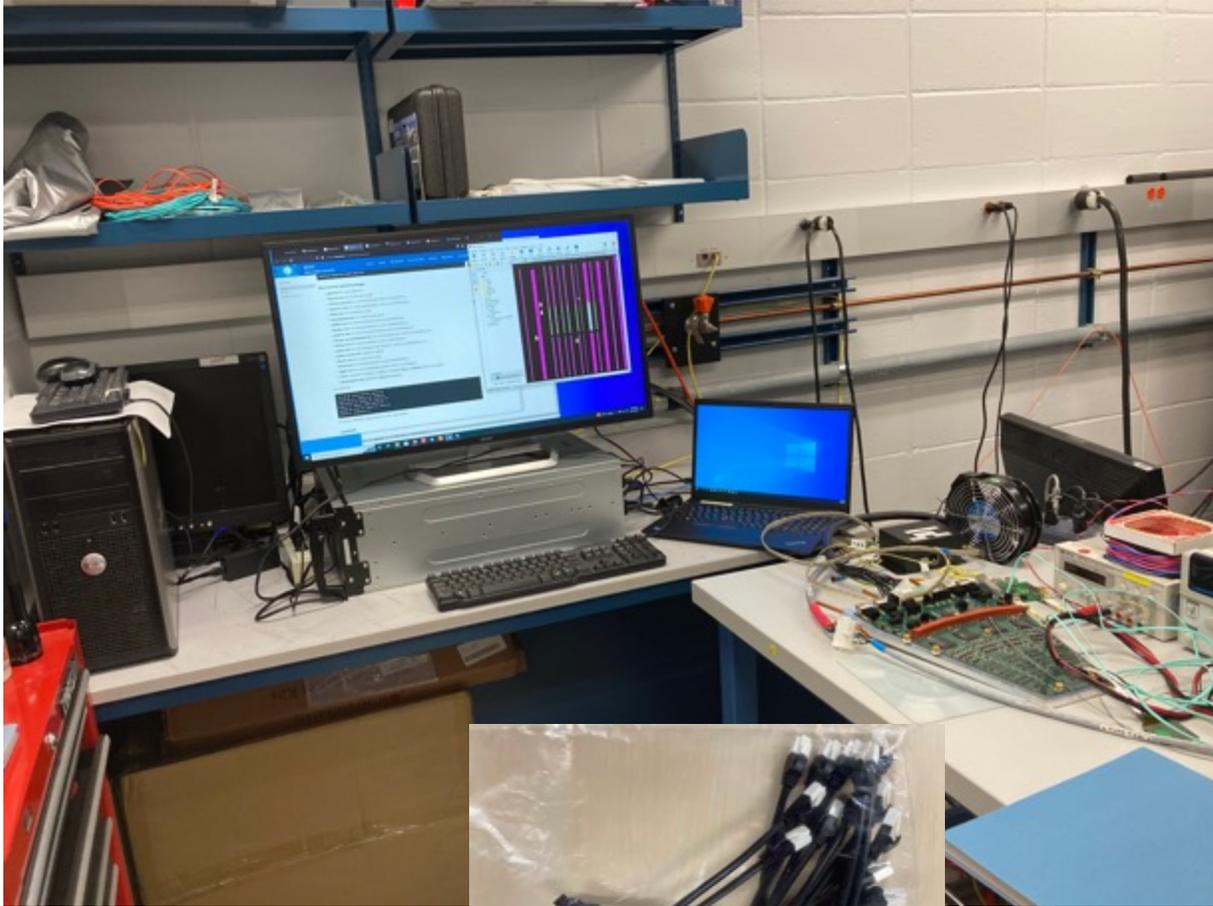


INTT+BEX+ μ -Coax



Measurements by Rikkyo Undergraduates

2nd Felix Test Bench Preparation



- Decoupled from Raul's development and now allocated dedicated machine for users to test as originally aimed.
- Loaded FPGA code with the latest stable version.
- Waiting for Raul to setup a spare fiber and cassette.
- Other components are ready.
- To be started data taking from next week.
 - **New DAC setting** for the calibration
 - 24 production beam clock cable test
 - Analysis on the felix server
 - Slow control command tests
 - Calibration database development
 - Readback test (once SC-FPGA @ ROC is ready)
 - Preparation for cosmic ray data taking (requires firmware upgrade by Raul).

sPHENIX End Game Review

Oct 13, 2022, 10:00 AM → Oct 14, 2022, 5:00 PM US/Eastern

Description <https://bnl.zoomgov.com/j/1605049719?pwd=cTQxNkR0TGhaSHB3TGJybWNgc1VGUT09>
Join ZoomGov Meeting

Meeting ID: 1605049719
Passcode: 076821

📎 Agenda_Installatio... Charge sPHENIX IF... **Critical path schedules** ▾ **Detailed Schedules** ▾
Monthly Status Reports ▾ **MoU/MoAs** ▾ **Project Management Plan** **Review Committee**
sPHENIX KPPs and Deliverables **sPHENIX TDR** **Summary Schedules**

<https://indico.bnl.gov/event/17429/>

THURSDAY, OCTOBER 13

- 10:00 AM** → 10:25 AM **sPHENIX Status (20+5)** ⌚ 25m
Speaker: Edward O'Brien (BNL)
 sPHENIX_ReviewE...
- 10:25 AM** → 10:45 AM **sPHENIX Organization and Resources (15+5)** ⌚ 20m
Speaker: Glenn Young (BNL)
 Resource Requirem... Young_Project_Org...
- 10:45 AM** → 11:05 AM **Experiment Expectations in 2023 (15+5)** ⌚ 20m
Speaker: Gunther Roland (MIT)
 EndGameReview_R...
- 11:05 AM** → 11:50 AM **Installation and Schedule (30+15)** ⌚ 45m
Speaker: Russell Feder (sPHENIX)
 2022OCT11_SCHE... 2022OCT13_sPHE...
- 11:50 AM** → 12:05 PM **Break** ⌚ 15m

Current Installation Schedule (not P6)

Tasks	Nov 22	Dec 22	Jan 23	Feb 23	Mar 23	Apr 23
Magnet Mapping	3 wks					
Finish Install EMCal/Cable IHCal		2 wks				
Install/Cable TPOT		6 wks				
Cable EMCal		6 wks				
Install/Cable TPC			6 wks			
Install/Bakeout Beampipe				3 wks		
Install/Cable INTT					3 wks	
Install/Cable MVTX						3 wks
Install MBD						2 wks
Ready for commissioning with beam						

sPHENIX construction schedule after magnet mapping



Sequential Build Steps	Start	End	N-22	D-22	J-23	F-23	M-23	A-23
Magnet Mapping		11/24/22	█					
Complete EMCAL sector installation	11/25/22	12/5/22		█				
iHCAL cabling, oHCAL cabling completion	11/25/22	12/5/22		█	█	█		
TPOT, EMCAL-face support frames, TPOT services N&S	12/6/22	1/23/23		█	█	█		
EMCAL services north and south	12/10/22	1/23/23		█	█	█		
TPC installation, TPC services north and south	1/8/23	2/19/23			█	█		
INTT support structure, <i>beam pipe, beam pipe bake</i>	2/20/23	3/10/23				█		
INTT installation, INTT services north and south	3/17/23	4/5/23					█	█
MVTX installation, MVTX services south	3/29/23	4/10/23						█
MBD, MBD services north and south	4/6/23	4/17/23/23						█
sEPD, sEPD services north and south, VESDA tubing	4/12/23	4/24/23						█
Racks and On-carriage AC power	Current	1/20/23	█	█	█			
Water infrastructure: ECW and chilled water systems	Current	2/17/23	█	█	█			
Gas systems	Current	3/17/23	█	█	█	█		
E-stops, VESDA system, safety systems	Current	4/24/23	█	█	█	█	█	
								14

Continue oHCAL, iHCAL, EMCAL, TPOT, TPC servicing and testing on alternate shifts and overtime

Infrastructure work on primary shifts and overtime

Winter holidays

- **Post Integration test in the Lab (Phy-lab 2-82): October 24, 2022**
 - After Integration of the two INTT halves in the lab, the INTT will be moved to the Si-Lab to be fully tested with:
 - Conversion cables (cable detector to ROC: 15 cm),
 - Simultaneous test of two ROCs with Felix readout,
 - Final survey of the two INTT halves.
 - Cosmic-Data and offline Analysis
- **Pre-installation@IR: February 2023**
 - Full INTT test at the sPHENIX-IR assembly hall using INTT bench test: LV/HV/DAQ rack
- **Installation@IR: March 17, 2023**
- **Post-installation@IR:**
INTT integration in the IR: using sPHENIX infrastructure @IR
 - Installation ROCs, optical cables ROCs-IR rack
 - Cooling powered
 - LV/HV racks powered
 - Electrical test of barrels North and South (pulse test calibration)

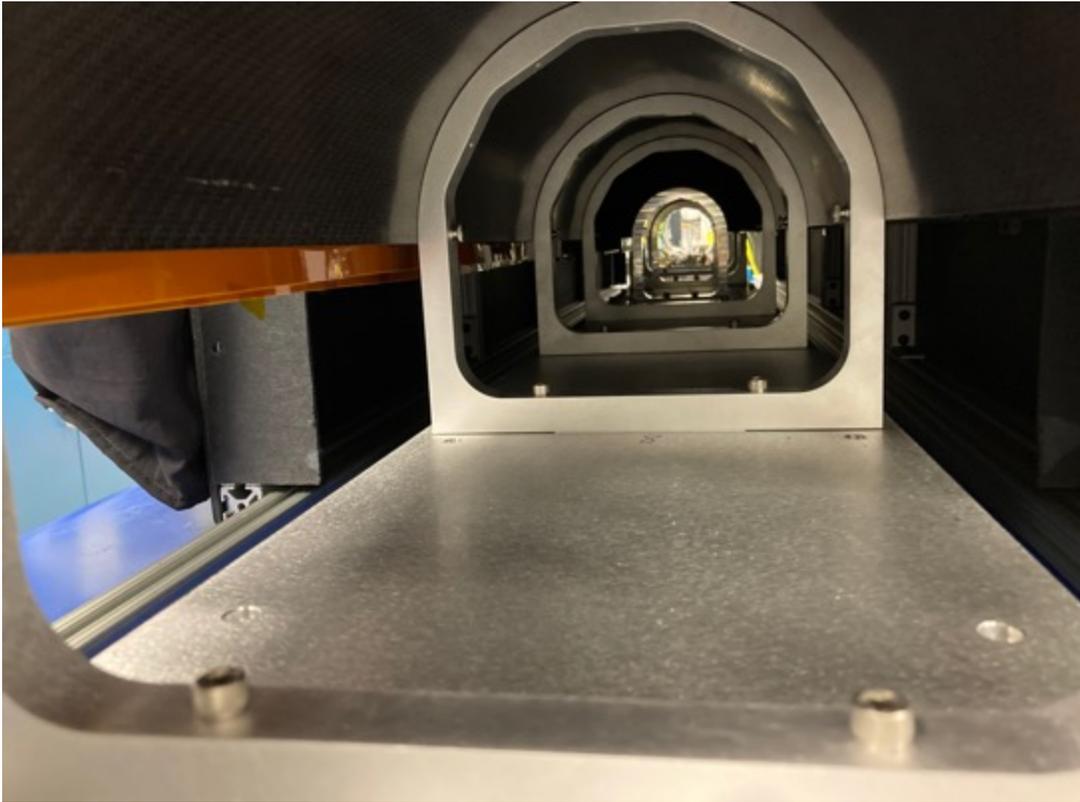
October	November	December	January, 2023	February, 2023	March, 2023
<ul style="list-style-type: none"> • INTT Integration test in the lab. • Felix Readout development 	<ul style="list-style-type: none"> • INTT full test with conversion cables and Felix readout with two ROC (14 half ladders) • LV/HV Gui development 	<p style="text-align: center;">Ready for installation</p> <ul style="list-style-type: none"> • Cosmic Data and offline analysis in the Si-Lab • LV/HV Gui development 	<ul style="list-style-type: none"> • Cosmic Data and offline analysis in the Si-Lab 	<ul style="list-style-type: none"> • INTT move to sPHENIX-IR assembly hall • Full test using INTT test-bench • Installation LV/HV cables to the racks • Installation of optical fibers from IR-racks to DAQ at electronic room 	<ul style="list-style-type: none"> • INTT insertion: 03/17/23 • Complete IR installation 04/05/23 • Commissioning INTT with full readout chain

Cosmic Ray Data Taking with the Barrel



To be implemented trigger scintillator paddle on top of the barrel.

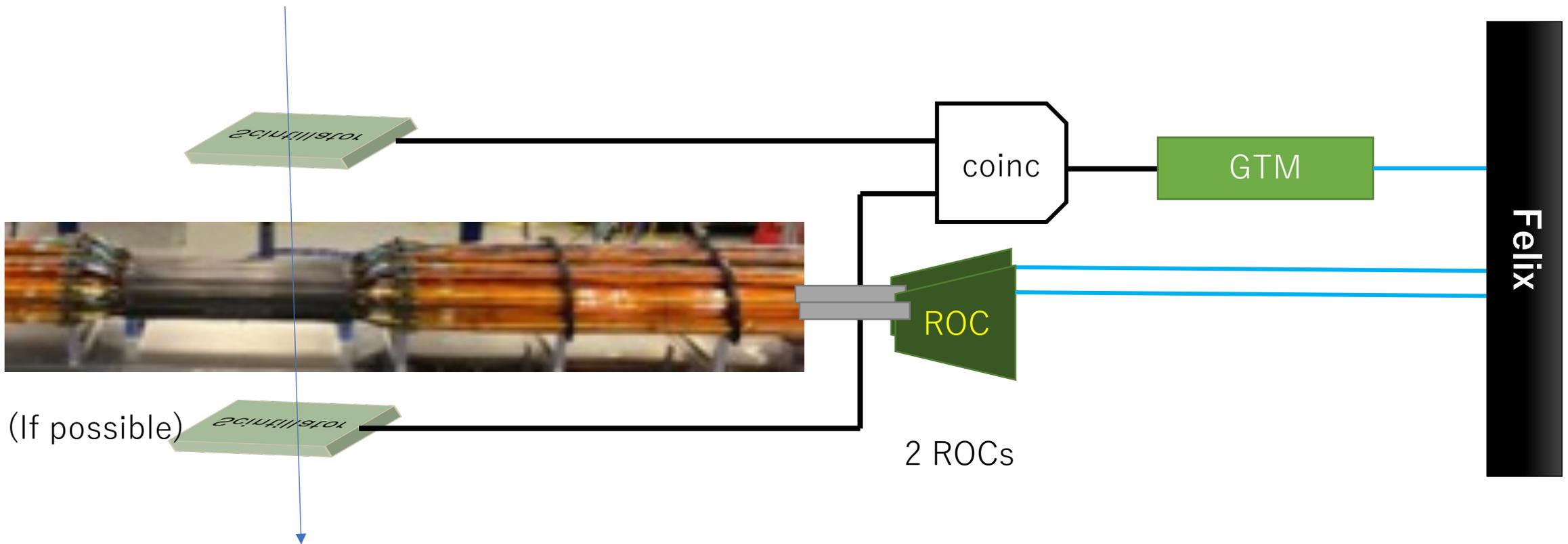
Sandwich Trigger?



Not easy. Need exact size scintillator to fit in between support structure.

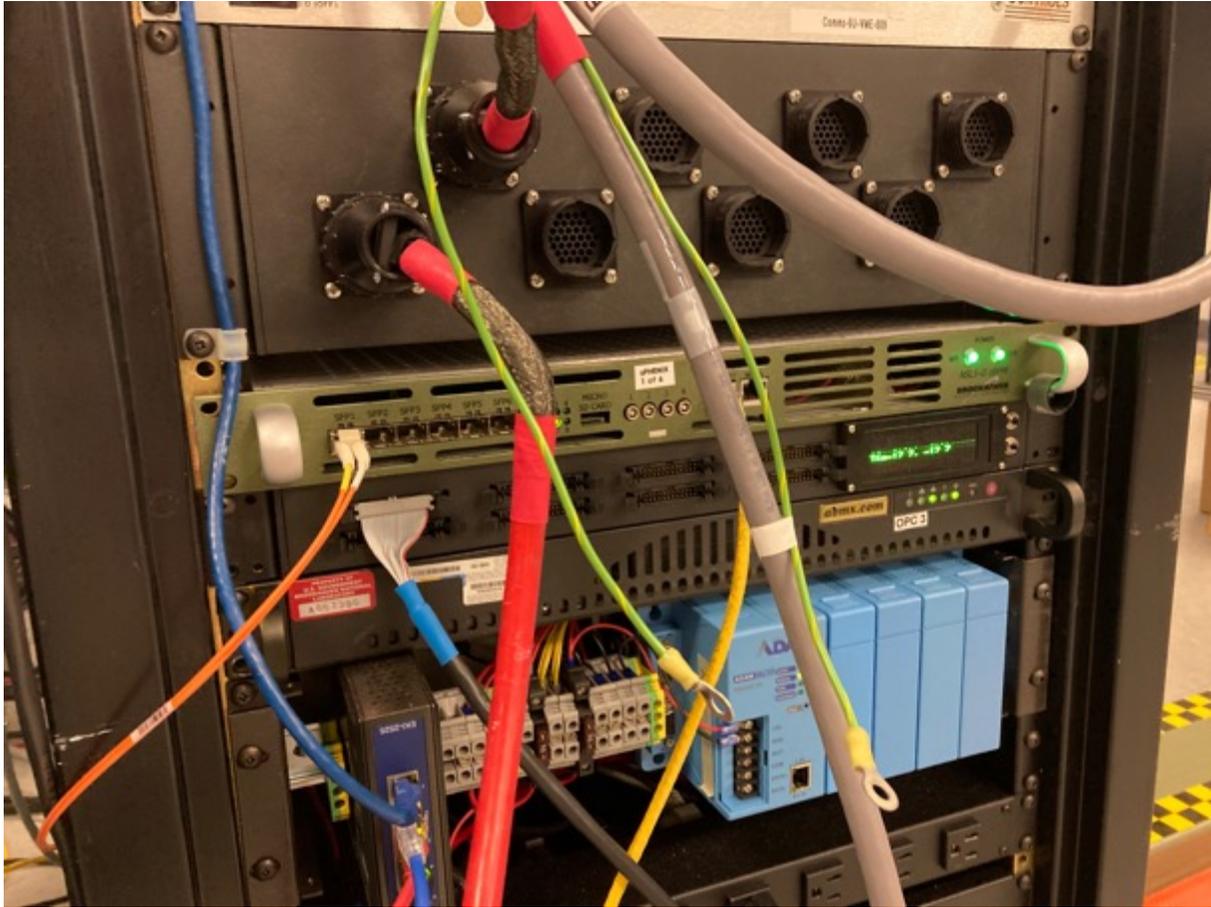
Cosmic Ray Data Taking with the Barrel

- Scintillator paddle(s) matching with a half of the half-barrel acceptance.
- External Trigger using GTM
- Number of ladder operation may be constrained by the power supply.



Cosmic Ray Data Taking with the Barrel

GTM prototype @ Silicon Lab.

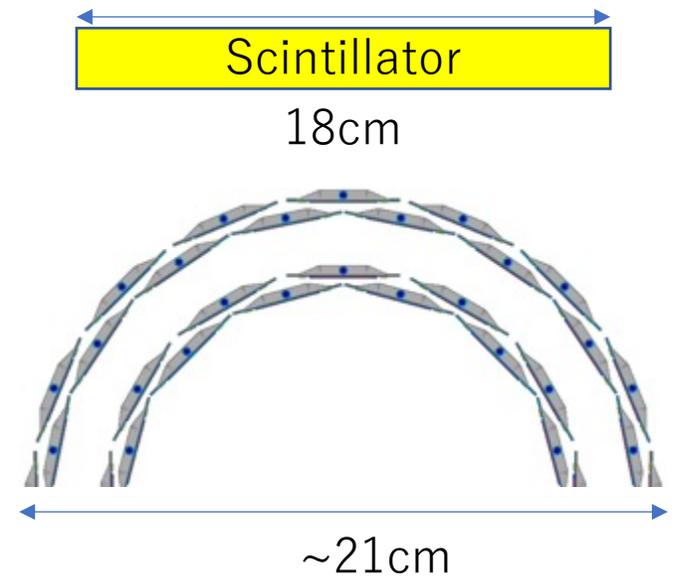


Although the GTM module in the Silicon Lab is a prototype, the firm ware is up-to-date to accept the TTL external trigger input (confirmed with Martin).

Trigger Scintillator



- Phobos Scintillator
81cm x 18cm x 5cm
- Heavy and better not to be mounted on top of the barrel dark box. Need to build a support structure.



Cosmic Ray Data Taking with the Barrel

- First silicon signal observation for the most of production ladders
- Simultaneous operation of multi-ladders (different test from multi-ladder calibration)
- Correlated hits between different layers. Can operate upto 14 half ladders
- Pilot experience of the time-in process prior to the commissioning.
 - Unsuccessful in 2019 Beam test, Successful in 2021 Beam test, but with FEM/FEM-IB based readout system. No experience with Felix.
- Nice testing and fine-tuning ground of online/offline software
 - Online monitor
 - Stability monitor
 - Event display
 - Track Reconstruction Code

