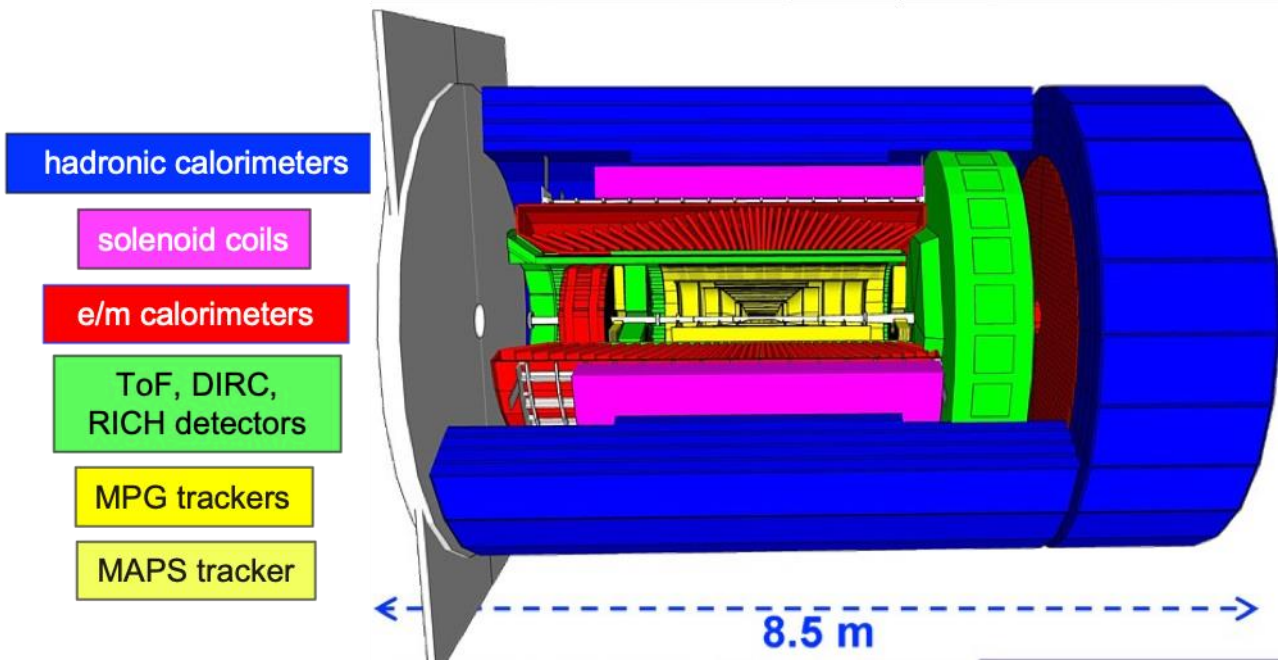
Special Streaming Workshop: ePIC DAQ and Electronics Protocols, Interface, Timing and Clock Distribution

Jeff Landgraf

This workshop tailored to the ePIC Detector's DAQ



- Electron / Ion collider
- Polarization by bunch
- 500kHz maximum event rate
- 100Mhz bunch frequency
- Streaming, triggerless DAQ
- Large number of channels
- Low occupancy
- Expected compressed collision/background ~< 100Gb/s

Detector Group	Channels				Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD				
Tracking	32B			100k	500	13	15	15
Calorimeters	50M		150k		2050	50	15	15
Far Forward	300M	2.3M	500		174	5	1	1
Far Backward		1.8M	700		113	4	100	2
PID		3M-50M	600k		638	40	3220	45
TOTAL	32B	7.1M-54M	750k	100k	3475	112	3350	78

Preliminary Information

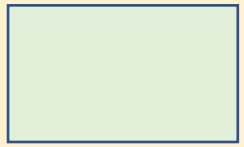
- Thank you to Jan Bernhauer and to the CFNS!
- How we fit into the major project schedule milestones

Milestone	Local Review	DOE Review	Approval
Change control	March 2023		
CD 3-A (60% design → costs)	Aug 2023 (pre-TDR)	Oct 2023	Jan 2024
CD 2 (90% design)	Aug 2024 (TDR)	Oct 2024	Jan 2025
CD 3 (construction)		(Jan 2025)*	April 2025

* = My guess, not scheduled scheduled

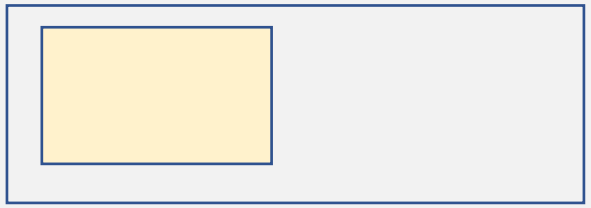
- RDO Status – Subgroup forming (Jo, Tonko, William, Pietro*, Marius), Hope to have update soon
- Hao Xu will have 1 FLX-182 board for testing likely available in March

EPIC Electronics / DAQ



Global Timing Unit (GTU)

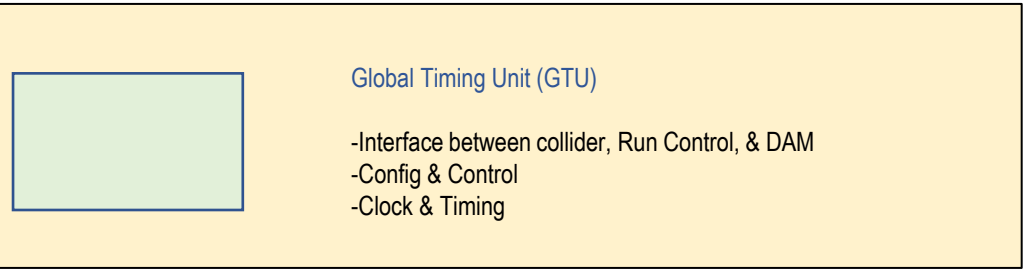
-Interface between collider, Run Control, & DAM
-Config & Control
-Clock & Timing



Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

This workshop is centered the RDO and its interfaces, including the GTU

- Crucial component
  - Single design to the extent practical, but variations are expected!
  - Constitutes the interface to the detectors
    - Common fiber protocols
    - Detector Specific electronic connections
  - The only component capable of sharing real-time information between detectors
  - The only information pathway to the front ends
    - Configuration
    - Firmware
    - Special ASIC/board support
    - Clock and Synchronization
    - Data transfer protocol
    - Special Data Handling (disable ML/AI, disable zero-suppression, select calibration modes, etc…)
    - Flow Control



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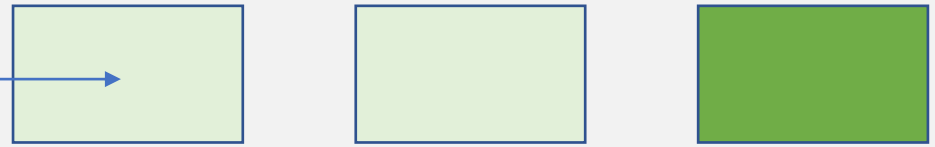

Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Few Variants	Common	Common
-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

Schedule

8:30am	Introduction
9:00am	FEB / ASICs (detector issues & interfaces)
11:45am	Functional Protocols (information flow)
2:30pm	Timing and Clocks (precision electronics)
5:00pm	Summary

Each session will have the same general format

1. Some short presentations describing the requirements, status, experience, and open questions in each area. The purpose of these presentations is to get the discussion going.
2. Open discussion

Because of the focus on the discussion the times here may be fluid.

Introductions…