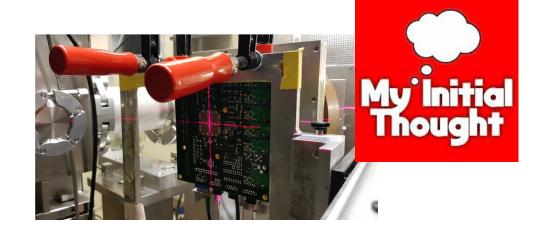
Radiation tolerance and electronics design choices for EPIC



"some initial thoughts"

- Generalities about SEL / SEU protection + some references
- assess some SEU rates at EIC (dRICH case)
- some food for discussion about next steps for our organization...

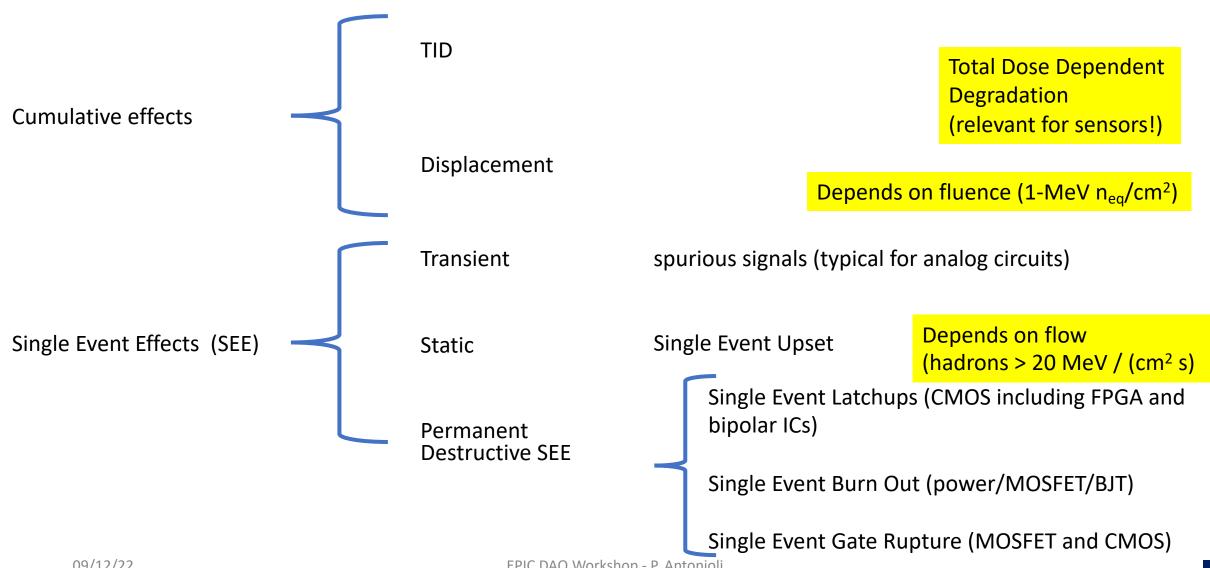




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Radiation effects in electronics: the usual picture





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LHC and space are useful reference....



- with LHC, space / military tests/procedures moved to HEP...
- rad-hard architecture in some cases are HEP-projects (ex: GBTx / lpGBTX)
- HEP world tries to be "rad-tolerant" (mitigation procedures) for SEU only in some cases rad-jard
- test against SEL plus SEL protection design of cards (usually with microcontroller space-grade acting as current watcher of sub-sections)
- commercially available technology rad-hard & space-grade especially for FPGA is usually too expensive for HEP/NP applications (ex. RT-Microsemi)
- key reference for methodology testing for SEU in HEP radiation environment remains M. Huhtinen and F. Faccio, <u>Nucl. Instrum. Methods Phys. Res., A 450 (2000) 155-72</u>
- various network resources available for component choice [<u>Xilinx XRTC Wiki</u>, Tullio Grassi's <u>preferred list</u> at CERN (CMS), accelerator community (ex: <u>Hydra</u>, <u>Distributed IO Tier</u>,)]
- Good general review on mitigation techniques: F. Siegle et al., "Mitigation of Radiation Effects in SRAM-based FPGAs for Space Applications", ACM Computing Surveys 47 (2015) 1 https://doi.org/10.1145/2671181

Some initial back of the envelope estimates



known (... to me) references on radiation levels for EIC environment (before listening Jin's talk at this workshop)

- a YR estimates from A. Kiselev
- https://indico.cern.ch/event/749003/contributions/3330764/attachments/1827617/2991610/07 ayk-2019-04-09-torino-dis.pdf
- a ECCE estimates from J. Huang

https://indico.bnl.gov/event/14715/contributions/59782/attachments/39682/65822/SiPMs%20for%20EIC%202-4-2022.pdf

only neutron fluence > 100 keV is reported for a given luminosity exposure. The two sets seem in contradiction (see next slides)

- an ATHENA estimate by Yuri Fysiak: https://www.star.bnl.gov/~fisyak/star/Flux_2017_ATHENA/

Neutron fluxes (total, > 100 keV , < 250 meV)

Neutron vertex production

Charged hadrons fluxes (total, > 100 keV)

Charged hadron vertex production

Electron fluxes (total, > 100 keV, < 250 meV)

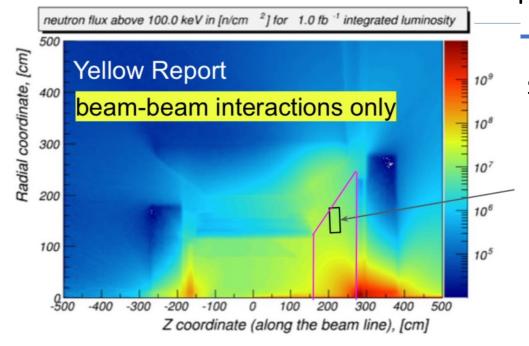
Gamma and muons

Deposited energy

Dose

How much radiation@EIC? YR/ECC estimates

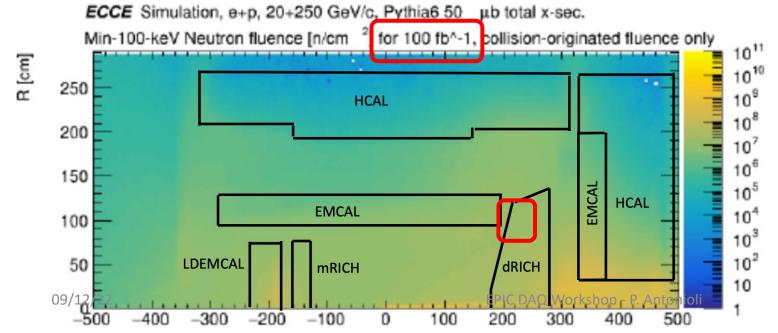




Source: Yellow Report

Only fluences, but better TID for cumulative damages and instantaneous fluxes (for SEU)

potential location of dRICH sensors $1-5\ 10^7\ \text{neq/cm}^2\ \text{every}\ 1\ \text{fb}^{-1}$ (*) note computation is for neutron > 100 keV

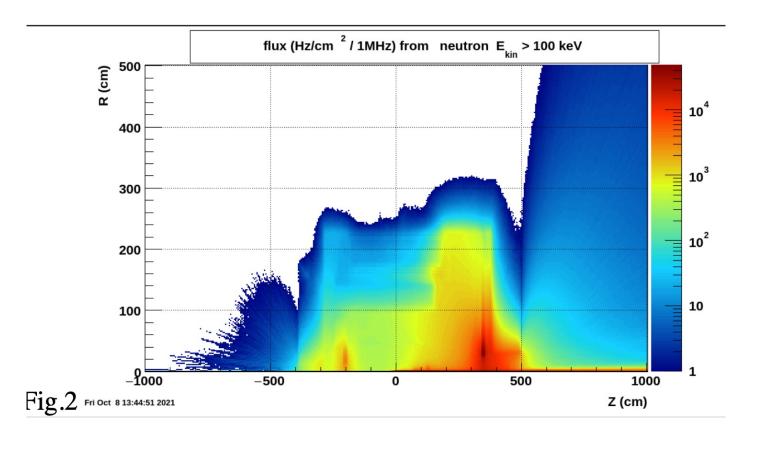


here it looks 5 10⁷ every 100 fb⁻¹ a factor 100 discrepancy?

Note factor 100 seems also "elsewhere" for example at x=0, Z=-180 just to make an example

How much radiation@EIC? ATHENA estimates





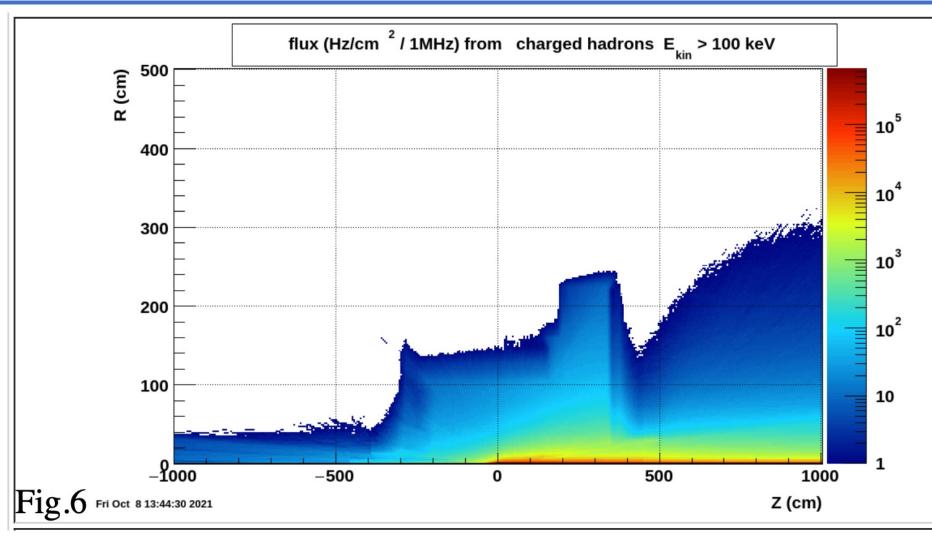
At z,x (200,100) we have $2x10^3$ Hz/cm² / 1MHz \rightarrow 10³ Hz/cm²

30 weeks @ $10^{34} = 100 \text{ fb}^{-1}$

- \rightarrow 30 Weeks = 30x7x8.6 10⁴ s = 10⁷ s
- \rightarrow 10³ Hz/cm² x 10⁷ s \rightarrow 10¹⁰ n with E>100 kev every 100 fb⁻¹
- → looks closer to AK predictions....

Note: plots normalized at 1 MHz collision rate at 18x275 Assuming maximum rate 500 kHz we get fluxes dividing these values by 2 (it is not fully correct at 18x275 but ok...)





for SEU are relevant hadrons > 20 MeV, let's keep what we have for charged hadrons

At 200,100 this gives fluxes at 10² Hz/cm² that is well affordable!

(ALICE-TOF in Run3 at 260 Hz/cm², outer ITS at 9000 Hz/cm²)

is this value an issue for SEU?

Note: plots normalized at 1 MHz collision rate at 18x275 Assuming maximum rate 500 kHz we get fluxes dividing these values by 2 (not fully correct but ok...)

dRICH case and some known FPGAs



Assumptions:

- 10² Hz/cm² hadrons > 20 MeV inst. Flux
- 310 FPGA on dRICH FEB

Note about RDO:

The FPGA+ opt. transceiver on FEB will manage the front-end counterpart of the RDO.

FPGA	SEL σ cm²/device	RAM SEU o cm²/bit	conf. upset rate/device (s)	MTBF (CONF) in the system (days)
Xilinx Ultrascale+ (1)	YES (8 10 ⁻¹²)	2 10 ⁻¹⁵	O(10 ⁸)	O (4 days)
Microsemi IGLOO2 (2)	NO (Sil. Rev>1)	2 10-14	0 (FLASH)	0
Microchip PolarFire (3)	NO	1.5 10 ⁻¹⁴	0 (FLASH)	0

(1)

- Microsemi, SmartFusion2 and IGLOO2 Neutron Single Event Effects (SEE)
- M. Giacalone, "Development of qualification procedures for DRM2 acquisition boards of the ALICE-TOF detector", UniBo Master Thesis, 2018 → results on IGLOO2
- (3) A. Scialdone, <u>"FPGA qualification for the LHC radiation environment"</u>, Master Thesis, Politecnico di Torino -→ results on PolarFIre and NanoXplore

This table is not "a result. Just first back on the envelope computation post a modest-Google effort

Life is more complicated: Flip/Flop, PLL upsets, Triple-Module Redundancy (TMR) + CRC mechanisms, SEFI, ...

[•] R. Koga et al, "Heavy Ion and Proton Induced Single Event Effects on Xilinx Zyng UltraScale+ Field Programmable Gate Array (FPGA)", 10.1109/NSREC.2018.8584319 >> SEL reported

[•] P. Maillard et al, Total Ionizing Dose and Single-Events characterization of Xilinx 20nm Kintex UltraScale, <u>10.1109/RADECS47380.2019.9745695</u>, → no SEL reported (2)

Tests are important and SEL are real....



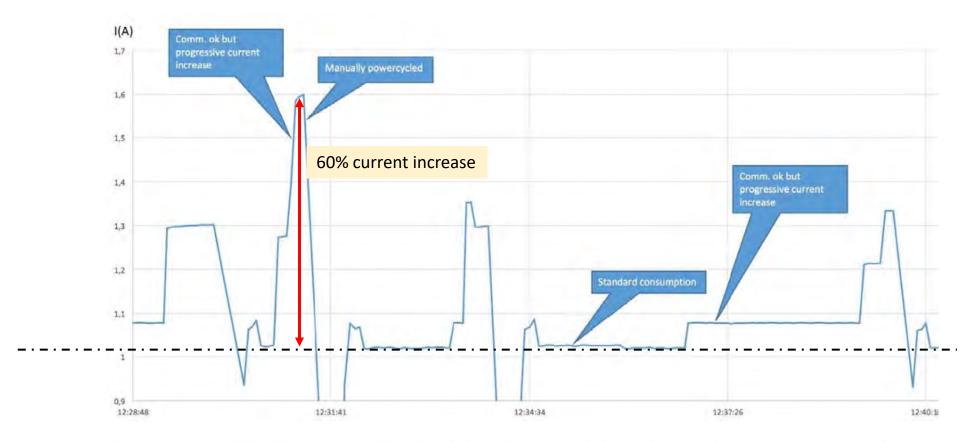


Figure 5.13: Total current absorbed by the tested board as a function vs time during irradiation tests in 2016.

Our (ALICE-TOF) test @ Trento protontherapy center 100 MeV proton beam on IGLOO2 FPGA (Silicon Version 1, back in 2016). Latchups were reported by many groups at that time to Microsemi! IGLOO2 are now deployed at LHC/ALICE (with silicon version > 1;-)).

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Some suggestions/food for discussion about EPIC next steps in this area



- consolidate ASAP estimates of fluences for 1-MeV n_{eq}/cm^2 , TID, and flows for hadrons > 20 MeV in EPIC
- agree a conservative reference official running scenario ("10 years at max lumi?")
- establish central database/Twiki collecting components to be deployed in FEE boards [
 FEB] (ASIC, FPGA, ... + all the others as optical transceivers, etc.)
- Share libraries for implementation of mitigation strategies (typically TMR), have common repository
- collect data of radiation tests done for qualification (sharing among groups!) on different components + collect already existing literature on candidate FPGAs
- Engineering Design Review and Production Readiness Review for electronics of each sub-system should include radiation tolerance aspects
- DAQ WG task group charged to define the "DAQ link" (timing, control, data) and related hardware should benchmark protocol/proposed hardware with radiation tests (BERR, lost link, clock recovery, PLL, ...)

• ...

