2022 EIC DAC Meeting on October 19-21, 2022

Indico page: https://indico.bnl.gov/event/17159/

- EIC project update on Oct 19 9:30-10:15am EDT
- Update on EPIC on Oct 19 10:15-11:15am EDT
- eRD112 presentation (20+10') on **Oct 20 10:10-10:40am EDT**
  - open R&D questions to be complete the R&D program before CD-3
  - milestones for FY2022
  - results from FY2022
  - plans/proposals for FY2023.
- eRD109 presentation (20+10') on **Oct 21 10:00-10:30am EDT**
- Close-Out on Oct 21 12:30-13:15pm EDT

EIC R&D Detector Advisory Committee:

Marcel Demarteau (ANL, chair), Carl Haber (LBNL), Ian Shipsey (Oxford), Rick VanBerg (Penn), Jerry Va'vra (SLAC), Glenn Young (JLab), Peter Krizan (University of Ljubljana, Ljubljana), Blair N. Ratcliff (SLAC)

EIC AC-LGAD R&D FY22 Report and FY23 Proposal

Brookhaven National Laboratory: E.C. Aschenauer, G. Giacomini, A. Jentsch, A. Kiselev, P. Shanmuganathan, P. Tribedy, A. Tricolli, T. Ljubicic, Z. Xu
Fermi National Accelerator Laboratory: A. Apresyan, R. E. Heller, C. Madrid, C. Pena, S. Xie, T. Zimmerman
Los Alamos National Laboratory: X. Li
Oak Ridge National Laboratory: O. Hartbrich, K. F. Read, C. Loizides
Purdue University: A. Jung
Rice University: F. Geurts, W. Li
University of California, Santa Cruz: S. Mazza, J. Ott, A. Seiden, S.H. Sadrozinski, B. Schumm
University of Illinois at Chicago: O. Evdokimov, S. Nanda, Z. Ye
IJCLAB/OEMGA/CEA-Irfu (France): A. Ba, J.-J. Dormard, B.Y Ky, D. Marchand, C. Munoz Camacho, E. Rauly, L. Serin, A.-S. Torrento, P.-K. Wang, P. Dinaucourt, N. Seguin-Moreau, C. de La Taille, M. Morenas, F. Bouyjou
National Cheng Kung University/Academia Sinica (Taiwan): W.-C. Chang, P.-J. Lin, Y. Yang

Institutions have expressed interests and plan to join future efforts:
Massachusetts Institute of Technology, Ohio State University
National Institute of Science Education and Research (India)
Hiroshima University (Japan), Nara Women's University (Japan), RIKEN (Japan)
South China Normal University (China), University of Science and Technology of China (China)

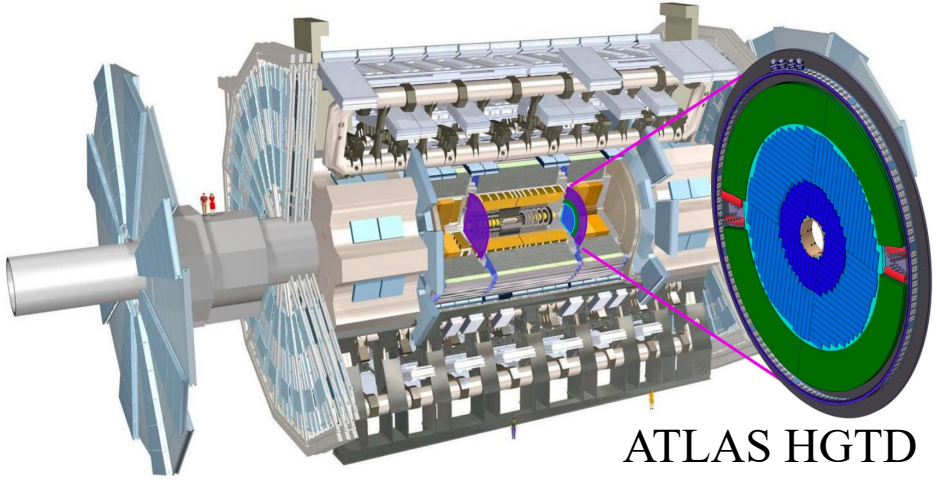
AC-LGAD Technology

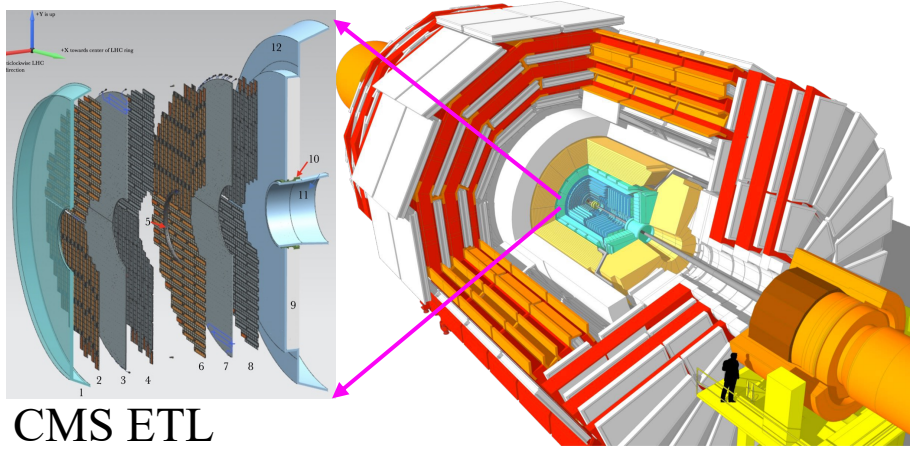
- Precise timing detectors based on DC-LGAD being built by ATLAS (6.4 m^2) and CMS (14 m^2) for data taking in 2028+.

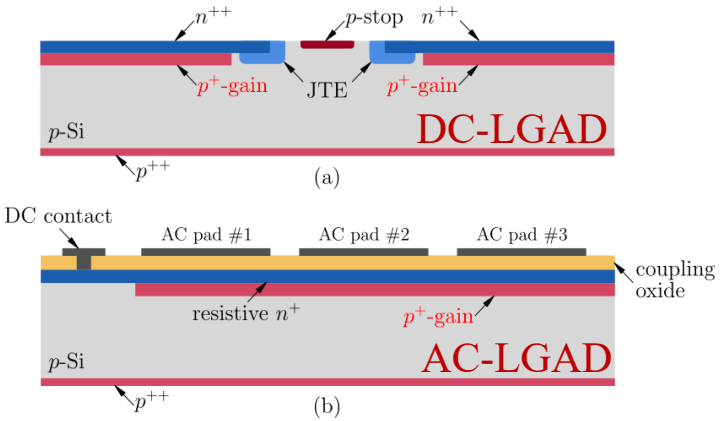
- AC-LGAD can not only provide precise timing resolution like DC-LGAD, but also 100% fill factor and much better spatial resolution with signal sharing.

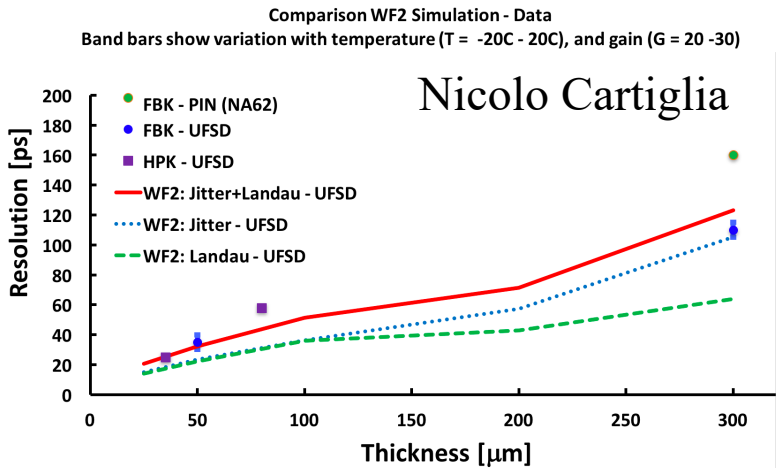
- AC-LGAD proposed for EIC experiments
  - TOF PID and tracking for central detectors
  - Timing and tracking for forward detectors

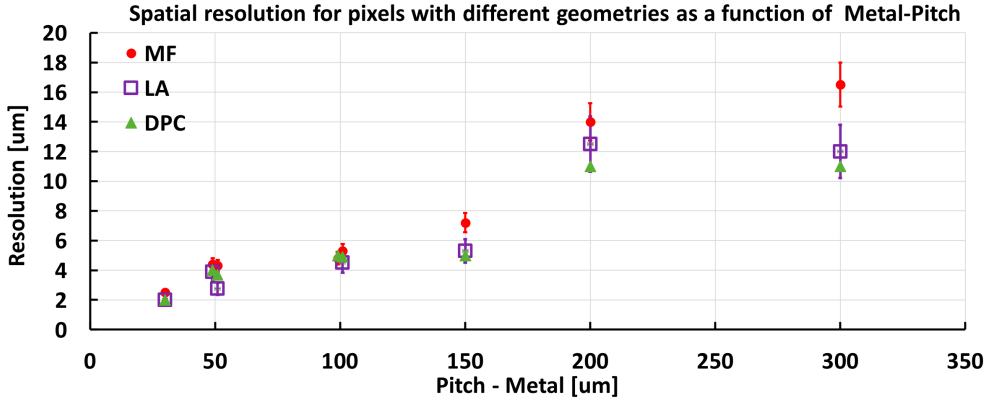
  with common designs in sensor, ASIC etc. where possible.



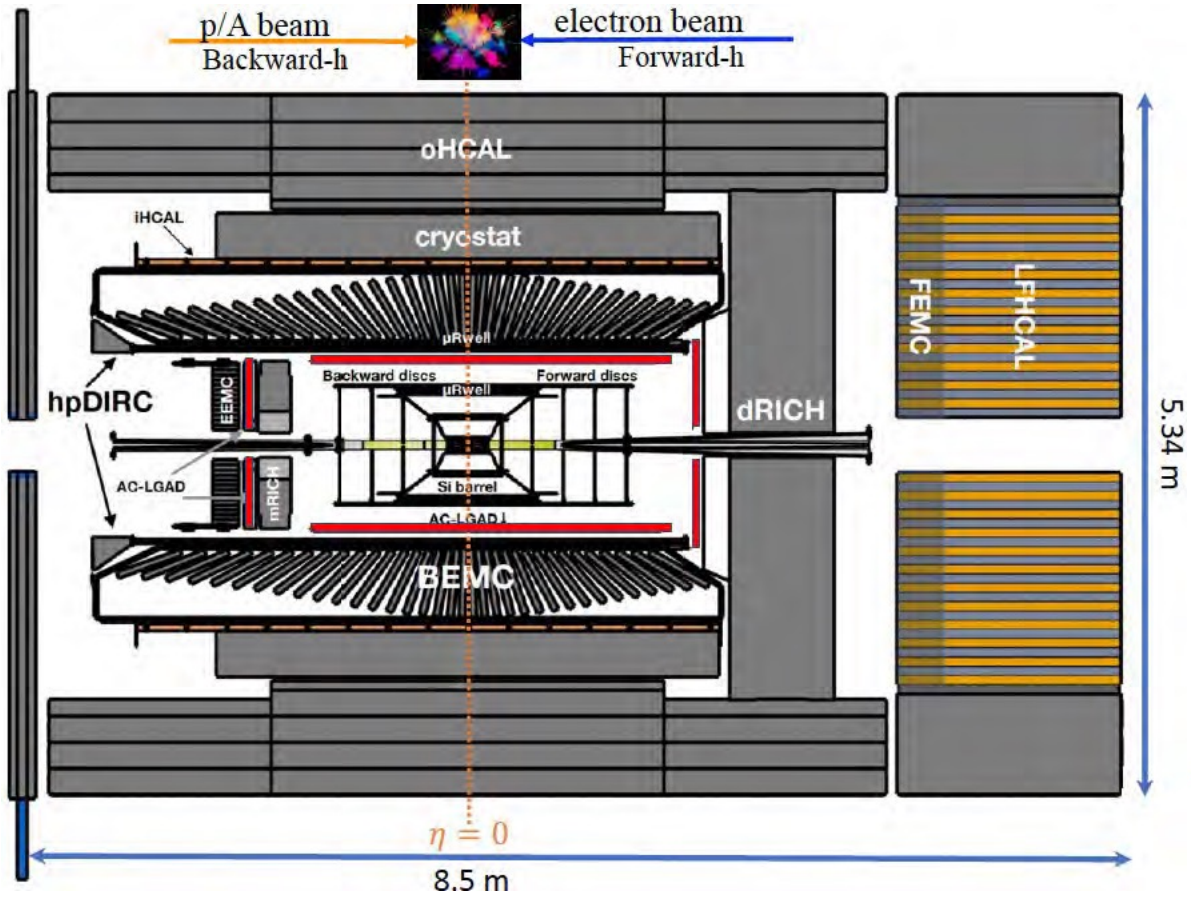


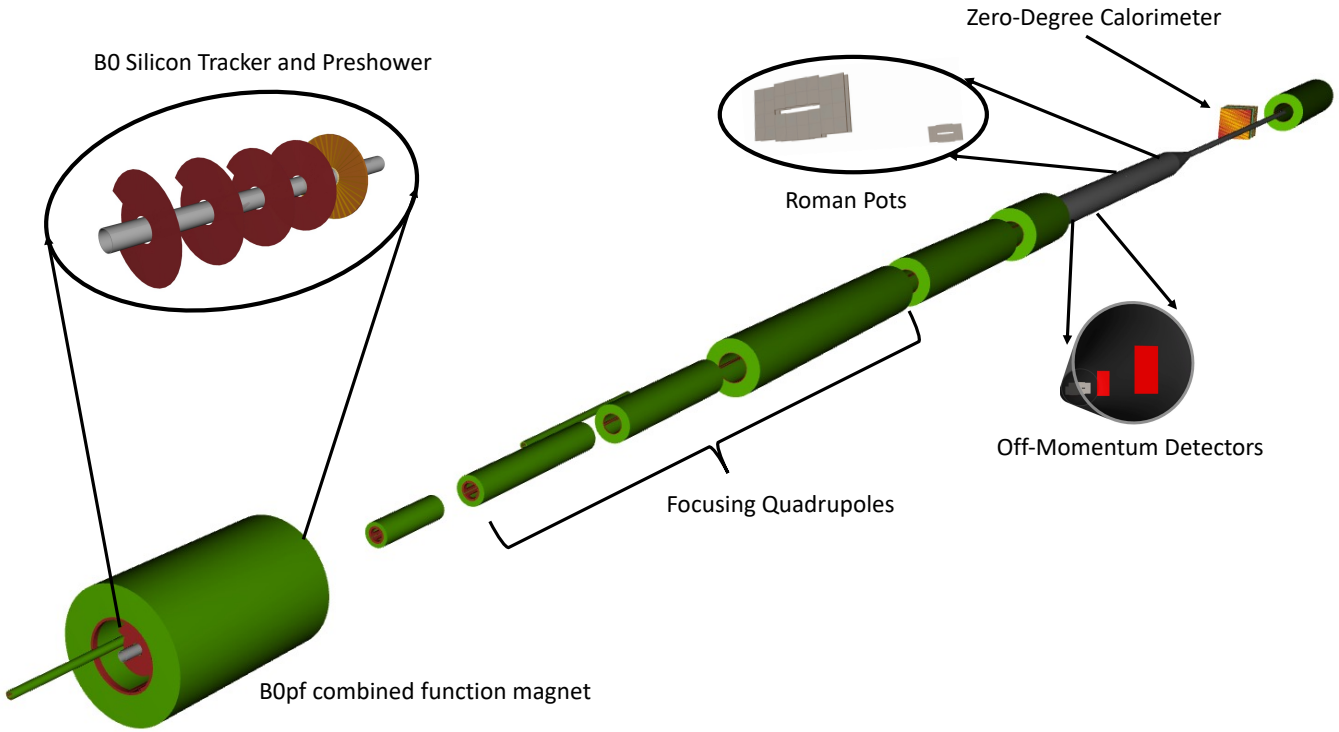






AC-LGAD Detectors for EPIC





	Area (m^2)	Time resolution	Spatial resolution	Material budget
Barrel Timing Tracking Layer	11	30 ps	30 μm in $r \cdot \phi$	0.01 X_0
Endcap Timing Tracking Layers	1.2+2.2	25 ps	30 μm in x and y	0.08 X_0
B0 Tracker	0.07	30 ps	$500/\sqrt{12}$ μm	0.01 X_0
Roman Pots	0.14	30 ps	$500/\sqrt{12}$ μm	no strict req.
Off-Momentum Detectors	0.08	30 ps	$500/\sqrt{12}$ μm	no strict req.

Table 1: Specifications of AC-LGAD detectors for EPIC, the EIC project detector. The timing and spatial resolutions are given for single hits, while the material budgets are given per detector layer.

Requirements on the timing and spatial resolutions and material budget are still being evaluated and are subject to changes as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

Open R&D questions to be addressed before CD-3

- **AC-LGAD sensor:**
  - Goal: large area sensors that meet timing/spatial resolution requirements with minimal # channels
  - Approach: utilize BNL IO to optimize the sensor design (pitch, electrode width, n-layer doping density, active volume thickness); engage commercial vendors to verify sensor quality and production cost/yield
- **Frontend readout ASIC:**
  - Goal: low jitter (15-20ps) and low power (1 mW/channel), streaming readout with TDC and ADC outputs
  - Approach: custom-designed EICROC and FCFD, ASICs from 3rd party institutions
- **Sensor/ASIC integration**
  - Goal: reliable and cost-effective way to establish connections between AC-LGAD sensor and frontend ASIC
  - Approach: bump-bonding, wire-bonding, interposer
- **Mechanical structure with cooling:**
  - Goal: light-weight structure with cooling that meet the material budget, thermal and mechanical requirements
  - Approach: finite element analysis and prototyping with carbon-fiber composite and PEEK materials
- **Flex and frontend electronics:**
  - Goal: low jitter clock to frontend ASICs (<5 ps), low X_0 flexible PCB to route power/signal to sensor/ASIC
  - Approach: design a precise clock distribution system in concert with EPIC DAQ group, design and prototype flexible PCB that meet the requirements; work with EPIC DAQ to define the streaming readout scheme

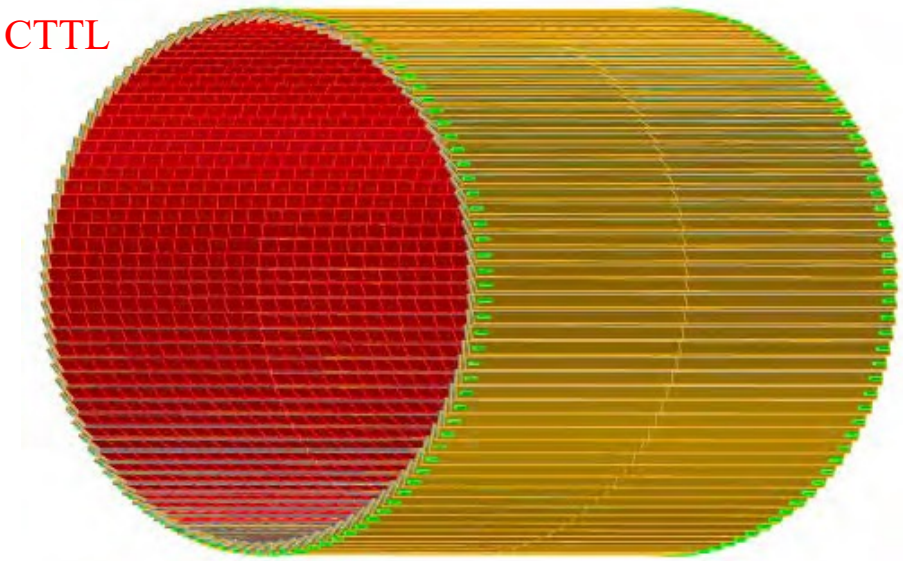
FY22 Deliverables (in FY22 Proposal)

- High-level strawman layout design and requirements for sub-systems using AC LGADs.
- Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes to optimize performance by BNL Instrumentation and HPK.
- Start production of sensors of small thickness (20, and 30 microns) for ToF applications with time resolution 20 ps by BNL Instrumentation.
- A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 micron pitch and 20 ps time resolution.

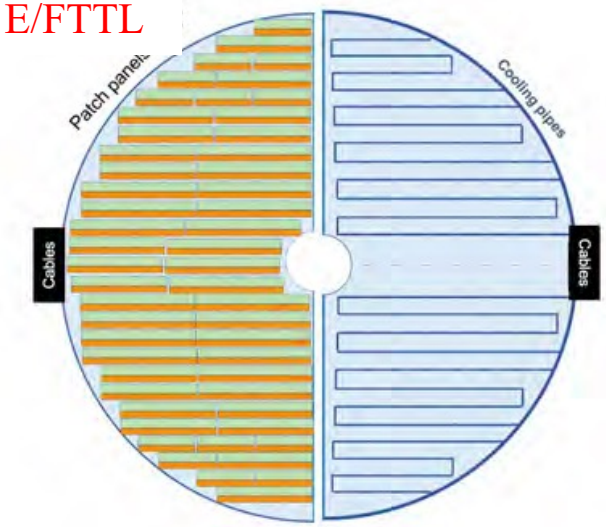
FY22 Deliverable #1

- High-level strawman layout design and requirements for sub-systems using AC LGADs.

CTTL



E/FTTL



Roman Pots

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
CTTL	10.9	0.5*10	2.4M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
E/FTTL	1.20/2.22	0.5*0.5	4.8M/8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	140 μm in x and y	0.01 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

Requirements on timing and spatial resolutions and material budget are still being evaluated and are subject to change as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

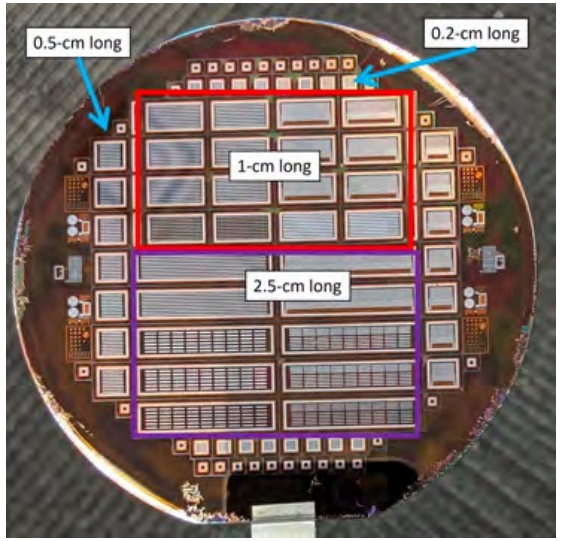
FY22 Deliverables #2 and #3

2. Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes to optimize performance by BNL IO and HPK.

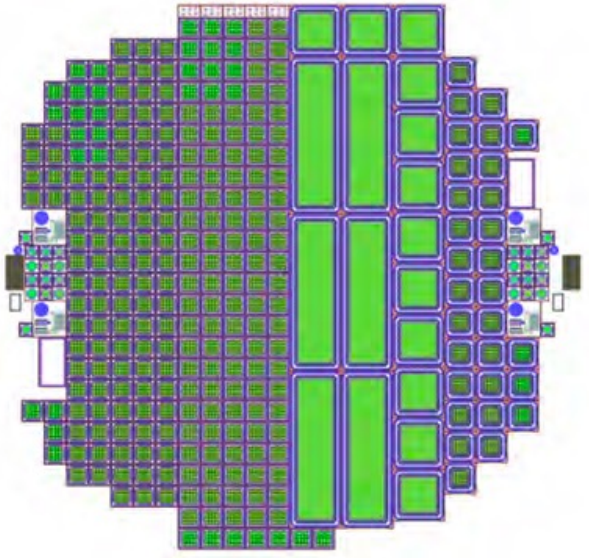
3. Start production of sensors of small thickness (20 and 30 microns) for ToF applications with time resolution 20 ps by BNL Instrumentation.

- 1st BNL IO (6-11/2021): 5-25 mm strips with 500 μm pitch, 100-300 μm electrode width, 50 μm active Si
- 2nd BNL IO (6-10/2022): 5-25 mm strips with 500-700 μm pitch, 50-100 um electrode width, 20-50 μm Si
- 3rd BNL IO (8-12/2022): pixels with 500 μm pitch, 20-50 μm active Si
- Joint HPK production with US-Japan (6/2022-2/2023): strip and pixel sensors with different pitch, electrode width, active Si thickness and n^+-layer doping

1st/2nd BNL Production

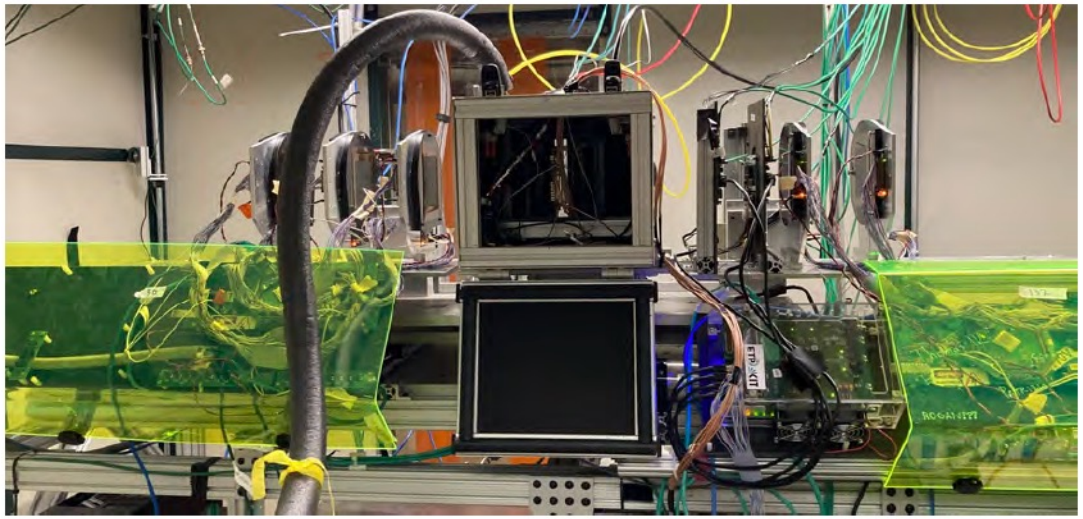


3rd BNL Production



Joint HPK Production

FY22 Deliverables #2 and #3



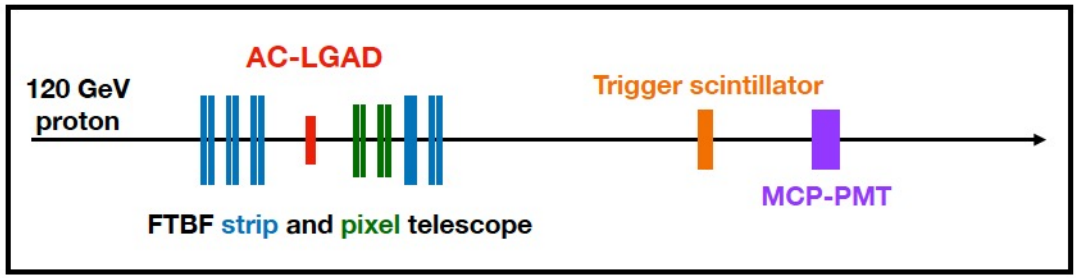


Figure 7: Picture (top) and diagram (bottom) of the FTBF silicon telescope and reference instruments used to characterize AC-LGAD performance. The telescope comprises five pairs of orthogonal strip layers and two pairs of pixel layers, for a total of up to 14 hits per track.

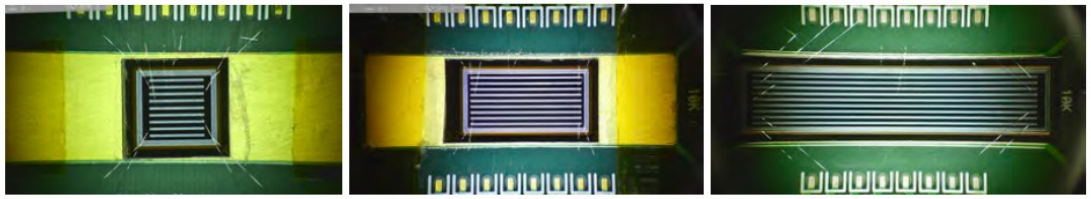
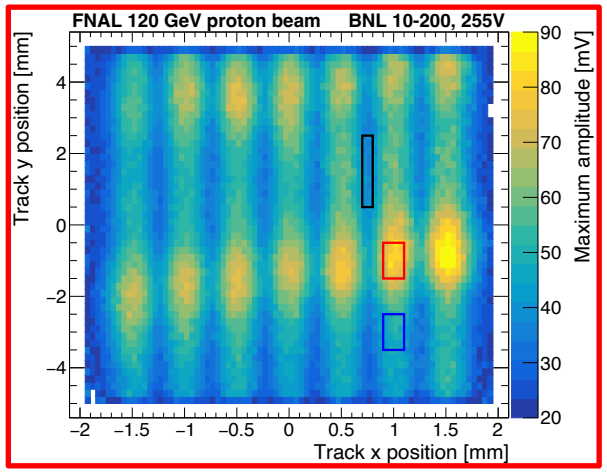
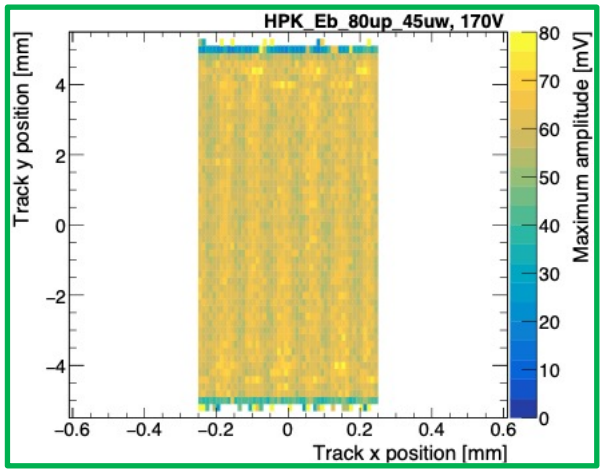


Figure 8: Three AC-LGAD strip sensors wire-bonded on Fermilab test board and tested at FTBF: BNL 5-200 (left), BNL 10-200 (middle) and BNL 25-200 (right). See text for details.





Name	Time resolution		Exactly one strip		Two strip	
	Overall	Hot region	Resolution	Fraction	Resolution	Fraction
Unit	ps	ps	μm	-	μm	-
BNL 5–200	35 ± 1	30 ± 1	52 ± 1	35%	12 ± 1	65%
BNL 10–100	42 ± 1	35 ± 1	28 ± 1	23%	19 ± 1	77%
BNL 10–200	42 ± 1	32 ± 1	55 ± 1	43%	18 ± 1	57%
BNL 10–300	40 ± 1	36 ± 1	78 ± 1	51%	16 ± 1	49%
BNL 25–200	72 ± 1	51 ± 1	71 ± 1	82%	31 ± 1	18%

Table 4: Test beam results of AC-LGAD strip sensors from the first batch of BNL production.

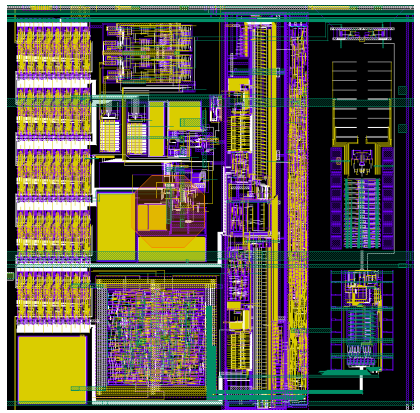
- Non-uniform gain in sensors from 1st BNL production, not in HPK sensor for US-Japan coll. New implantation approach at BNL to fix it.
- Timing and spatial resolutions in the hot region of 1 cm long strip sensors from 1st BNL production are comparable to those of 500x500 μm^2 pixel sensors from HPK (~30 ps, 25 μm), making strip sensors a promising candidate for EIC applications.

FY22 Deliverable #4

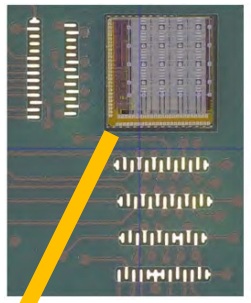
4. A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 micron pitch and 20 ps time resolution.

EICROC0 (submitted in 3/2022, received in 7/2022) by OMEGA/CEA Irfu/AGH/IJCLab

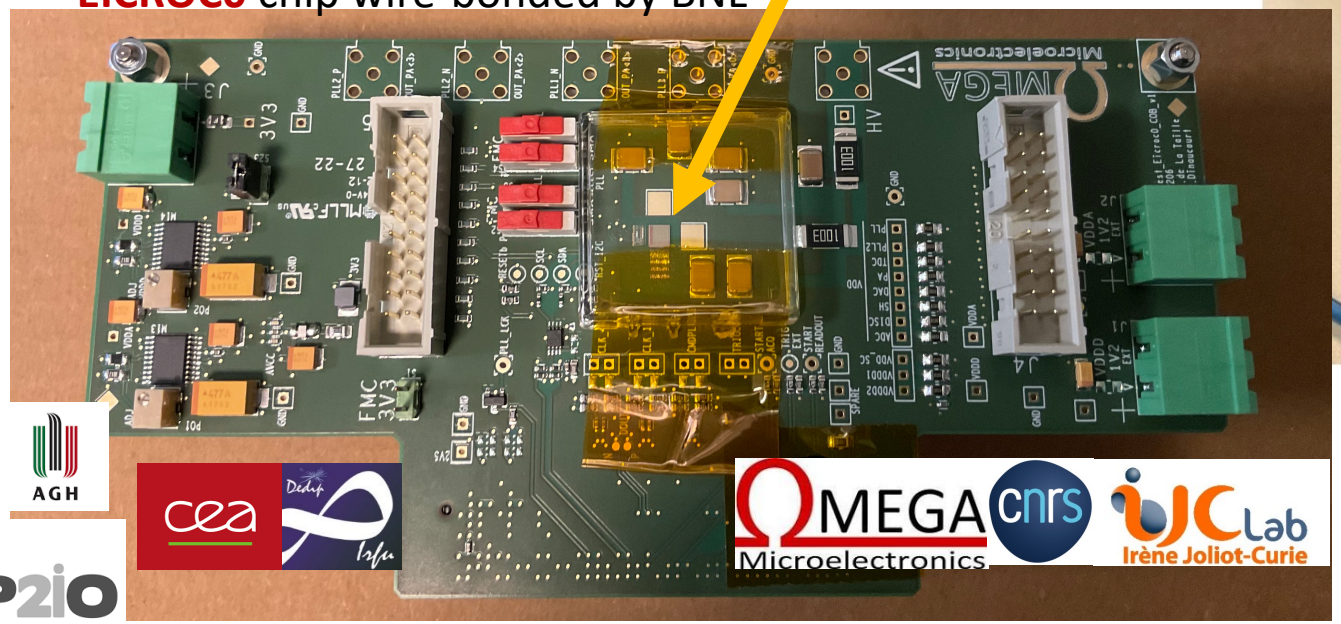
- 4 x 4 channels
- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TDC (TOA) adapted by CEA-Saclay/Irfu
- ADC (40 MHz) adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)



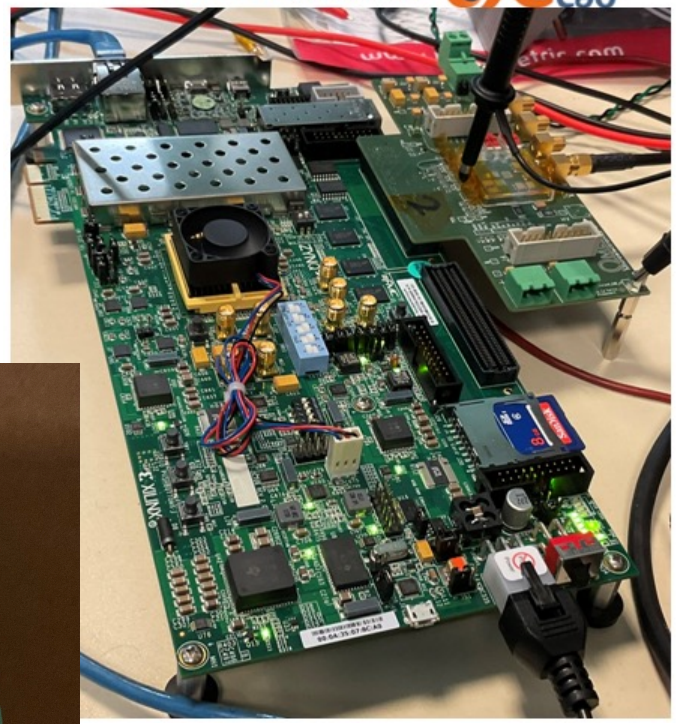
EICROC0, *1 channel implantation*



EICROC0 chip wire-bonded by BNL



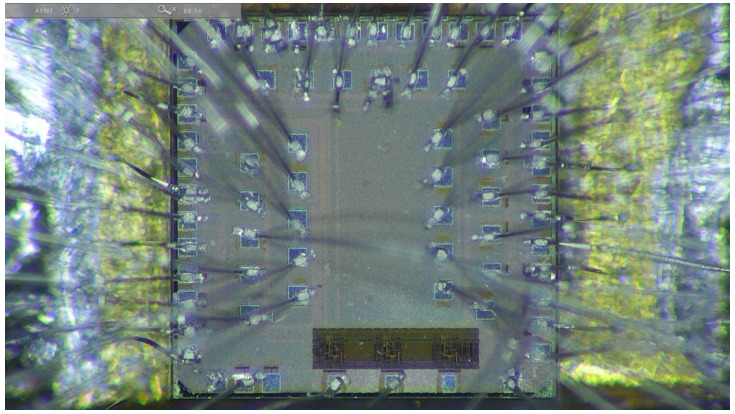
EICROC0 Test bench at IJCLab



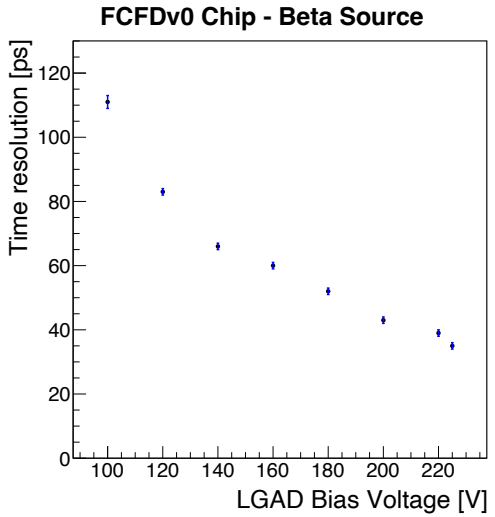
FY22 Deliverable #4

FCFD0 (submitted in 2021 and received in 2022 by Fermilab)

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel when a CFD is paired with a TDC, one time measurement gives the final answer.
- Charge injection and beta source tests consistent with expectation. Tests with beam are planned

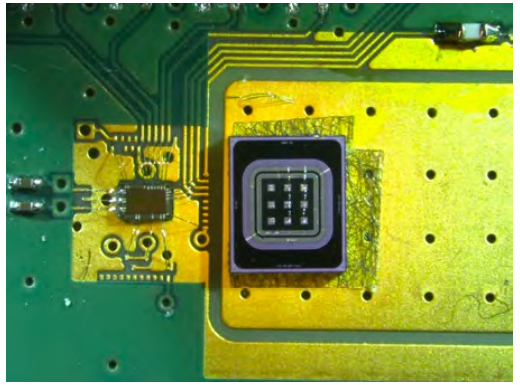


FCFD0

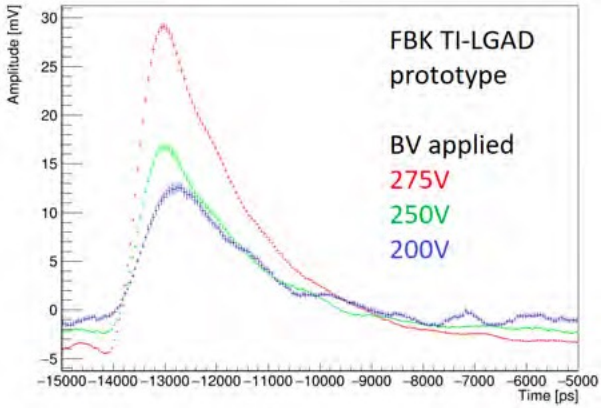


ASIC Efforts at UC Santa Cruz

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations, final Layout, Board design



HPSoC



FY23 Plan/Proposal

- AC-LGAD Sensor (eRD112)
  - Productions by BNL IO and HPK/FBK
  - TCAD simulation, sensor characterization in the lab/beam, irradiation test
- Frontend readout ASIC (eRD109)
  - EICROC0 lab/beam test, EICROC1 submission
  - FCFD0 beam test, FCFD1 submission
  - Characterization of ASICs from 3rd party institutions
- Sensor/ASIC integration (eRD112)
  - Interposer to connect pixelated ASICs with strip sensors, or pixel sensors with various pitch
- Frontend electronics (eRD109)
  - Timing, streaming readout, low-density flexible PCB, service hybrids
- Mechanical structure (eRD112)
  - Light-weight structure made from carbon-fiber composite materials and/or PEEK

FY23 Resource Requests by eRD112

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Sensor Production				**175**
BNL IO	Sensor fabrication (incl. labor)	50 (10 wafers)	1.5	75
HPK/FBK	Sensor fabrication	75+3-5/wafer	1	100
Sensor Characterization				**13.7**
UIC	M&S for test beam setup	-	-	5
LANL	M&S for irradiation test	-	-	5
SCIPP	Fermilab 16-channel boards	-	-	3.7
Sensor/ASIC Integration				**30**
UIC	Interposer fabrication and bump-bonding	30	1	30
Mechanical Structure				**15**
NCKU	Material for light-weight support structure	-	-	10
Purdue	Material for light-weight support structure	-	-	5
Travel				**21**
BNL	Trips to Fermilab testbeam	2	2	4
UIC	Trips to Fermilab testbeam	1	5	5
ORNL	Trips to Fermilab testbeam	3	2	6
Rice	Trips to Fermilab testbeam	3	2	6
TOT.				**254.7**

Table 8: eRD112 resource request for M&S costs in FY23, excluding frontend ASIC and electronics.

FY23 Resource Requests by eRD112

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Sensor R&D				**172.3**
BNL	Sensor+ASIC and test board assembly	El. Tech.	10	20
UIC	Sensor+ASIC and test board assembly	El. Tech.	10	15
	lab/beam test for sensors and ASICs	Research Sp.	50	45
LANL	Sensor irradiation test	Scientist	2.5	10
	Sensor irradiation test	Student	5	5
Rice	pixel sensor test	Postdoc	40	40
SCIPP	Oversight and coordination	Project Scientist	5	9
	TCAD sim. and sensor design	El. Design Specialist	10	16.5
	Prototype Assembly	EM Engineer	5	11.8
Sensor/ASIC Integration				**15**
UIC	interposer design and testing	El. Engineer	10	15
Mechanical Structure				**20**
NCKU	light-weight support structure R&D	Mech. Engineer	10	5
Purdue	light-weight support structure R&D	Mech. Engineer	10	15
TOT.				**207.3**

Table 9: eRD112 budget request for labor costs in FY23, excluding frontend ASIC and electronics.

FY23 Resource Requests by eRD109

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Frontend ASIC				**118.3**
IJCLAB	EICROC1 submission	65	1	65
	EICROC test boards	-	-	10
FNAL	FCFDv1 submission	25	1	25
	FCFD test boards	-	-	15
SCIPP	ASIC service boards	-	-	3.3
Frontend Readout Electronics				**31**
BNL	Xilinx Dev Kit	4	1	4
	Timing cihps and boards	15	-	15
ORNL	Xilinx Dev Kit	4	1	4
	M&S	8	-	8
TOT.	-	-	-	**149.3**

Table 10: eRD109 budget request for M&S costs in FY23 on frontend ASIC and electronics.

FY23 Resource Requests by eRD109

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Frontend ASIC				**29.7**
SCIPP	Service board design layout	Electronic Design Specialist	7.5	12.4
	Board Assembly	Electro-Mechanical Engineer	5	11.8
	Board loading and lab msmt	Assistant specialist	5	5.5
Frontend Readout Electronics				**88**
BNL	Readout and Timing Distribution	Research Associate	20	38
ORNL	Barrel TOF Low-Mass Service Hybrid	Electric Engineer	10	32
Rice	Endcap TOF Service Hybrid	Electric Engineer	15	18
TOT.	-	-	-	**117.7**

Table 11: eRD109 budget request for labor costs in FY23 on frontend ASIC and electronics.

FY23 Deliverables

- Sensor prototype with 30 ps time and space resolution match RPs and Tracker;
  Sensor prototype with 20 ps time resolution for ToF
- 1st sensor + ASIC demonstrator for EIC applications and testing with particle beam.
- 2nd ASIC prototype submissions with better performance and extended features.
- Irradiation campaign for sensor and ASIC prototypes.
- Design and prototype of flexes, interconnects and off-detector electronics.
- Design and prototype of light-weight structure with embedded cooling tubes

eRD112
- Sensor R&D (382k$)
  - BNL, HPK/FBK productions
  - Lab/beam test, irradiation test
- Sensor/ASIC integration (45k$)
  - Interposer
- Mechanical structure ($35k)
  - Light-weight structure with cooling

eRD109
- Frontend ASICs (148k$)
  - EICROC1, FCFD1, SCIPP
- Frontend electronics (119k$)
  - Clock distribution system
  - Streaming readout
  - Low-mass flexible PCB
  - Service hybrid

EPIC Simulation
- Geometry model, digitization and reconstruction
- Requirements on spatial, timing resolutions, and material budget

Project Engineering Design
- Engineering design for pre-TDR
- Integration & services

Sensor **ASIC** **Prototype Module** **Services**

FY23 Resource Requests by eRD112

Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Sensor Production				**175**
BNL IO	Sensor fabrication (incl. labor)	50 (10 wafers)	1.5	75
HPK/FBK	Sensor fabrication	75+3-5/wafer	1	100
Sensor Characterization				**13.7**
UIC	M&S for test beam setup	-	-	5
LANL	M&S for irradiation test	-	-	5
SCIPP	Fermilab 16-channel boards	-	-	3.7
Sensor/ASIC Integration				**30**
UIC	Interposer fabrication and bump-bonding	30	1	30
Mechanical Structure				**15**
NCKU	Material for light-weight support structure	-	-	10
Purdue	Material for light-weight support structure	-	-	5
Travel				**21**
BNL	Trips to Fermilab testbeam	2	2	4
UIC	Trips to Fermilab testbeam	1	5	5
ORNL	Trips to Fermilab testbeam	3	2	6
Rice	Trips to Fermilab testbeam	3	2	6
TOT.				**254.7**

Table 8: eRD112 resource request for M&S costs in FY23, excluding frontend ASIC and electronics.

Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Sensor R&D				**172.3**
BNL	Sensor+ASIC and test board assembly	El. Tech.	10	20
UIC	Sensor+ASIC and test board assembly	El. Tech.	10	15
	lab/beam test for sensors and ASICs	Research Sp.	50	45
LANL	Sensor irradiation test	Scientist	2.5	10
	Sensor irradiation test	Student	5	5
Rice	pixel sensor test	Postdoc	40	40
SCIPP	Oversight and coordination	Project Scientist	5	9
	TCAD sim. and sensor design	El. Design Specialist	10	16.5
	Prototype Assembly	EM Engineer	5	11.8
Sensor/ASIC Integration				**15**
UIC	interposer design and testing	El. Engineer	10	15
Mechanical Structure				**20**
NCKU	light-weight support structure R&D	Mech. Engineer	10	5
Purdue	light-weight support structure R&D	Mech. Engineer	10	15
TOT.				**207.3**

Table 9: eRD112 budget request for labor costs in FY23, excluding frontend ASIC and electronics.

FY23 Resource Requests by eRD109

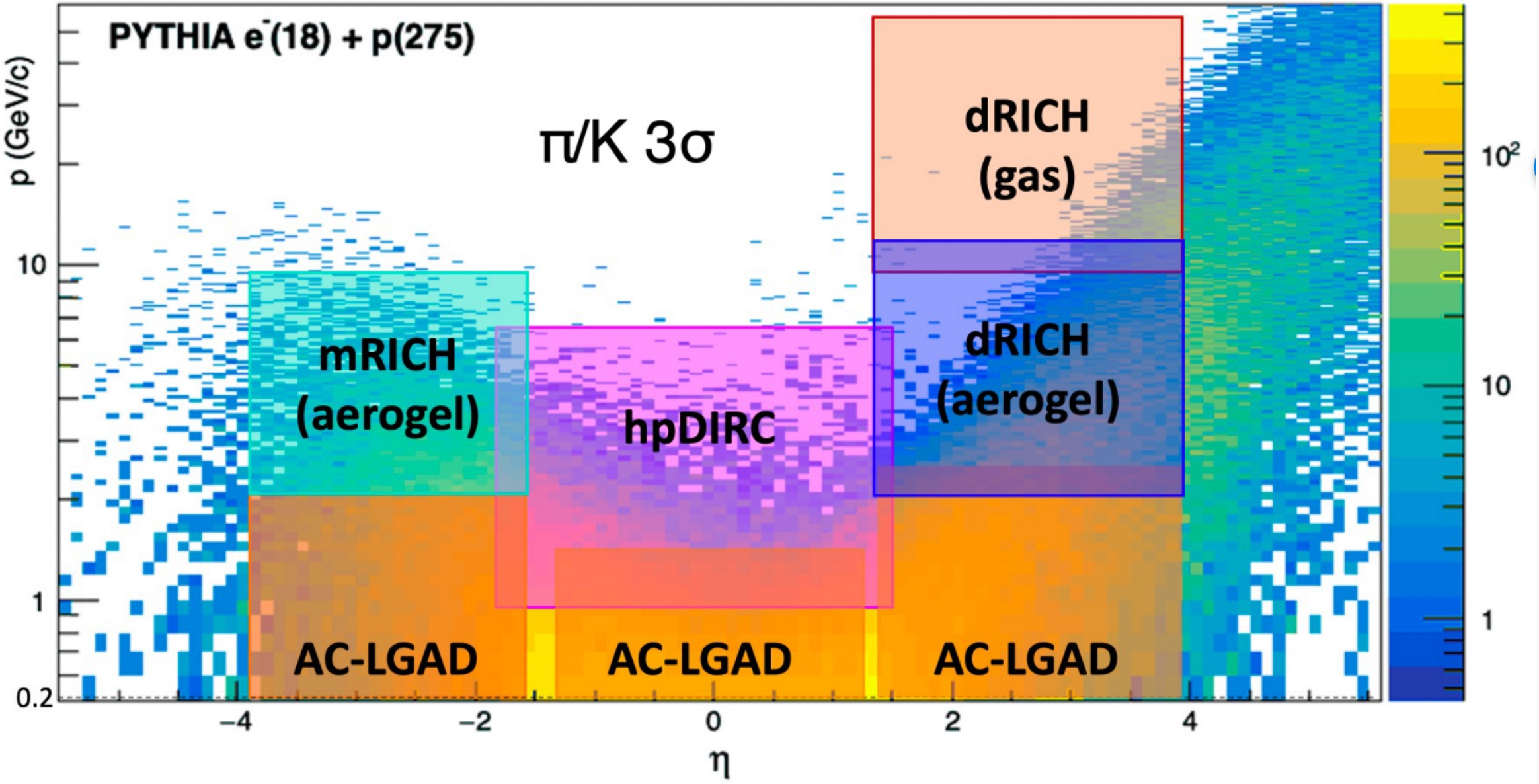
Vendor/ Institute	M&S Item	Cost per Item (k$)	N. Items	Tot. Cost (k$)
Frontend ASIC				**118.3**
IJCLAB	EICROC1 submission	65	1	65
	EICROC test boards	-	-	10
FNAL	FCFDv1 submission	25	1	25
	FCFD test boards	-	-	15
SCIPP	ASIC service boards	-	-	3.3
Frontend Readout Electronics				**31**
BNL	Xilinx Dev Kit	4	1	4
	Timing cihps and boards	15	-	15
ORNL	Xilinx Dev Kit	4	1	4
	M&S	8	-	8
TOT.	-	-	-	**149.3**

Table 10: eRD109 budget request for M&S costs in FY23 on frontend ASIC and electronics.

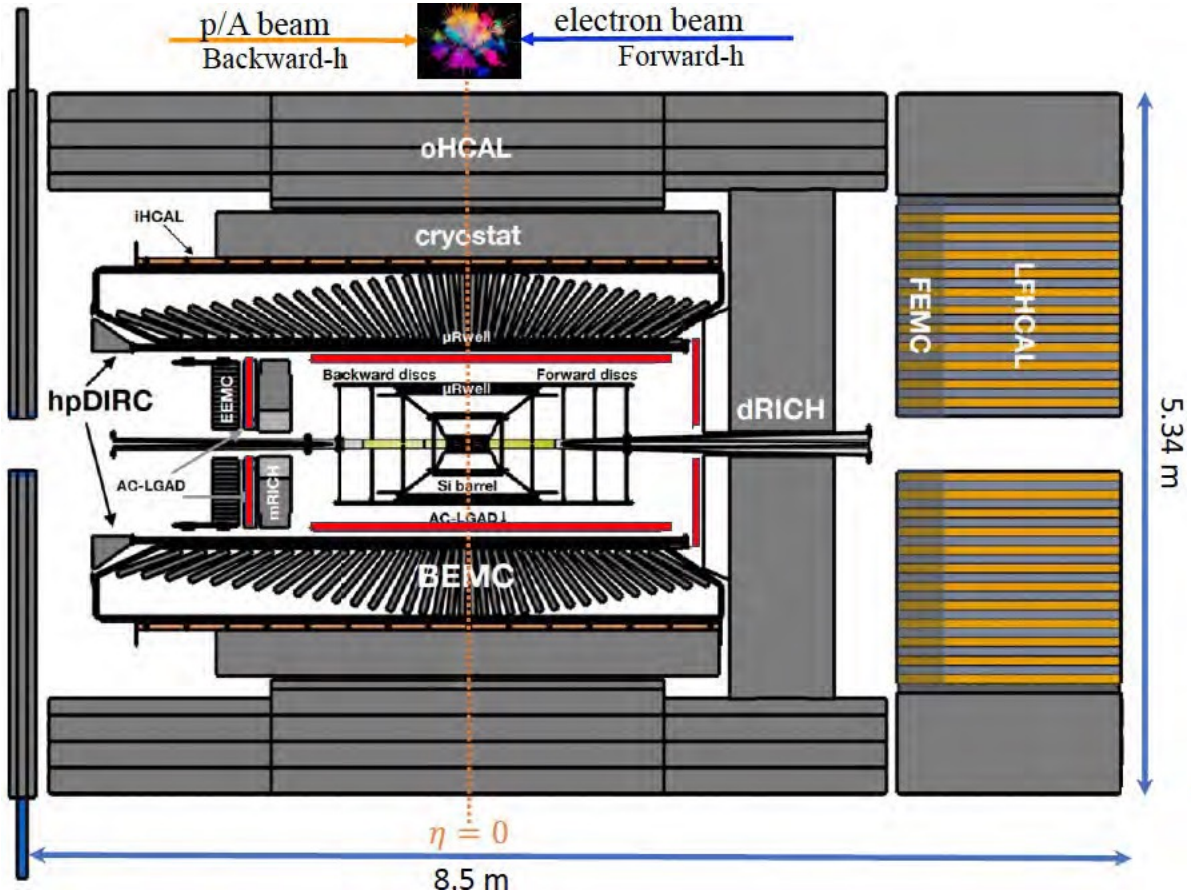
Inst.	Task	Labor Type	FTE (%)	Tot. Cost (k$)
Frontend ASIC				**29.7**
SCIPP	Service board design layout	Electronic Design Specialist	7.5	12.4
	Board Assembly	Electro-Mechanical Engineer	5	11.8
	Board loading and lab msmt	Assistant specialist	5	5.5
Frontend Readout Electronics				**88**
BNL	Readout and Timing Distribution	Research Associate	20	38
ORNL	Barrel TOF Low-Mass Service Hybrid	Electric Engineer	10	32
Rice	Endcap TOF Service Hybrid	Electric Engineer	15	18
TOT.	-	-	-	**117.7**

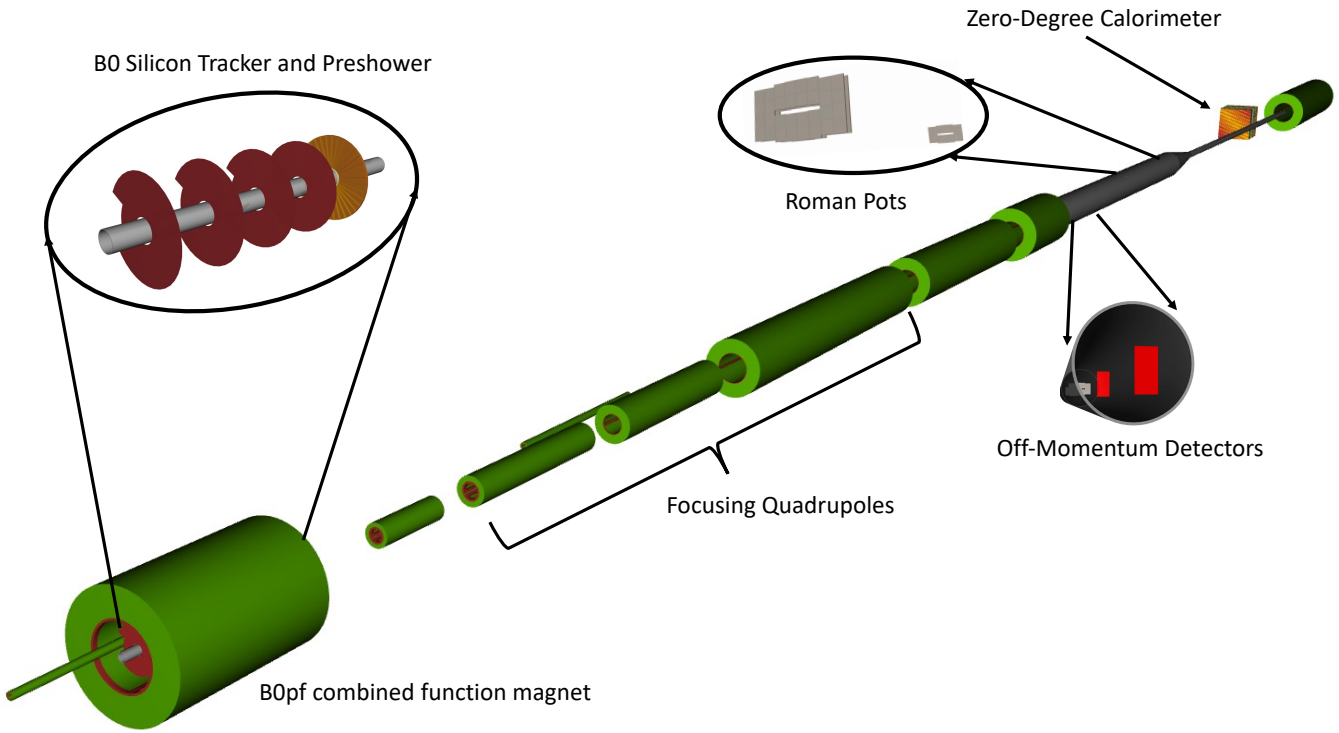
Table 11: eRD109 budget request for labor costs in FY23 on frontend ASIC and electronics.

PID for EPIC Experiment



AC-LGAD Detectors for EPIC



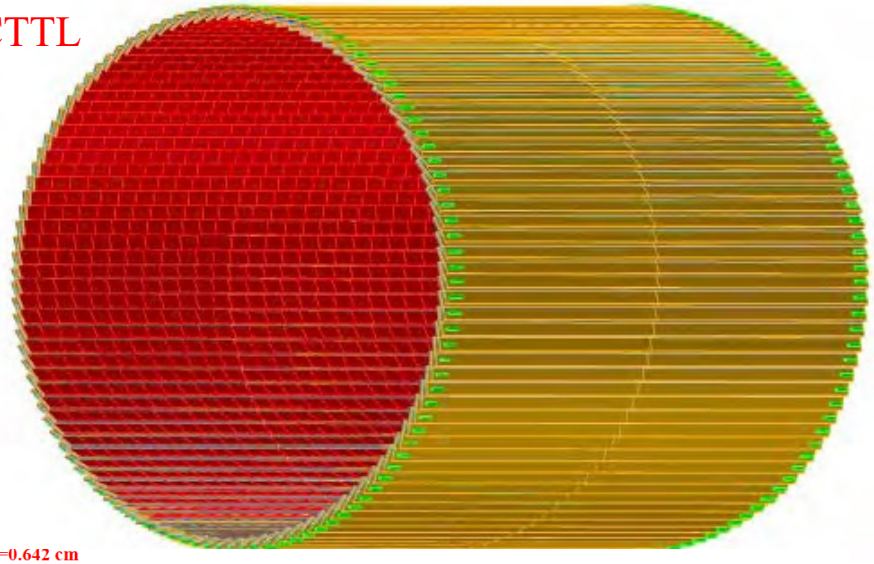


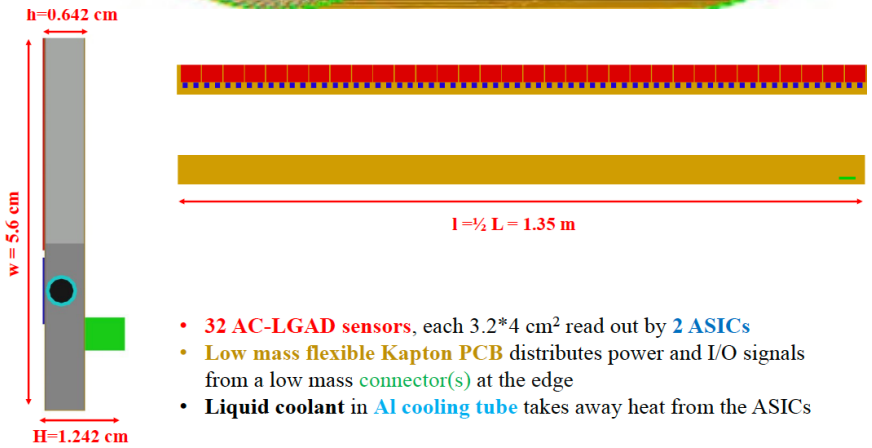
	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
CTTL	10.9	0.5*10	2.4M	30 ps	30 μm in $r \cdot \varphi$	0.01 X0
E/FTTL	1.20/2.22	0.5*0.5	4.8M/8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	140 μm in x and y	0.01 X0
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

FY22 Milestone #1

- High-level strawman layout design and requirements for sub-systems using AC LGADs.

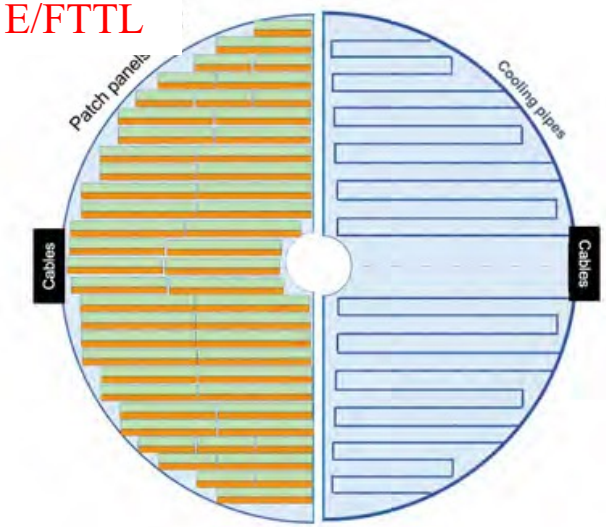
CTTL



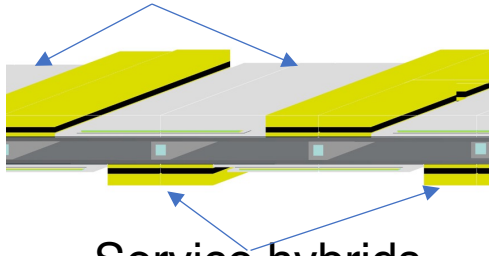


- **32 AC-LGAD sensors**, each 3.2*4 cm² read out by **2 ASICs**
- **Low mass flexible Kapton PCB** distributes power and I/O signals from a low mass connector(s) at the edge
- **Liquid coolant** in **Al cooling tube** takes away heat from the ASICs

E/FTTL

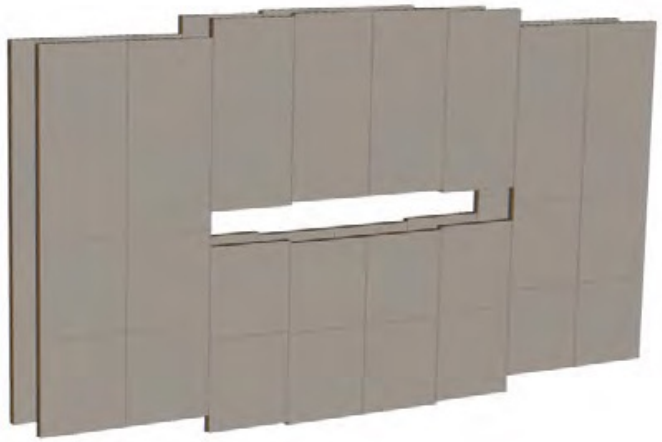


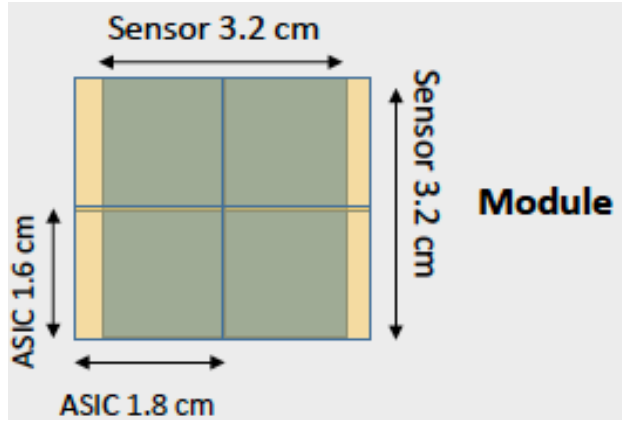
Sensor module



Service hybrids
(readout, power)

Roman Pots

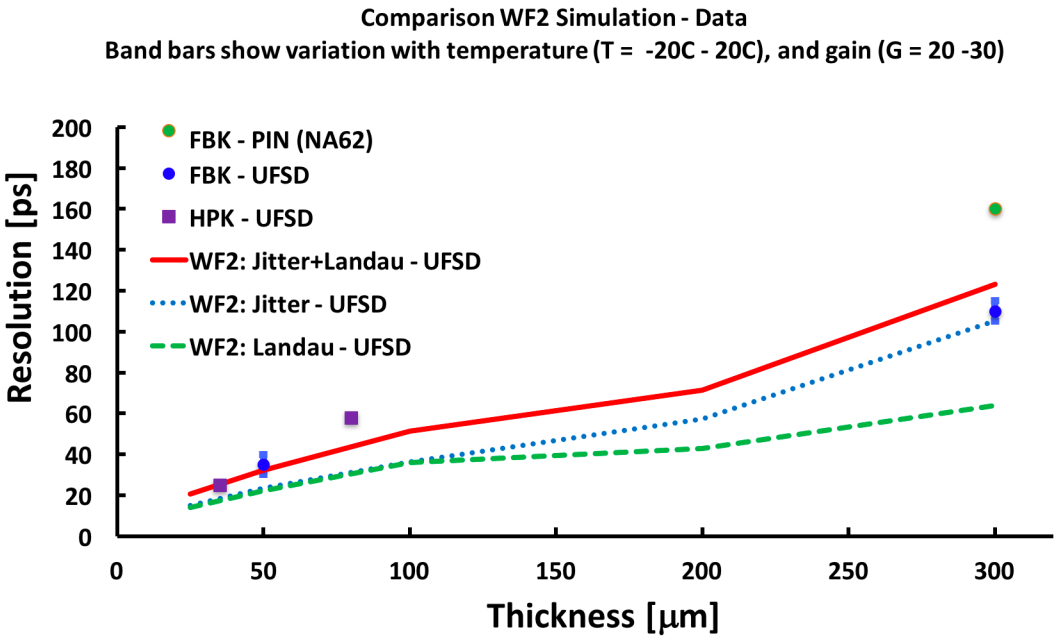


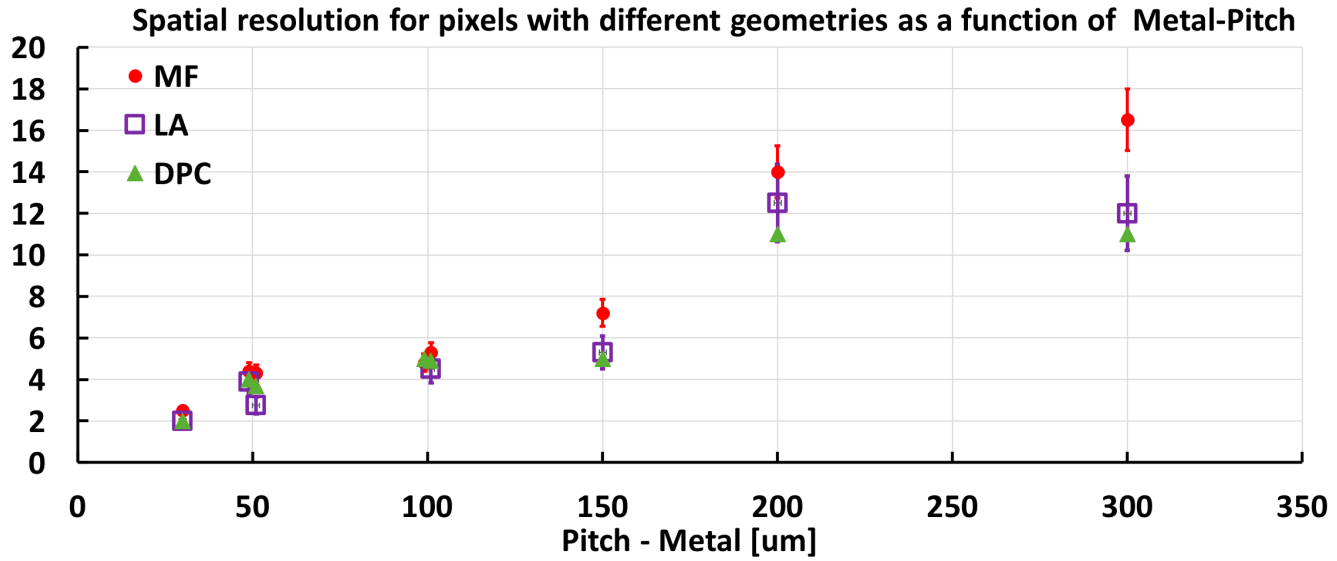


Requirements on timing and spatial resolutions and material budget are still being evaluated and are subject to change as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

eRD112: AC-LGAD Sensor R&D

Nicolo Cartiglia

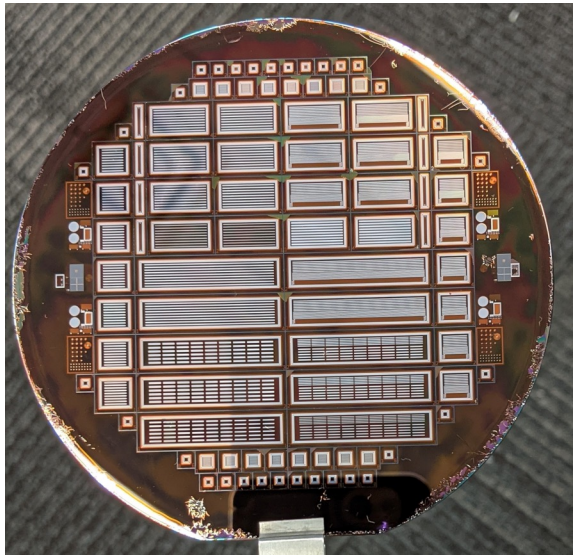




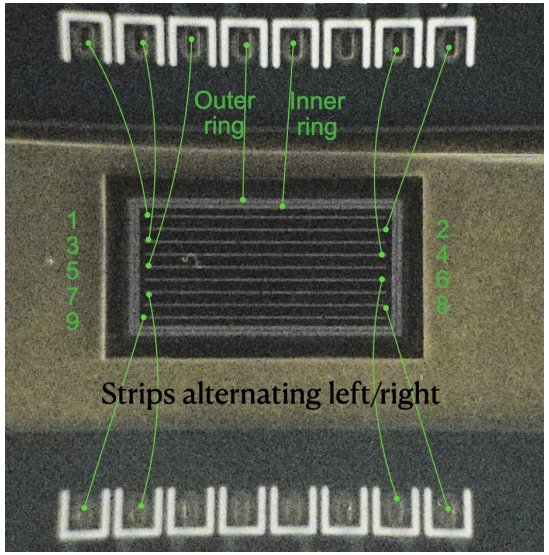
- **R&D Goals**
  - 15-20 ps timing resolution, O(3-50μm) position resolution where needed
  - Minimal readout channel density (long strip, rectangular pixel) for reduced power, material and cost
- **Plan**
  - Produce and test sensors with thinner active volume to achieve the desired timing resolution
  - Optimize implantation parameters and AC-pad segmentation through simulation and real device studies
  - Engage commercial vendors to improve fabrication process and yield

eRD112: AC-LGAD Sensor R&D

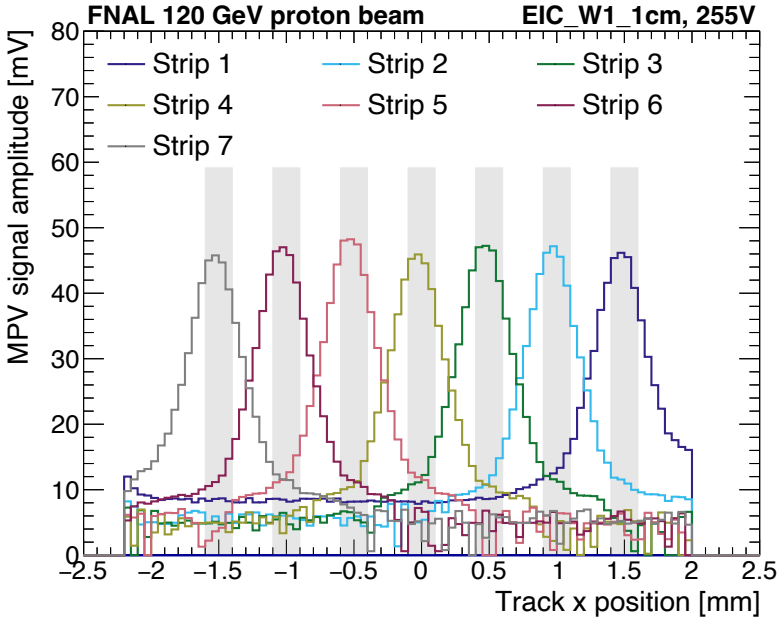
- **FY22**:
  - Production of thin (20 and 30 um) sensors for ToF application with time resolution ~20 ps by BNL IO.
  - Production of medium/large-area sensors with different doping concentration, pitch, and gap sizes between electrodes to optimize performance by BNL IO and HPK.
- **FY23 Q3**: Design and submission for fabrication of advanced sensor prototypes with <20 ps time resolution and space resolution that matches RPs, ToF, and Tracker requirements. This will be baseline for CD2/3A.
- **FY24 Q2**: Sensor batch submission with optimized sensor layouts and performance, based on laboratory and test-beam results. This sensor design will be used as baseline for the CD3 review.
- **FY25**: Module-size sensor fabrication with target time and space performance.



Strip AC-LGAD Sensor Wafer for EIC by BNL

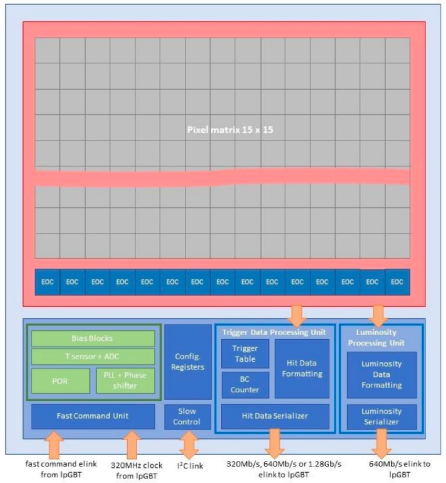


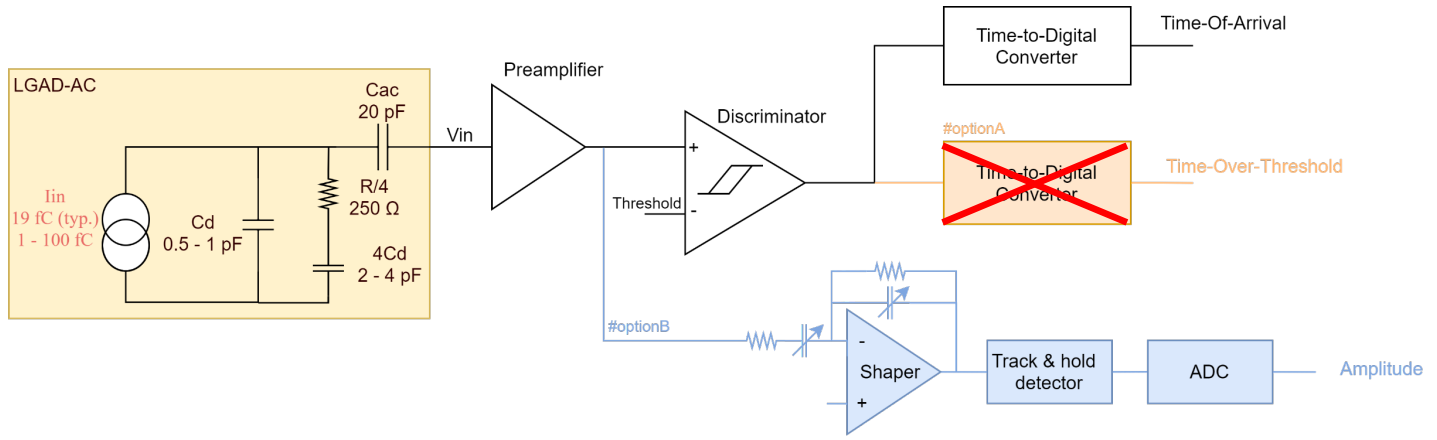
500 um*1cm strip AC-LGAD sensor mounted on test board



Signal amplitude vs x position at 2022 Fermilab test beam

eRD112: Frontend ASIC R&D





- **R&D Goal**
  - 15-20 ps jitter with minimal (1-2 mW/ch) power consumption, match AC LGAD sensors for EIC
- **Strategy**
  - Continue the ASIC prototyping effort for RPs by IJCLAB/Omega (1st submission in FY22 funded externally)
  - Utilize the design from ATLAS and CMS, and investigate common design for RP/B0 and ToF
- **Milestones**
  - **FY22 (funded externally):**
    - A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC LGAD with ~500 um pitch and ~30 ps time resolution.
    - **Deliverable (Sept. 2022)**: A prototype ASIC design to readout AC LGADs using signal sharing across neighboring electrodes and has 30 ps time resolution with low power consumption.
  - **FY23 Q1**: 2nd prototype design and submission with better performance and extended features. Baseline for CD2 review.
  - **FY24 Q2**: 3rd ASIC submission, aiming to match ToF timing requirements. Baseline for the CD3 review.
  - **FY25**: Full-scale ASIC submission.

BNL Proposal on Sensor R&D in FY23

Deliverables:

- 1 batch of AC-LGADs with optimized geometrical layouts, active substrate thickness and doping concentrations
- half a batch of large area sensors to test yield efficiency
- Several EICROC + sensor assemblies
- In-house performance characterization of BNL's produced batches of sensors and EICROC + sensor assemblies.

Resource Request:

- 75k$: fabrication of 1.5 batches of sensors: 50k$ for a batch of 10 wafers and 25k$ for half a batch of 5 wafers.
- 20k$: sensor + test board assembly (incl. wire/bump-bonding).
- 4k$: cost of 2 travels to FNAL for test-beams (2k$ each).
- In-kind: sensor dicing and testing before distribution as well as sensor testing by a technician and a postdoc

UIC Proposal on Sensor/ASIC R&D in FY23

Deliverables:

- Lab/beam testing results for the new AC-LGAD sensors from BNL and HPK
- Lab/beam testing results for EICROC0 and FCFDv0
- Interposers that connect strip/pixel sensors with pixelated frontend ASIC with different pitches
- Beam test setup at FTBF using prototype AC-LGAD sensors and frontend ASICs for EIC
- Test boards with AC-LGAD sensors and frontend ASICs mounted and wire-/bump-bonded

Resource Request:

- 45k$: research specialist on lab/beam test of sensors and ASICs
- 15k$: sensor + test board assembly (incl. wire/bump-bonding)
- 5k$: M&S for test beam setup
- 5k$: travels to FNAL for test-beams (1k$ each)
- 30k$: interposer fabrication and bump-bonding
- 15k$: interposer design and testing by electric engineer
- In-kind: coordination and detector design by faculty, lab/beam test by graduate, telescope assembly by UG student

Workforce at UIC on EPIC:
2 Faculties
1 electrical engineer
1 electrical technician
1 postdoc
2 PhD students
1 undergrad student

SCIPP Proposal on Sensor R&D in FY23

Deliverables:

- Lab/beam testing results for the new AC-LGAD sensors from BNL and HPK
- TCAD simulation for sensor optimization

Resource Request for sensor R&D:

- 9k$: oversight and coordination by project scientist
- 16.5k $: TCAD simulation and sensor design by electronic design specialist
- 11.8k$: prototype assembly by electro-mechanical engineer
- 3.7k$: test boards

Workforce at SCIPP on EPIC:
3 Faculty (20% FTE)
1 junior faculty (30% FTE),
1 staff scientist (30% FTE),
3 technical staff (20% FTE),
2 postdocs (40% FTE),
3 PhD students
8 undergrad students

LANL Proposal on Sensor R&D in FY23

Proposed work:

- Characterize the analog output of radiated samples before and after the irradiation tests
- Study the digital signal amplitudes with the wire-bound AC-LGAD carrier boards from BNL (LANL will provide the assembled carrier boards) to use the 90Sr source bench tests.
- Compare the pixel hit occupancy before and after the irradiation tests with different doses to check the noise rate dependence on the radiation doses and possible radiation damage effects.

Resource Request for sensor R&D:

Resource	FTE (%)	Budget (k$)
Staff Scientist	2.5	10
Graduate Student	5	5
Materials and Supplies	-	5
Total	-	**20**

ORNL Proposal on Sensor R&D in FY23

Proposed work:

- Contribute to the planned sensor test beam campaigns
- Perform ”slow” simulation for the AC-LGAD sensors using appropriate silicon sensor simulation tools. Develop sensor digitization module to be included into the EPIC simulation software

Resource Request for sensor R&D:

Resource	Task	FTE (%)	Budget (k$)
Staff Scientist	Sensor simulation	20	0 (in-kind)
Travel	beam test	-	6
Total	-	-	**6**

Rice Proposal on Sensor R&D in FY23

Proposed work:

- La/beam tests of pixel sensors with different pitch and thickness, in collaboration with other groups

Resource Request for sensor R&D:

Resource	Task	FTE (%)	Budget (k$)
Postdoc	endcap TOF layout design	10	0 (in-kind)
Postdoc	pixel sensor testing (lab/beam)	40	40
Travel	beam test	-	6
Total	-	-	**46**

IJCLab/OMEGA/CEA-Irfu on EICOC in FY23

Deliverables:

- Design/submission EICROC1 with 8x4 (or 16x4) pads including lower power ADC and adapted to 100 MHz clock
- Performance characterization of EICROC0: stand-alone, with a sensor connected, with realistic energy deposits

Resource Request:

Institution	Resource	Task	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	WP2	60	0 (in-kind)
	Senior scientist	WP2	35	0 (in-kind)
	Senior scientist	WP1&2	20	0 (in-kind)
	Research engineer	WP1&2	30	0 (in-kind)
	Research engineer	WP2	25	0 (in-kind)
	PhD student	WP2	50	0 (in-kind)
	EICROC1 [8 (or 16) $\times$ 4 channels] submission (MPW)	-	-	65
	Fabrication of testboards and associated components	-	-	10
OMEGA	Senior research engineer	WP1	25	0 (in-kind)
	Senior research engineer	WP1	20	0 (in-kind)
	Research engineer	WP1	15	0 (in-kind)
	Assistant engineer	WP1	20	0 (in-kind)
CEA/Irfu	Senior research engineer	WP1	30	0 (in-kind)
	Senior research engineer	WP1	10	0 (in-kind)
Total	-	-	-	**75**

Table 17: eRD109 budget request for FY23 on EICROC. All entries in thousands of dollars.

FNAL Proposal on FCFD in FY23

Deliverables:

- Characterization of FCFDv0 in beam
- Specifications for the FCFDv1, and selection of the sensors for demonstrator.
- Design, submission and initial testing of 10-channel FCFDv1.

Resource Request:

Resource	Task	FTE	Budget (k$)
Staff Scientists	oversight and coordination	5	0 (in-kind)
Postdoc	Sensor testing	15	0 (in-kind)
Engineers	FCFDv1 design	25	0 (in-kind)
Postdoc	FCFD+Sensor testing	25	0 (in-kind)
FCFDv1 Multi-Project Wafer (MPW)	-	-	25
FCFD test boards and components	-	-	15
Total	-	-	**40**

Table 18: eRD109 FNAL Budget request for FY23 on FCFD. All entries in thousands of dollars.

SCIPP Proposal on ASIC R&D in FY23

Proposed work:

- Guidance and characterization of frontend ASICs from 3rd party institutions

Resource Request:

- 12.4k$: service board design and layout by electronic design specialist
- 11.8k$: board assembly by electro-mechanical engineer
- 5.5k$: board loading and lab measurement by assistant specialist
- 3.3k$: M&S for ASIC service boards

Workforce at SCIPP on EPIC:
3 Faculty (20% FTE)
1 junior faculty (30% FTE),
1 staff scientist (30% FTE),
3 technical staff (20% FTE),
2 postdocs (40% FTE),
3 PhD students
8 undergrad students

ASICs from 3rd Party Institutions Studied by SCIPP

- FAST2, developed by INFN Torino: Longer shaping time ($\geq$ 800 ps) not optimized for thin sensors (200–500ps signal rise). Power draw: 1 mW/channel for analog, 1 mW/channel for discriminator/TDC. New design (FAST3) ready soon.
- ASROC: Uses fast SiGeprocess for front end. Promising design but prototype not yet in hand. Front-end power draw good ($\leq$1 mW) but not clear it can be mated to low-power CMOS for back-end. Future funding sources unclear
- HP-SoC: Full, highly flexible "system on chip" (SoC). Both front and back end carefully optimized for timing precision. Integrated 65 nm process promises low power for full readout chain. Ongoing project with DOE recognition and support. Prospective performance characteristic on following page. Power draw: 1.6 mW/chfor analog, 1 mW/ch for digitizer and 1 mW/ch for digital (current goal, still under development).

LGAD characteristic	50 μm	20 μm
Rise time (10-90%) [ps]	455	182
Input charge [fC]	11	4.6
ASIC characteristic	**50 μm**	**20 μm**
Jitter [ps]	10	5
S/N	>50	>40
Voltage signal [mV]	70	70
Noise RMS [mV]	1.4	1.8
Internal sensor gain	20	20

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

Table 7: Characteristics of ASICs followed by SCIPP.

BNL/ORNL/Rice on Frontend Electronics in FY23

Deliverables:

- Preliminary prototype of an integrated readout board that supports the first iterations of the EICROC.
- Prototype of flexible Kapton PCBs for service hybrid with integrated data aggregation and power distribution.
- Prototype of frontend service hybrid including readout and power boards to minimize material budget and space.

Resource Request:

Inst.	Resource	FTE (%)	Budget (k$)
	Readout and Timing Distribution R&D		
BNL	Research Associate	20	38
BNL	2 Staff Scientists	2x20	0 (in-kind)
BNL	Xilinx Dev. Kit	-	4
BNL	Timing Chips + Boards	-	15
	Barrel Low-Mass Service Hybrid R&D		
ORNL	Electrical Engineer	10	32
ORNL	Staff Scientist	10	0 (in-kind)
ORNL	Materials and Supplies	-	8
ORNL	Xilinx Dev. Kit	-	4
	Endcap Service Hybrid R&D		
Rice	Faculty	10	0 (in-kind)
Rice	Electrical Engineer	15	18
Total			**119**

AS/NCKU/Purdue on Light-Weight Structure in FY23

Deliverables:

- Barrel structure design and prototype with deflection within a few hundred μm and material budget less than 1%.
- Endcap structure design and prototype with similar requirements on barrel

Resource Request:

Institution	Resource	FTE (%)	Budget (k$)
Purdue	Faculty	20	0 (in-kind)
Purdue	Mechanical engineer	10	15.0
Purdue	Material and Supplies	-	5.0
NCKU/AS	2 Faculties	2×20	0 (in-kind)
NCKU/AS	Senior scientist	20	0 (in-kind)
NCKU/AS	2 Engineers	2×10	0 (in-kind)
NCKU/AS	Graduate Student	20	0 (in-kind)
NCKU/AS	Undergraduate Student	100	0 (in-kind)
NCKU/AS	Production cost	-	5.0
NCKU/AS	Materials and Supplies	-	10.0
Total	-	-	**35.0**

Workforce on EPIC:
3 Faculty (3x20% FTE)
1 senior scientist (20% FTE)
3 engineers (3x10% FTE)
1 PhD student
1 undergrad student

FY22 Deliverables

- High-level strawman layout design and requirements for sub-systems using AC LGADs.
- Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes to optimize performance by BNL Instrumentation and HPK.
- Start production of sensors of small thickness (20, and 30 microns) for ToF applications with time resolution 20 ps by BNL Instrumentation.
- A first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 micron pitch and 20 ps time resolution.

FY23-26 Deliverables and Milestones

FY23

- Sensor prototype with 30 ps time and space resolution match RPs and Tracker;
  Sensor prototype with 20 ps time resolution for ToF
- 1st sensor + ASIC demonstrator for EIC applications and testing with particle beam.
- 2nd ASIC prototype submission with better performance and extended features.
- Irradiation campaign for sensor and ASIC prototypes.
- Development of cooling strategy and mechanical requirements.

FY24

- Optimized AC-LGAD sensor layouts and performance.
- 3rd ASIC submission, aiming to match ToF timing requirements.
- Definition of cooling strategy and mechanical design.
- Design of flexes, interconnects and off-detector electronics.

Sensor **ASIC** **Prototype Module** **Services**

FY23-26 Deliverables and Milestones

FY25

- Sensor fabrication with expected module-size and target time and space performance.
- 1st full-scale ASIC submission.
- 2nd sensor+ASIC demonstrator with second generation parts, testing with beam.
- Irradiation campaign for sensor and ASIC prototypes.
- Cooling strategy demonstration.
- Prototyping of flexes, interconnects and off-detector electronics.

FY26

- 2nd (and last) full-scale ASIC submission with optimized design.
- 3rd demonstrator of module with optimized sensor, ASICs, prototype interconnect and cooling

Sensor **ASIC** **Prototype Module** **Services**