Sensor R&D: Status and Plan

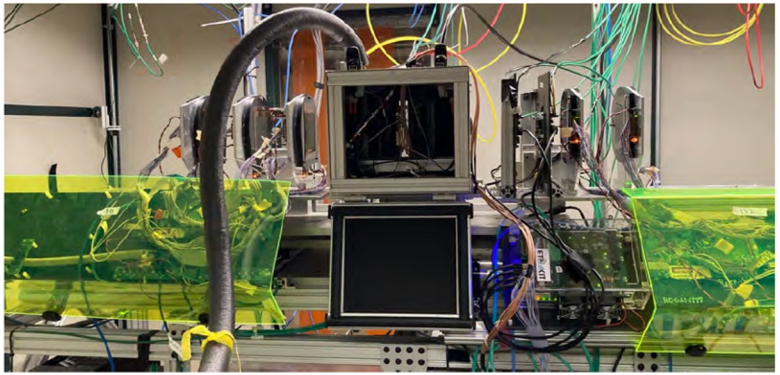


Figure 7: Picture (top) and diagram (bottom) of the FTBF silicon telescope and reference instruments used to characterize AC-LGAD performance. The telescope comprises five pairs of orthogonal strip layers and two pairs of pixel layers, for a total of up to 14 hits per track.

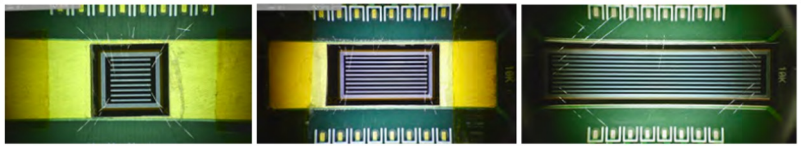


Figure 8: Three AC-LGAD strip sensors wire-bonded on Fermilab test board and tested at FTBF: BNL 5-200 (left), BNL 10-200 (middle) and BNL 25-200 (right). See text for details.

	Time resolution	Spatial resolution				
		Exactly one strip		Two strip		Effective
Name	High gain	Resolution	Eff.	Resolution	Eff.	Resolution
Unit	ps	μm	-	μm	-	μm
BNL 5–200	30 ± 1	61 ± 1	35%	12 ± 1	65%	37 ± 1
BNL 10–100	35 ± 1	69 ± 1	23%	19 ± 1	77%	37 ± 1
BNL 10–200	32 ± 1	82 ± 1	43%	18 ± 1	57%	55 ± 1
BNL 10–300	36 ± 1	83 ± 1	51%	16 ± 1	49%	60 ± 1
BNL 25–200	51 ± 1	128 ± 1	82%	31 ± 1	18%	117 ± 1

https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23

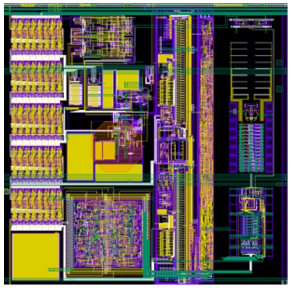
- Status: achieved ~30 ps timing and ~25 micron spatial resolutions from 500 micron pitch pixel sensors, and ~35 ps timing and ~35 micron spatial resolutions from 1 cm long, 500 micron pitch strip sensors
- Plan: move to thinner active Si thickness to improve timing resolution, study different doping concentration, pitch and electrode width to further optimize performance.

Frontend ASIC R&D: Status and Plan

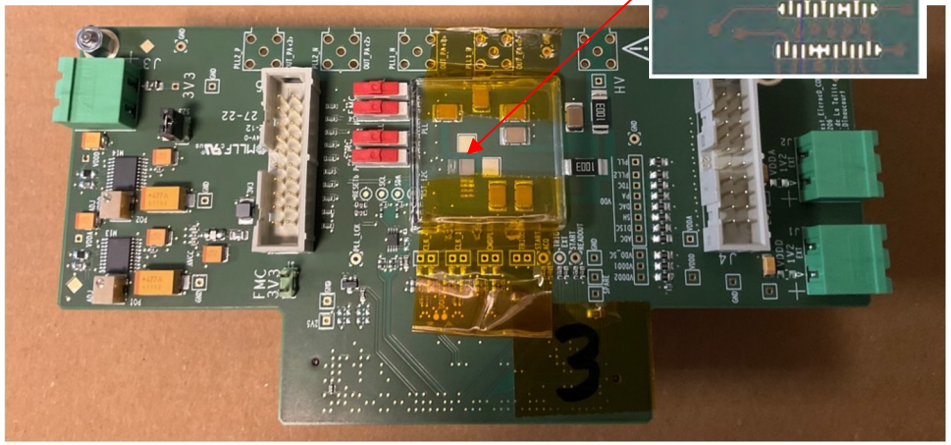
EICROC0: first ASIC prototype that is compatible with EIC Roman Pot requirements and can read out an AC-LGAD with 500 micron pitch and 20 ps time resolution.

submitted in 3/2022, received in 7/2022 by OMEGA/CEA-Irfu/AGH/IJCLab

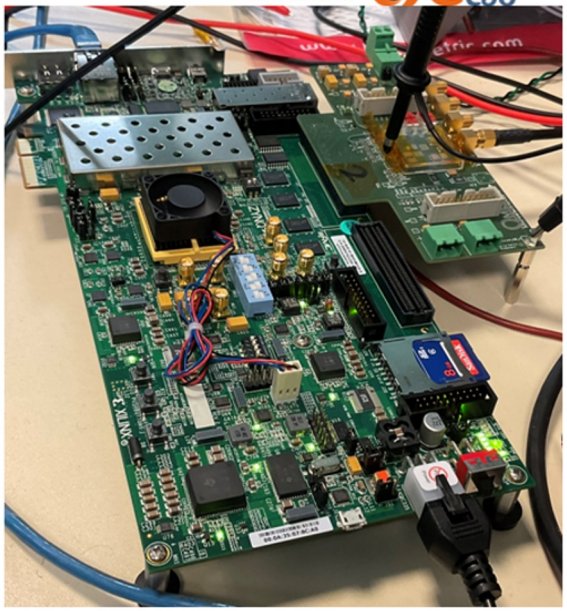
4 x 4 channels with 500x500 um2 pitch
Preamp, discri. taken from ATLAS ALTIROC
I2C slow control taken from CMS HGCROC
TDC (TOA) adapted by CEA-Saclay/Irfu
ADC (40 MHz) adapted to 8bits by AGH Krakow
Digital readout: FIFO depth8 (200 ns)



EICROC0, *1 channel implantation*



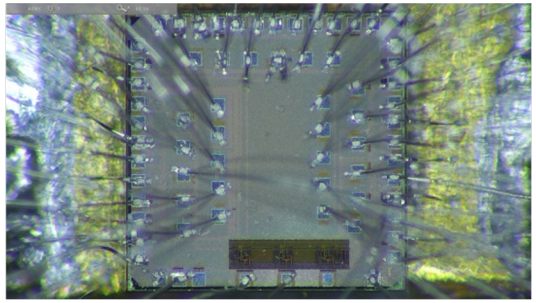
EICROC0 Test bench at IJCLab

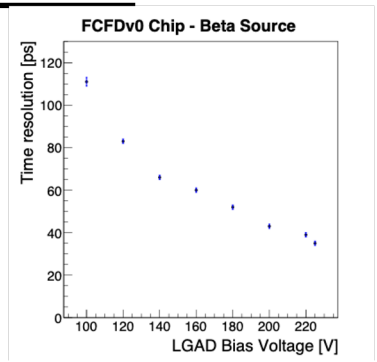


Frontend ASIC R&D: Status and Plan

FCFDv0 (Fermilab CFD v0):

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel when a CFD is paired with a TDC, one time measurement gives the final answer.
- Charge injection and beta source tests consistent with expectation. Tests with beam are planned



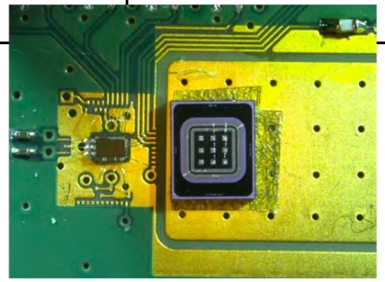


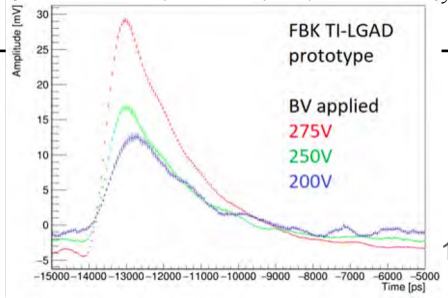
ASIC effort by UC Santa Cruz:

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASRO C	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations, final Layout, Board design

Plan:

- Continue the ASIC prototyping efforts utilizing the design and experience in ASICs for fast-timing detectors from ATLAS and CMS, and investigate common ASIC design and development for RP/B0 and ToF



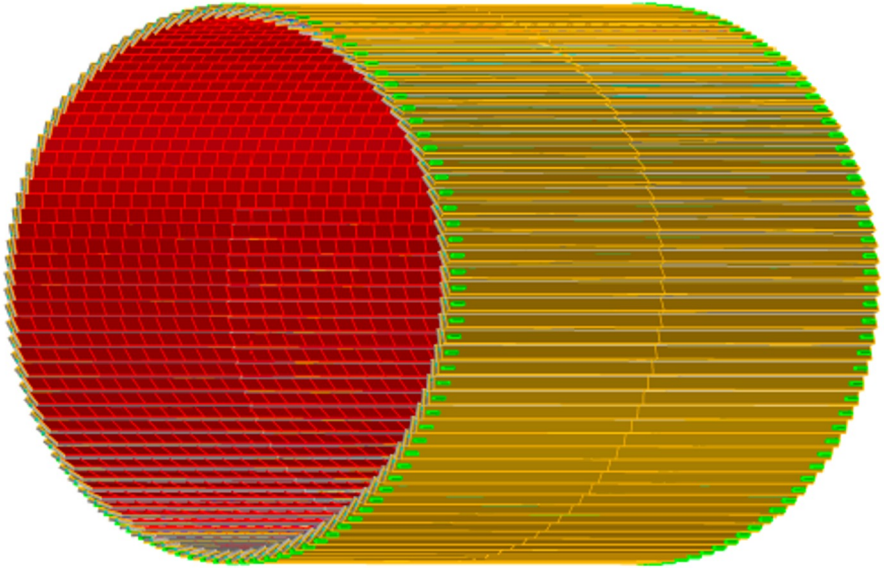


TOF-PID Report: Integration

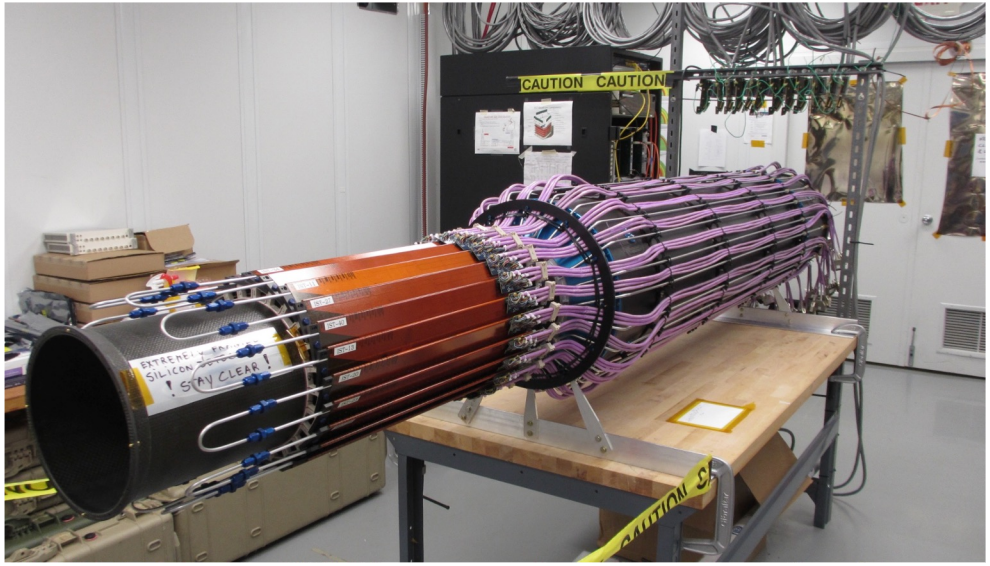
ePIC GD/I meeting
November 7, 2022

Barrel TOF Layout and Integration

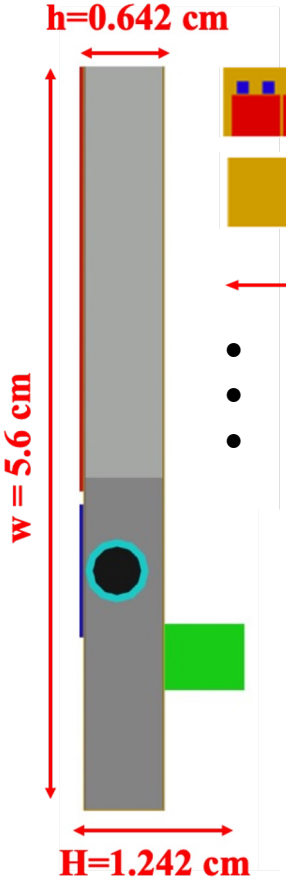
Barrel TOF CAD Drawing

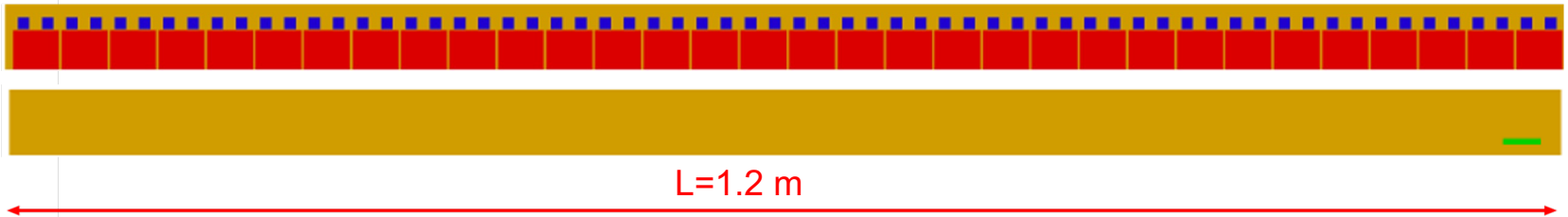


STAR Intermediate Silicon Tracker

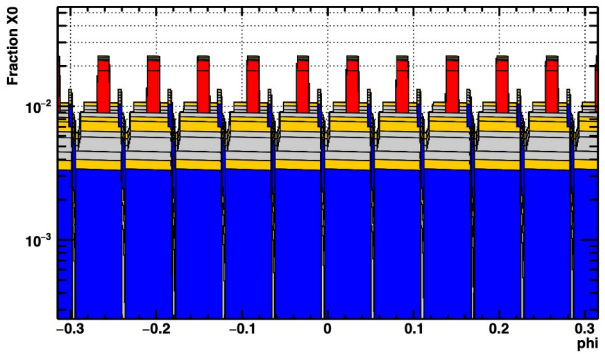


Barrel TOF Layout and Integration





- **32 AC-LGAD sensors**, each 3.2*4 cm^2 read out by **2 ASICs**
- **Low mass flexible Kapton PCB** distributes power and I/O signals from a low mass connector(s) at the edge
- **Liquid coolant** in **Al cooling tube** takes away heat from the ASICs



288 modules, each powered and read out by 1 service board with

1 LV+HV cable, 1 fiber to DAQ, 1 liquid cooling line

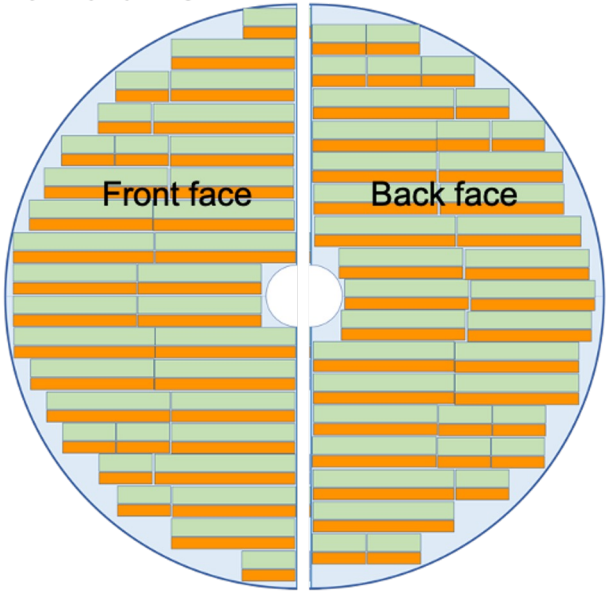
Total weight: ~70 kG

Total power consumption: ~4 kW (2.4kW for ASIC, 1.0kW for DC-DC, 0.6kW for sensors+cables+RB)

https://indico.bnl.gov/event/17336/

Endcap TOF Layout and Integration

Forward TOF: Strawman layout

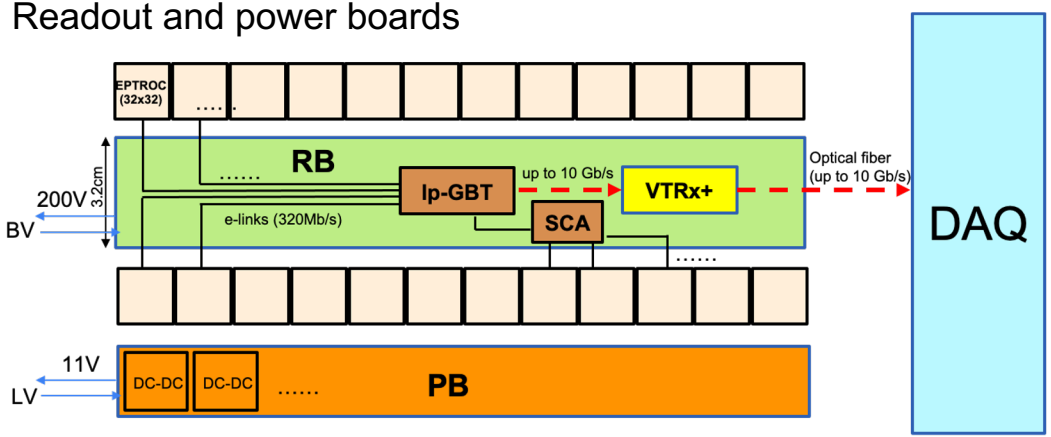


Sensors+ASICs: matrix of 32x32 pixels,

"Clam shells" or DEEs:

- Convenient for installation/maintenance
- Each is patched by TOF modules (one or more types) on both faces

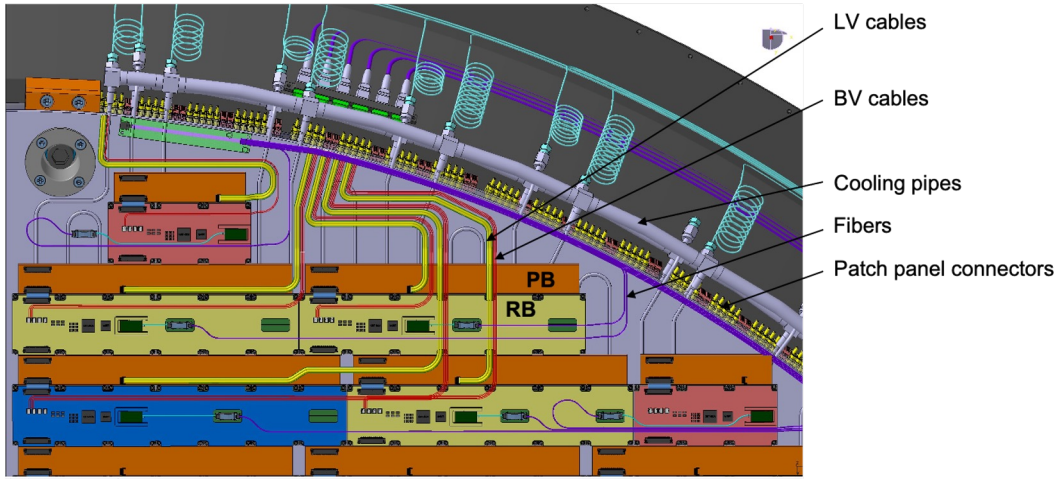
Readout and power boards



More details: https://indico.bnl.gov/event/17336/

Endcap TOF layout and integration

Service routing, similar to the CMS design



<10cm in z thickness

Services (baseline)	Forward	Backward
Sensors/ASICs	8704	4608
LV cables	424	248
HV cables	424	248
Fibers	212	124

Power Consumption	Forward	Backward
500x500 micron^2 (baseline)	13kW	6kW
800x800 micron^2 (possible alternative)	6kW	3kW

Planned/proposed R&Ds to optimize baseline design to minimize power consumption and develop effective cooling scheme

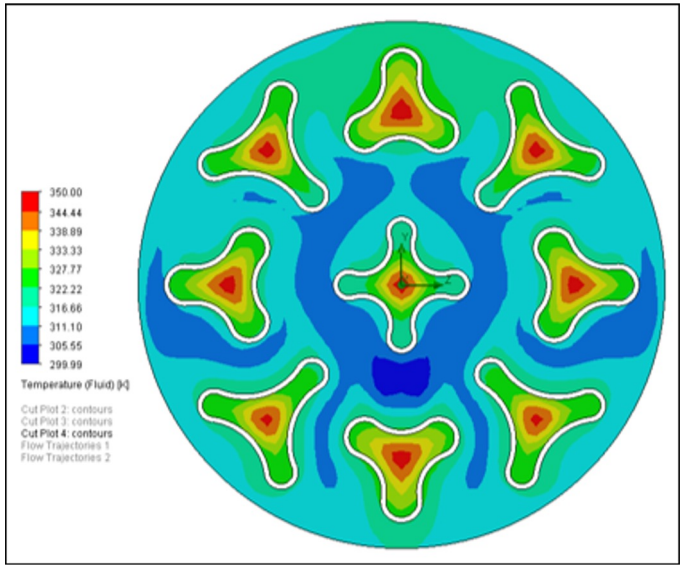
More details: https://indico.bnl.gov/event/17336/

Support and Cooling Development

Need realistic engineering design for AC-LGAD systems for CD2/3a

- Minimal material budget, appropriate cooling system for stable operation, heat load impact on nearby sub-detectors
- Requested R&D resources in eRD112 and PED request

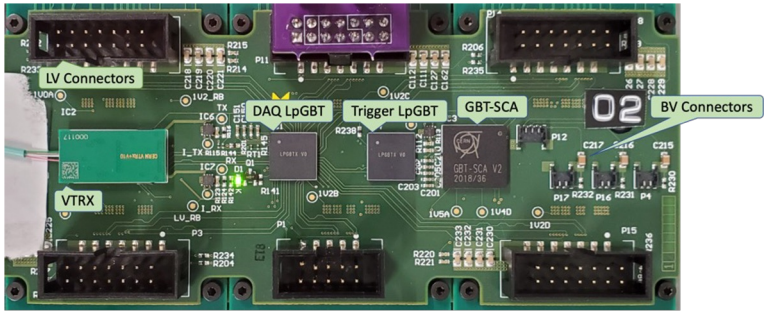
- Purdue/NCKU: lightweight support and Barrel mechanical design
  - Studies based on CF composites/PEEK
  - Extensive experience with lightweight composite tracking detector supports from CMS tracking upgrade projects
- ORNL: TOF Endcap mechanical design
  - Integrated water cooling system
  - Wealth of experience from similar projects
- Engineers have experience with FEA, Solidworks and ANSYS Comp. Fluid. Dyn.



On-detector Electronics Development

R&D proposal (eRD109) includes collaborative AC-LGAD readout electronics work from BNL, Rice, ORNL. Further PED request through DAQ group is anticipated

- BNL: Readout board reference prototype
  - Precision clock distribution
  - EICROC readout studies
- Rice: Readout board implementation for TOF endcap, power board
  - Based on CMS-ETL service hybrids
- ORNL: Readout R&D for barrel implementation
  - Targeting kapton flex design for minimal material budget
  - Integration into barrel mechanics



Experienced electrical engineers

Summary and Outlook

- Geometry implementation in EPIC software simulation stack done
- (Re-)starting PID + tracking performance impact analyses
  - Beam background + noise impacts to be studied

- Work towards engineering design towards CD2/3a underway with funding requests submitted to project: eRD112, eRD109, PED
  - R&D on sensor, ASIC, sensor/ASIC integration, lightweight support and electronics
  - PED on mechanical support and cooling (and electronics in the near future)
  - Involving multiple institutes with wide range of experience

https://wiki.bnl.gov/EPIC/index.php?title=TOFPID