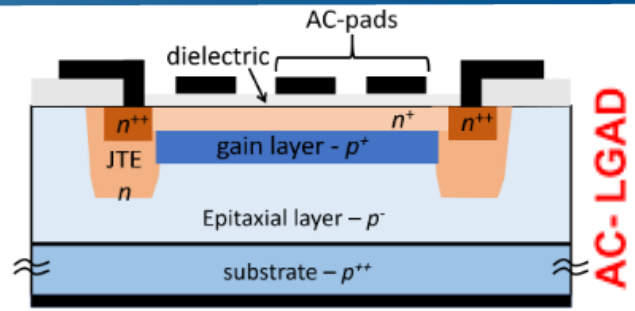
Front-End ASICs to read-out AC-LGAD sensors: status and plan

Dominique Marchand (IJCLab, Orsay, France)

on behalf of teams involved in ASIC development and characterization for ePIC detectors

OUTLINE

Objective: **ASIC design and characterization**
dedicated to the read-out of **AC-LGAD**
(Low-Gain Avalanche Diode) silicon sensors



4D reconstruction (timing & position)

Central **T**racking & **T**iming **L**ayer (Barrel TOF): AC-LGAD **strips** (reduced number of # to lower power)
(Far)-Forward detectors (TOF & Roman Pots): **pixelated** AC-LGAD (0.5 x 0.5 mm^2)

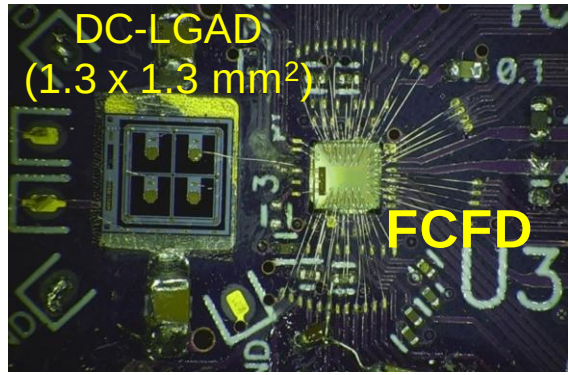
- **FCFD (FermiLab) ⇨ AC-LGAD strips**
- **Univ. of California Santa Cruz / SCIPP: HPSoC, ASROC, FAST**
- **EICROC (French collaboration + BNL) ⇨ pixelated AC-LGAD**
- **Summary**

FCFD: Forward Constant Fraction Discriminator

From Artur Apresyan (FermiLab)

Goals:

- Develop a robust fast-timing measurement technique for fast detector
- 30 ps time resolution or better
- easy to use & stable: no corrections, no calibration or threshold adjustement
- very low dead time after a hit (< 25 ns)



Methodology:

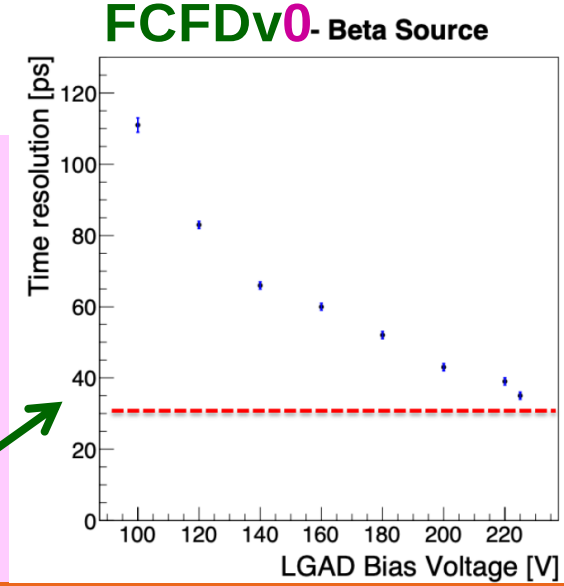
✸« A simulation model of front-end electronics for high precision timing measurements with LGAD », C. Peňa *et al.,* NIM A 940 (2019) 119.

⇨ CFD outperforms Leading edge Discriminators for low amplitude signal (**preferred** for AC-LGAD charge sharing capability)

FCFDv0 (TSMC 65 nm CMOS technology)

1 single channel, **only analog blocks** to test CFD approach

- Chip performance characterization with internal charge injection circuit
  Jitter: **~30 ps** (5 fC); < 10 ps (30 fC)
- + DC-LGAD (CMS-size pixel:1.3 x 1.3 mm²) 1 # wire-bonded
  IR Laser, Beta source ⇨ confirmation of expected time resolution: **~30 ps**
- *measurements at test beam facility will follow*



FCFD: FY23 plan

From Artur Apresyan

✸FCFDv1 (TSMC 65 nm CMOS technology): 2nd half 2023, characterization ⇨2nd half '24
10 channels, analog blocks + ADC (charge measurement)

- optimized for EIC AC-LGAD strips (500 μm pitch, 1 cm length)
- development of associated PCB test board
- + AC-LGAD sensor < BNL
  IR Laser, Beta source, Test beam

✸FCFDv2 (TSMC 65 nm CMOS technology): 2nd half '24, characterization ⇨2025
10 channels, + digital readout

- development of associated PCB test board
- + AC-LGAD sensor < BNL
  IR Laser, Beta source, Test beam

FCFD presentations at eRD112 meetings:
https://indico.bnl.gov/event/17999/ (01/04/23)
https://indico.bnl.gov/event/17084/ (09/14/22)

UCSC/SCIPP effort: 3rd party ASIC characterization

From Jennifer Ott et al.(UCSC/SCIPP)

Objective: closely collaborating with 3rd party **institutions** and **companies** to **guide** ASIC developments **targetting EIC requirements** developing **PCB test boards** and performing **thorough characterization** (calibration ; laser, 90Sr source with LGAD wire-bonded) allowing for ASIC performance comparison

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

FY23 plan:

- **HPSoC** *(High Pitch digitizer System on Chip):* awaited new optimized prototype (EIC)
- **ASROC:** production and characterization of the 1st prototype
- **FAST3** characterization

SCIPP presentations at eRD112 meetings: https://indico.bnl.gov/event/17999/ (01/04/23)
https://indico.bnl.gov/event/16767/ (09/06/22)

EICROC effort

2021-2022 funding

Objective: Development of an **ASIC prototype**
EICROC0
able to readout a new generation of silicon sensors:
AC-LGAD
(Low-Gain Avalanche Diode)
for the **Electron Ion Collider** (EIC) **Roman Pots**

Organization for Micro-Electronics desiGn and Applications, Ecole Polytechnique, Palaiseau

CEA Saclay/Irfu/
Département d'Electronique des Détecteurs et d'Informatique pour la Physique (DEDIP)

eRD112 AC-LGAD: weekly meetings

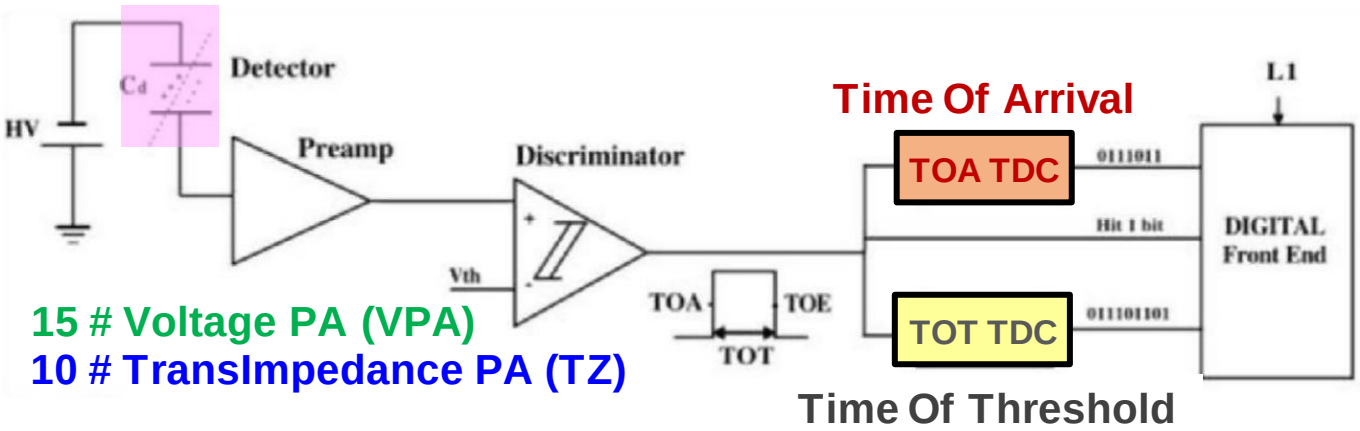
ATLAS/HGTD (High Granularity Timing Detector): ALTIROC ASIC

ALTIROC: **A**TLAS **L**GAD **T**iming **I**ntegrated **R**ead **O**ut **C**hip [TSMC **CMOS 130 nm** technology]

designed and characterized by OMEGA and IJCLab dedicated to pixelated DC-LGAD (1.3 x 1.3 mm²) read-out [**ALTIROC3** full size: 225 channels)]

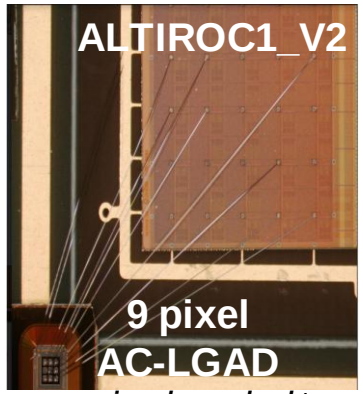
ALTIROC prototypes: a good start to evaluate AC-LGAD response
⇨ guide EICROC0 design

Schematics of ALTIROC1_v2 for 1 channel (1 pixel)



15 # Voltage PA (VPA)
10 # TransImpedance PA (TZ)

ALTIROC1: 25 channels



wire-bonded to ALTIROC1 by BNL

Average jitter: **~ 15 - 20 ps** (in agreement with ALTIROC previous measurements)
Lowest detectable charge: **2.5 fC ⇨ very encouraging to fulfill EIC requirements**

G. D'Amen *et al.*, "Signal formation and sharing in AC-LGADs using the **ALTIROC0** front-end chip", JINST **17** P11028, Nov 22

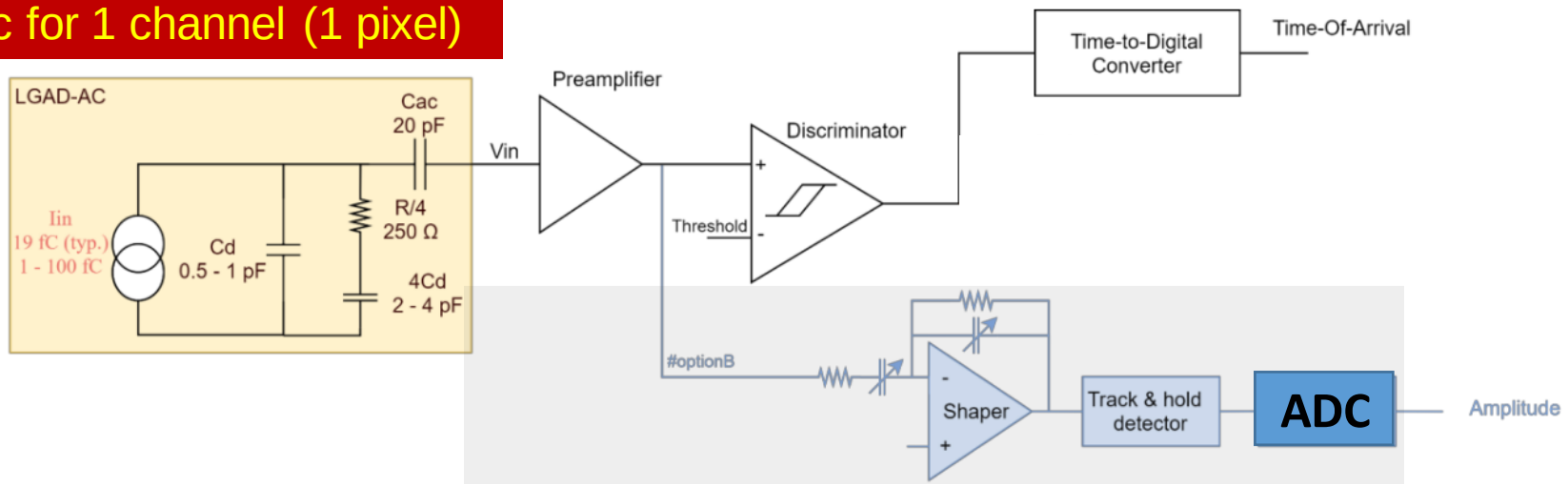
EICROC0 design: 16 channels (4x4)

Requirements:
- pixel size **0.5 x 0.5 mm²** *(HGTD 1.3x1.3 mm²)*
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**

Charge sharing studies (simulation + β source)

EICROC0 design:
- TZ Preamplifiers from ALTIROC
- TDC from HGCROC (CMS, CEA/Irfu/DEDIP)
- 8 bit ADC for time-walk correction (AGH Krakow, adapted from HGCROC)

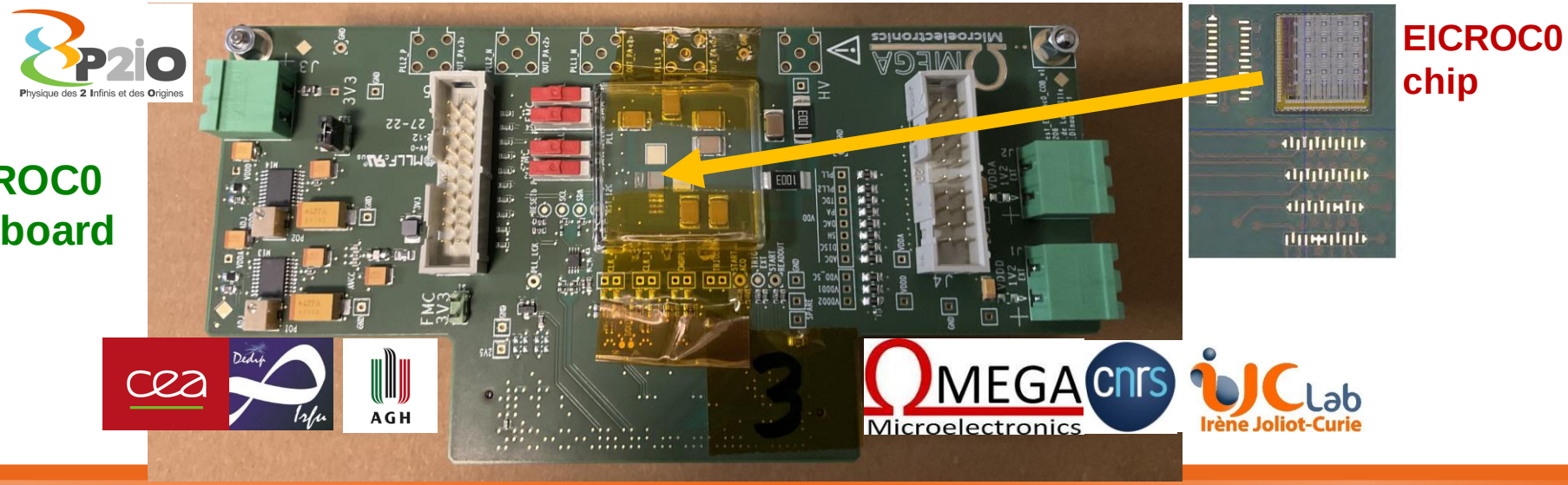
Schematic for 1 channel (1 pixel)



Compared to ALTIROC, ToT TDC (non-linear behavior as a function of deposited charge) replaced by an ADC

EICROC0: EIC 4x4 AC-LGAD readout test chip

- Submitted through a Multi Project Wafer (130 nm CMOS technology) in March 22
  EICROC0 chips delivered mid July 22
- **Test board** (PCB) designed by OMEGA, 10 pieces **delivered end of July 22**
  - test board cabling by IJCLab
- **Wire-bonding of EICROC0 to test boards** by BNL collaborators
- Delivery of 3 test boards to IJCLab in **Oct. 22**
- **Interface board** (Xilinx ZC 706): firmware / software developments (IJCLab)



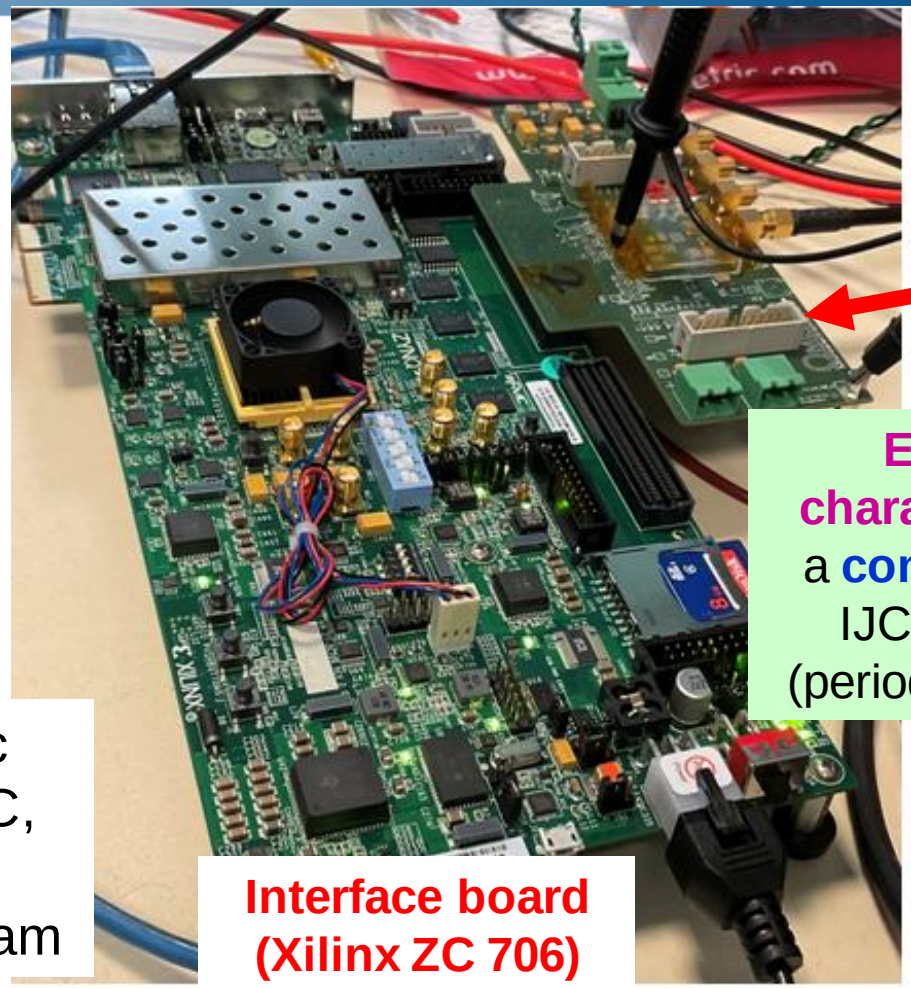
EICROC0 Test Bench at IJCLab

Test bench finalization under progress

- ✓ I²C communication (firmware dev.)
- ✓ Data stream written/read
- ✸ decoding under investigation
- ✓ EICROC0 DC levels
- ✓ Discri. threshold exploration
- ✸ EICROC0 internal injection circuit under investigation

Goal:

EICROC0 channel by channel electronic response characterization (PA, TDC, ADC, jitter evaluation, cross talk)
+ AC-LGAD: 90Sr source, IR laser, test beam



EICROC0 Test board

Interface board (Xilinx ZC 706)

EICROC0 characterization: a **common effort** IJCLab & BNL (periodic meetings)

FY23 & beyond plan: 2 step iteration to provide a 32x32 chip fulfilling ePIC detector requirements

Summary

➢ AC-LGAD: new generation of LGAD sensors, so far never implemented in HEP exp.
➢ Designing AC-LGAD dedicated ASICs represents a real challenge to fully exploit their timing and spatial resolution capabilities as well to fulfill ePIC detector requirements (low power, sensitivity to low charge, low noise, small pixel size or strips, …)

⇨Within a constructive emulation among the collaboration, for the next 2-3 years, this calls for multi developments relying on different technologies and the setup of characterization procedures to evaluate best candidates associated with each detector specificities

- FCFD (FermiLab)
- EICROC (French collaboration + BNL)
- SCIPP: FAST, HPSoC, ASROC readout & characterization

⇨ Sharing between involved teams (including sensor design & readout/DAQ) and among concerned detector working groups / eRD consortium **is crucial**

Back-Up

EICROC0: 1 pad (500 x 500 µm²) overview

- High speed TZ PA and discriminator (from ALTIROC)
- I²C slow control (from CMS HGCROC)
- 8 bits 40 MHz ADC (adapted from HGCROC 10 bits ADC M. Idzik *et al.*, AGH Krakow)
- Digital readout FIFO (depth 8, 200 ns)
- 10 bits **TDC** (TOA) designed by **CEA Irfu/DEDIP**:
  HGCROC TDC (1 mm x 120 µm):
  - spatially adapted to fit in a pixel of 0.5 x 0.5 mm²
  - optimization in terms of dynamic range and resolution (10 ps rms) as well as power consumption
  - common block for calibration of all TDC channels

✸ <u>5 slow control bytes/pixel:</u>
- 6 bits local threshold
- 6 bits ADC pedestal
- 16 TDC calibration bits
- Various on/off and probes

EICROC0 layout (1 pad = 1 channel)