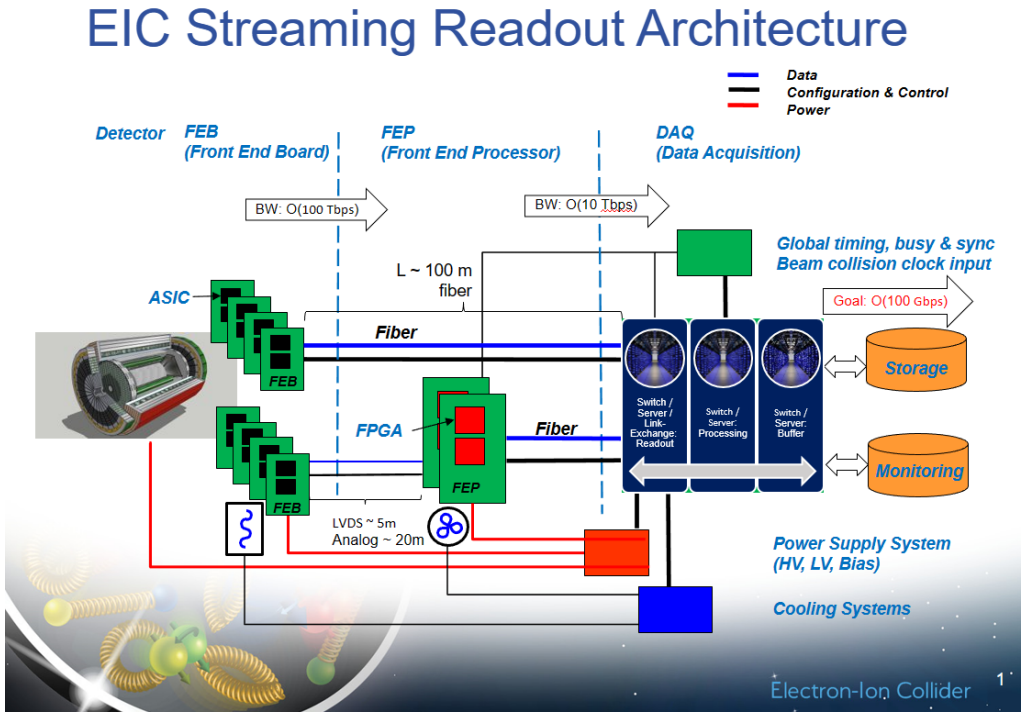
Electronics and DAQ WG status and activities

Conveners: Alexandre Camsonne, Chris Cuevas, Jeff Landgraf, Jo Schambach

ePIC Electronics and DAQ WG has been refining the readout system based on previous efforts

- ❑ Streaming Workshop (10 workshops)
  https://indico.jlab.org/event/519/overview (May 2022)
- ❑ Yellow Report
- ❑ eRD projects
- ❑ ECCE and Athena Proposals
- ❑ Special Special Streaming Workshop: ePIC DAQ and Electronics Protocols, Interface, Timing and Clock Distribution
  https://indico.bnl.gov/event/17452/ (December 2022)



Operational Requirements

- Bunch Crossing Rate 100MHz
- Maximum Interaction Rate 500KHz
- Budgeted Rate to tape 100Gb/s

Functional Characteristics

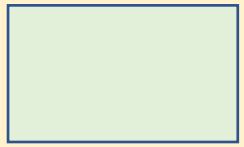
- Multiple Readout Technologies
- Triggerless operation (Detectors are self-triggered)
- Streaming (Deadtime-less, independent readouts)
- Aggressive Zero Suppression
- Large Channel Counts / Low occupancy
- Flexible Event Identification
- Potential for AI/ML integration

Working Towards CD2/3A

- ❑ 60% Design Maturity
  - Working towards pre-TDR (or draft of TDR)
  - Defined and Defendable Cost
    - Naming, Defining, & Counting the components
  - Define how DAQ will operate
  - Describe and defend that the system will work. Answer questions like:
    - What will the data volume on this link, and what kind of safety margin do you have?
    - Will radiation destroy your components, or make them misbehave?
    - How can you ensure that the data from these two detectors correspond to the same collision?
    - What happens if you get a hot channel?
    - How well can you measure the time of hits?
    - What happens if this board does not respond to signals?
    - ➢ Must define the protocols and information flow through the DAQ system

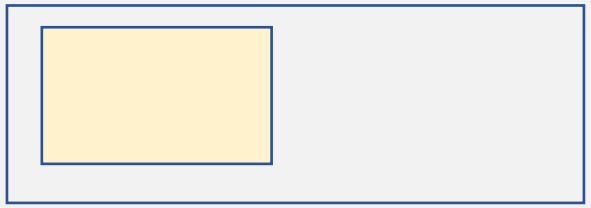
EPIC Electronics / DAQ

Standard Component Names and Functions



Global Timing Unit (GTU)

-Interface between collider, Run Control, & DAM
-Config & Control
-Clock & Timing



Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

Summary of Channel Counts

Detector Group	Channels					RDOs / Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	LAPPD				
Tracking	32B			100k		415	11	15	15
Calorimeters	88M*		150k			305	11	15	15
Far Forward	300M	2.3M	500			174	5	1	1
Far Backward		1.8M	700			113	4	100	2
PID		3M-50M	300k		150k	1070	41	1856	45
TOTAL	32B	7.1M-54M	450k	100k	150k	1662	72	1987	78

Noteworthy characteristics: MAPS – long integration time, highly zero-suppressed
SiPM – High dark currents at low thresholds, standard channels
*AstroPix – Depends upon SciGlass vs Imaging EMCAL decision

EPIC Detector Scale and Technology Summary:

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2	300	5Gb/sec	6-8	MAPS:	
MPGD tracking: 3 layers						
Calorimeters: Forward: LFHCAL pECAL HCAL inse Barrel: HCAL ECAL Imaging Backward: ECAL						
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAI 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorir 32 Silicon pad 4 silicon pixel 2 boxes scintill						l low
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters (Up/ Photon Detector						
PID-TOF						
PID-Cherenkov: dRICH pfRICH (if selected) mRICH (if selected) DIRC						

DAQ group has been trying to maintain the component counts because they directly impact our plans, but we don't define the detector needs.

We have had a lot of cooperation from the detector groups, (each group has presented their DAQ concepts and needs at our meetings) However we can always benefit from better communication

Don't hesitate to contact our conveners or to simply show up at our WG meetings with questions, needs, or changes.

https://indico.bnl.gov/category/409/

Please fill out the specific definitions of the readout chain for your detector!

https://wiki.bnl.gov/EPIC/index.php?title=Project_Information

EPIC Detector Scale and Technology Summary:

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2 32B pixels 5,200 MAPS sensors	400	5Gb/sec	10	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w its-3 improvements	Fiber count limited by Artix Transcievers
MPGD tracking: 3 layers	100k	15	<10Gb/sec	1	64 channel SALSA ASIC	Assume 512 Channel (8 ASIC)/FEB + 16 FEB/RDO
Calorimeters: Forward: LFHCAL ECAL W/SciFi Barrel: HCAL HCAL insert* ECAL (Imaging) SciFi/PB ASTROPIX ECAL (SciGlass) Backward: NHCAL ECAL (PWO)	 64k 19k 8k 8k 8k 88M pixels 8k 16.2k 3k	 80 75 32 32 32 24 32 18 12	15Gb/sec	10	SiPM using HGCROC &/or FPGA bases boards with FLASH ADC	ECAL will be SciGlass OR Imaging Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/fiber Assume FLASH FEB 16 ch * 16 FEB/RDO = 256 ch/fiber HCAL assume HGCROC ECAL assume FLASH for fiber calculations *HCAL inset not yet part of baseline
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 6 30 64 42 10 10 10 2	<1Gb/sec	5	 MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters (Up/Down) Photon Detector	 1.3M 480k 700	 80 32	100Gb/sec (<1 Gb/sec to tape)	4	 AC-LGAD / EICROC AC-LGAD / EICROC PMT / SiPM	 40cmx40cmx500um 30cmx20cmx500um Possible tracking layers
PID-TOF	3M-50M	240-500	6Gb/sec	12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov: dRICH pfRICH (or) mRICH DIRC	 300k 225k (26k, 25 LAPPD) 225k (76k, 75 LAPPD) 74k	 200 25 75 288	 1830Gb/s (<20Gbps to tape) 15Gbps 11Gb/sec	 20 1 2 6	 SiPM / ALCOR SiPM / ALCOR LAPPD LAPPD HDSoC64	 Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML) 12 boxes x 24 sensor x 4 asic x 64 ch

Summary of Current and Pending Activities

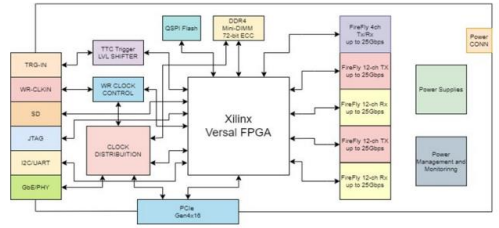
- Hardware Acquisition and Development
  - Have the opportunity buy 1 or 2 FELIX-182 boards being assembled for the ATLAS FELIX upgrade (Thanks to Hao Xu)
  - Obtaining FPGA Development Kits, Timing modules (which combined with existing electronics) will be sufficient to stand in for 5 GTU/DAM/RDO chains

- Evaluate Timing Synchronization Feasibility
  - Transmit clock by reconstructing it from data transmitted on fiber
    - 5ps jitter
    - Phase stability (even across power cycles)
  - Must demonstrate it is possible using the <$300 FPGAs for use in RDO.
  - Formed RDO/Synchronization and Timing group to demonstrate this
    - Jo Schambach, William Gu, Marius Wensing, Tonko Ljubicic, & Pietro Antonioli
  - First active development towards working RDO

Prototype: FLX-182

FPGA: Xilinx Versal Prime XCVM1802-1MSEVSVA2197
production device

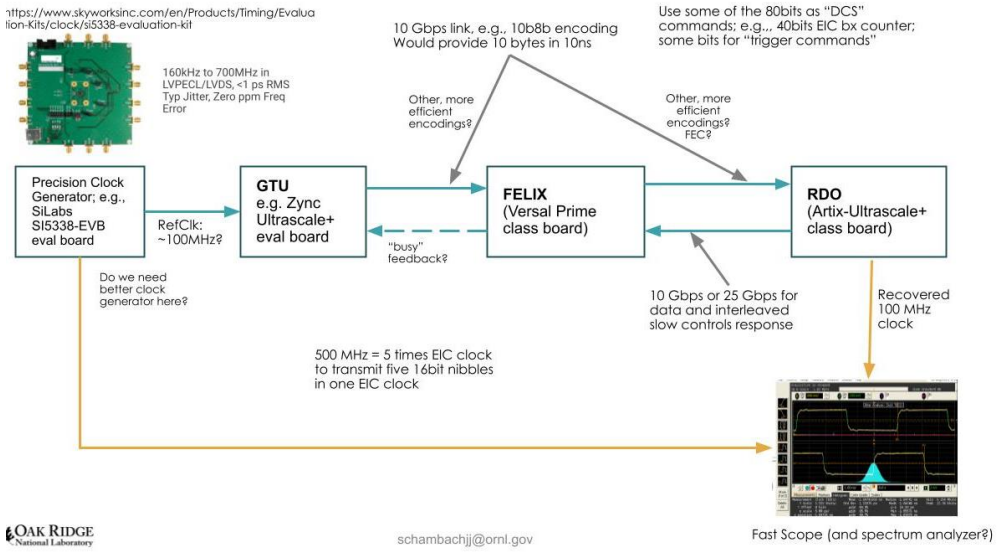
- PCIe Gen4 x16: PL and CPM compatible
- 24 FireFly links with 3 possible configurations
  - 24 links @25 Gb/s
  - 24 links @10 Gb/s (CERN-B-Y12)
  - 12 links @25 Gb/s + 12 links @10 Gb/s
- 4 FireFly links with 2 possible configurations
  - LTI interface
  - 100GbE
- Electrical signals on front panel
  - 3 inputs and 3 outputs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART



Block diagram of FLX-182

Brookhaven National Laboratory

11



OAK RIDGE National Laboratory

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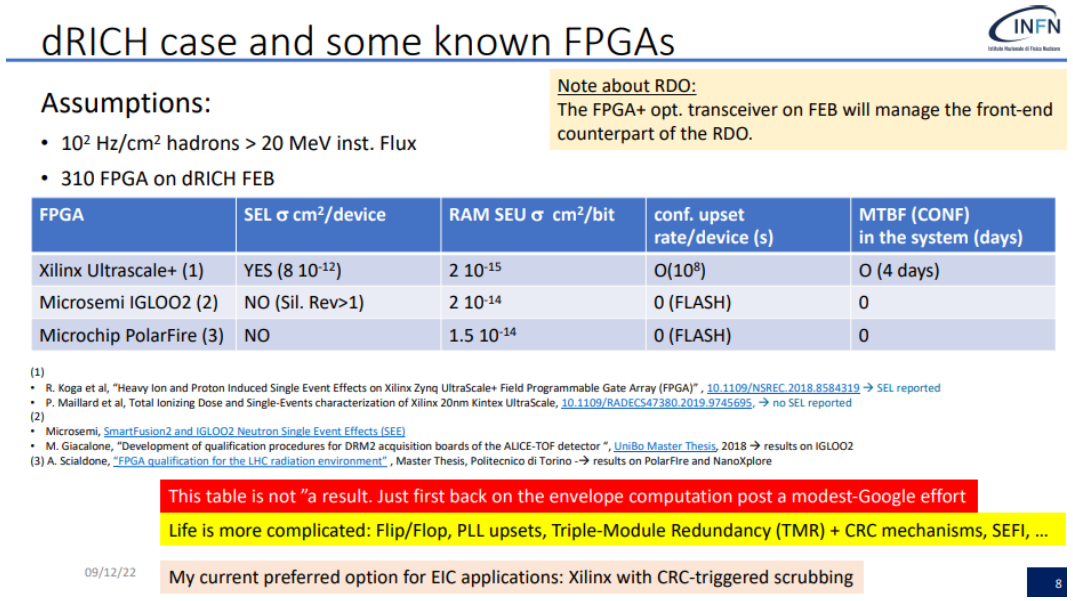
Fast Scope (and spectrum analyzer?)

Summary of Current and Pending Activities

- ❑ Need to define RDO locations

- ❑ Coordinate with backgrounds group
- ❑ Need to produce tables for each detector outlining best case / worst case / average case
  - ❑ Radiation effects (Pietro's Antonioli's talk at the December Workshop – useful despite his caveats!)
  - ❑ Backgrounds
  - ❑ Noise
  - ❑ Collision data volume using reasonable data models based upon ASIC functionality



dRICH case and some known FPGAs

Note about RDO:
The FPGA+ opt. transceiver on FEB will manage the front-end counterpart of the RDO.

Assumptions:

- 10^2 Hz/cm^2 hadrons > 20 MeV inst. Flux
- 310 FPGA on dRICH FEB

FPGA	SEL σ cm²/device	RAM SEU σ cm²/bit	conf. upset rate/device (s)	MTBF (CONF) in the system (days)
Xilinx Ultrascale+ (1)	YES ($8\ 10^{-12}$)	$2\ 10^{-15}$	O(10^8)	O (4 days)
Microsemi IGLOO2 (2)	NO (Sil. Rev>1)	$2\ 10^{-14}$	0 (FLASH)	0
Microchip PolarFire (3)	NO	$1.5\ 10^{-14}$	0 (FLASH)	0

(1)
- R. Koga et al, "Heavy Ion and Proton Induced Single Event Effects on Xilinx Zynq UltraScale+ Field Programmable Gate Array (FPGA)" , 10.1109/NSREC.2018.8584319 → SEL reported
- P. Maillard et al, Total Ionizing Dose and Single-Events characterization of Xilinx 20nm Kintex UltraScale, 10.1109/RADECS47380.2019.9745695, → no SEL reported

(2)
- Microsemi, SmartFusion2 and IGLOO2 Neutron Single Event Effects (SEE)
- M. Giacalone, "Development of qualification procedures for DRM2 acquisition boards of the ALICE-TOF detector ", UniBo Master Thesis, 2018 → results on IGLOO2

(3) A. Scialdone, "FPGA qualification for the LHC radiation environment" , Master Thesis, Politecnico di Torino -→ results on PolarFire and NanoXplore

This table is not "a result. Just first back on the envelope computation post a modest-Google effort

Life is more complicated: Flip/Flop, PLL upsets, Triple-Module Redundancy (TMR) + CRC mechanisms, SEFI, …

09/12/22

My current preferred option for EIC applications: Xilinx with CRC-triggered scrubbing

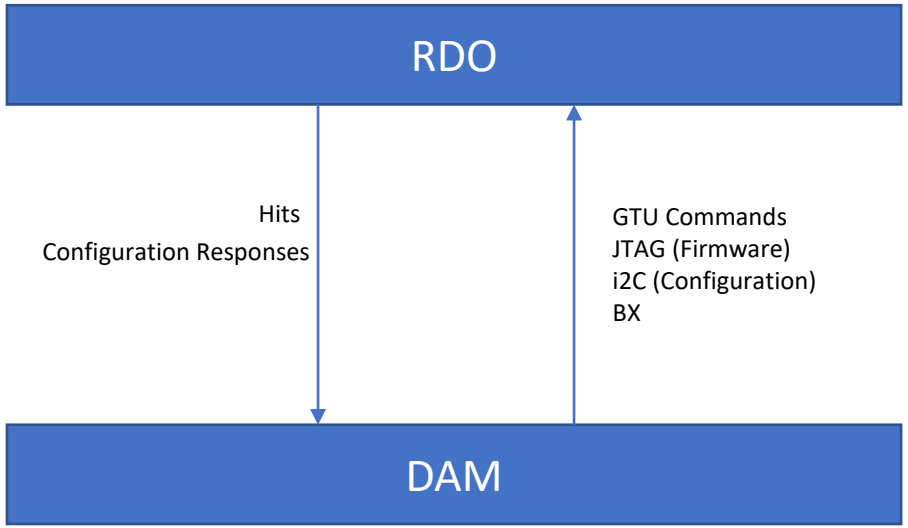
8

Summary of Current and Pending Activities

- ❑ Define Functional Protocols

- ❑ RDO <-> DAM
  - Multiple Functions
  - Maintain ASIC formats when possible, but apply DAQ headers
  - Multiplex multiple channels / FEB, multiple FEB / RDO
  - Time Frame definitions
    - Mechanism to handle “Channels off vs no hits”
    - Unit of packetization & formatting
  - Flow control mechanisms
  - ➢ All of these conflict with simple “oscilliscope” view of streaming
  - ➢ Discussed at December DAQ workshop, but the discussion demonstrated the lack of consensus

- ❑ RDO <-> FEBs
  - Electrical/Mechanical protocol
  - Data & Control Protocols



Summary of Current and Pending Activities

- ❑ Must define precisely what trigger capabilities we will have
  - Software trigger remains baseline for handling dRICH data volume and FB needs
  - Maintenance of hardware trigger options has been part of requirements, However
    - Any trigger would involve latency
    - No buffering existing in planned hardware for a store/forward trigger operation
    - No significant routes for significant explanation of a hardware trigger decision planned
    - ➢ “Traditional trigger system” not possible to put in after the fact

  - But many potential hardware trigger routes are open
    - Set busy / free busy mechanism
    - Artificial deadtime application
    - Software mediated hardware trigger
      - Use the DAM board or Readout computer as the buffer for a triggered system

Summary of Current and Pending Activities

- ❑ Need for integration with offline computing
  - Incorporate streaming digitization scheme into simulations
  - File management
  - Event selection
  - File Formats
  - Databases
  - Seamless incorporation of DAQ and offline code
  - Mechanisms for calibration turn around

Questions?