ePIC SVT configuration for eRD104/111/113 work

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EIC SC general meeting - 7 November 2022

EIC SC work for FY23

 The work of the EIC SC for the development of the EPIC silicon vertex and tracking (SVT) detector proceeds within the eRD104, eRD111, eRD113 projects.

- The combined aim of eRD104/111/113 for FY23 is to
 - Be ready to design the LAS sensor in FY24.
 - Reach a mature conceptual design of all items of the EPIC SVT (supported by prototyping/testing of components).

Full details in the proposals at https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23

- Work needs to start work towards these goals. Clearly, there still many open points and unknowns, but we need to start working on technical details and engineering aspects that will feed back important information to evolve the design.
- Let's discuss a starting point today \rightarrow ePIC SVT configuration v0.0

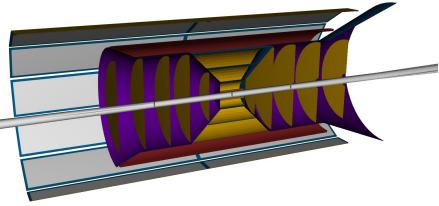
Current status: ePIC SVT layout

• EPIC SVT layout developed for the first simulation campaign

- 5 barrel layers, 5 disks per side
- See Ernst's talk at https://indico.bnl.gov/event/17418/
- Current implementation in DD4Hep in Shujie's talk at https://indico.bnl.gov/event/17394/
- This design includes only Si active area and simplified description of support structures and services \rightarrow Engineering details need to be worked out and added, see Nikki's talk next.
- Also, we are still using truth seeding and have no background embedded in simulations, so this layout might still change.

BARREL	r [mm]	l [mm]	X/X0 %	
Layer 0	36	270	0.05	
Layer 1	48	270	0.05	
Layer 2	120	270	0.05	
Layer 3	270	540	0.25	
Layer 4	420	840	0.55	

DISKS	+z [mm]	-z [mm]	X/X0 %	
Disk 1	250	-250	0.24	
Disk 2	450	-450	0.24	
Disk 3	700	-650	0.24	
Disk 4	1000	-900	0.24	
Disk 5	1350	-1150	0.24	

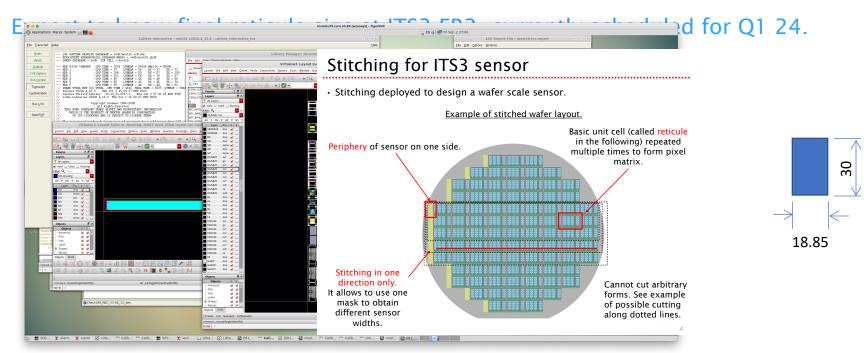


Current status: Sensor technology

- 65 m technology validation almost completed with testing of MLR1 structures \rightarrow no show stopper.
- ER1 submission of first, wafer-scale sensor by end of the year. Scope: learning about stitching and yield of large area sensor.

Expect to know yield in about 9 months to one year from now.

Reticule size not yet fixed, current assumption to progress our work on LAS and conceptual designs 18.85 mm x 30 mm.



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Layout Studies

EIC Vertex Layers

Use ITS3 curved wafer-scale stitched sensors Three layers (L0, L1, L2); Radii = 36 mm, 48 mm and 120 mm (see note below)

EIC Sagitta Layers

Baseline is smaller format stitched sensors (EIC LAS) on staves Two layers (L3, L4); Radii = 270 mm and 420 mm

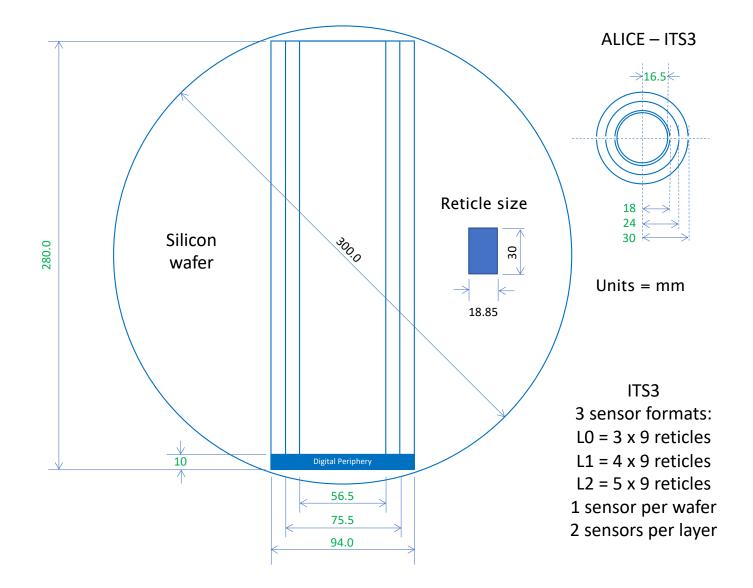
EIC Disks

Several sensor variants (different sizes) needed for improved yield and tiling flexibility Requires changes to stitching plan & periphery Studying optimum tiling geometry

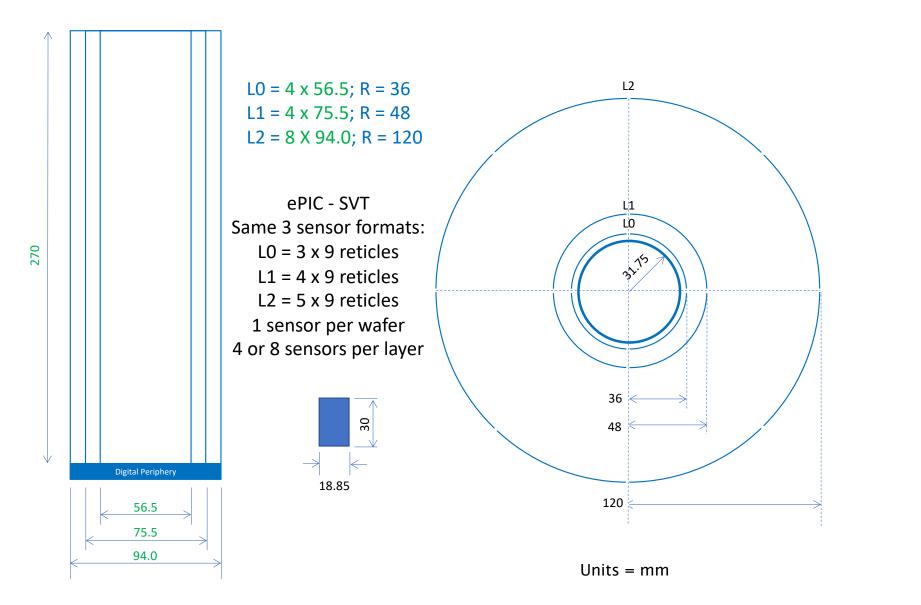
• What follows is based on studies done by Peter Jones

Note: beryllium beampipe outer radius = 31.75 mm Require spacing of 5 mm to first vertex layer for beam pipe bakeout

ALICE ITS3 Sensor Layout

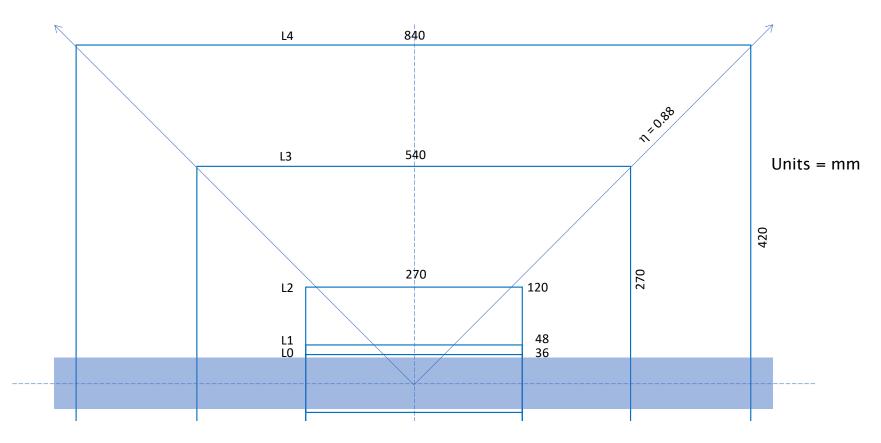


EPIC Vertex Layers



EPIC Vertex and Sagitta Layers

Note: these are active lengths; they do not include the periphery

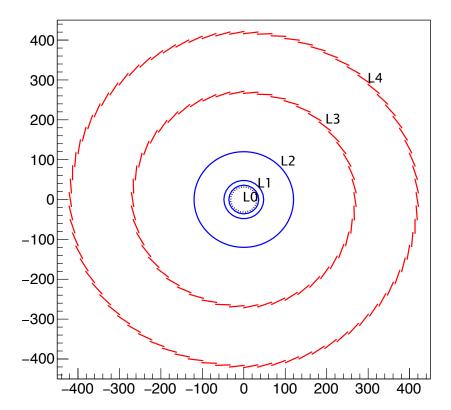


L0, L1 and L2 lengths are single sensors that are 270 mm long (9 reticles)

L3 length can be achieved using two sensors 270 mm long (9 reticles), or three sensors 180 mm long (6 reticles) Choice of two or three sensors may be decided by sensor yield

L4 length can be achieved using four sensors 210 mm long (7 reticles)

EPIC Sagitta Layers



ePIC ITS3-VL EIC-BL

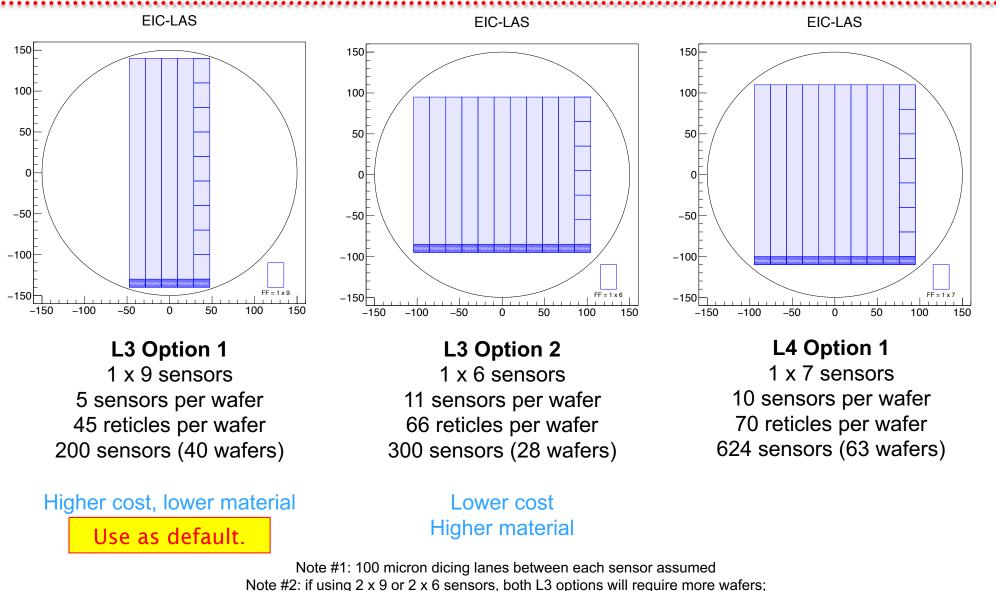
- Sagitta Layers
 Default design consists of ITS2-like staves
- L3

50 staves, 2 x 18.85 = 37.7 mm wide Mean radius = 268.4 mm Rφ overlap = 3.5 mm ~ 10% 2 x 2 = 4 or 2 x 3 = 6 sensors per stave Require 200 1x9 sensors or 300 1x6 sensors

■ L4

78 staves, 2 x 18.85 = 37.7 mm wide Mean radius = 418.5 mm $R\phi$ overlap = 3.5 mm ~ 10% 2 x 4 = 8 sensors per stave Require 624 1x7 sensors

Wafer Usage - Sagitta Layers



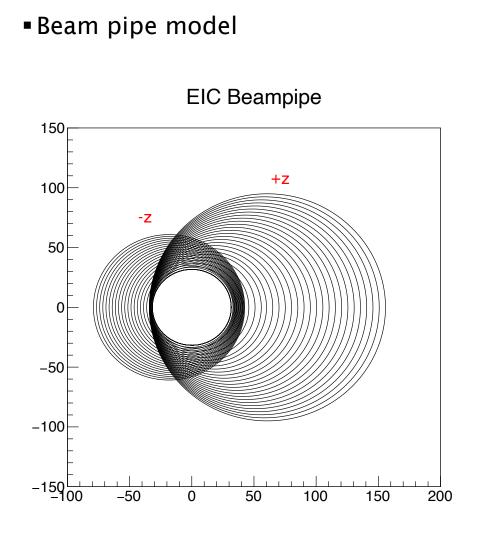
module concept needed (one module made of two 1x9/1x7 sensors for L3/L4)

Summary - Barrel v0.0

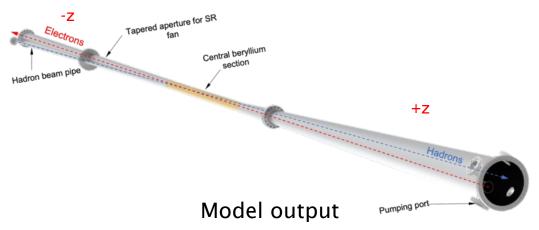
Note: these are active lengths; they do not include the periphery

Layers	Reticules	Sensor width x length [mm ²]	Layer length [mm]	Layer radius [mm]	Number of sensors per layer	Number of staves
LO	3 x 9	56.55 x 270	270	36	4	NA
L1	4 x 9	75.4 x 270	270	48	4	NA
L2	5 x 9	94.25 x 270	270	120	8	NA
L3	1 x 9	18.85 x 270	540	268.4	200	50
L4	1 x 7	37.7 x 210	840	418.5	624	78

Forward and Backward Disks



Beampipe profile; 100 mm steps

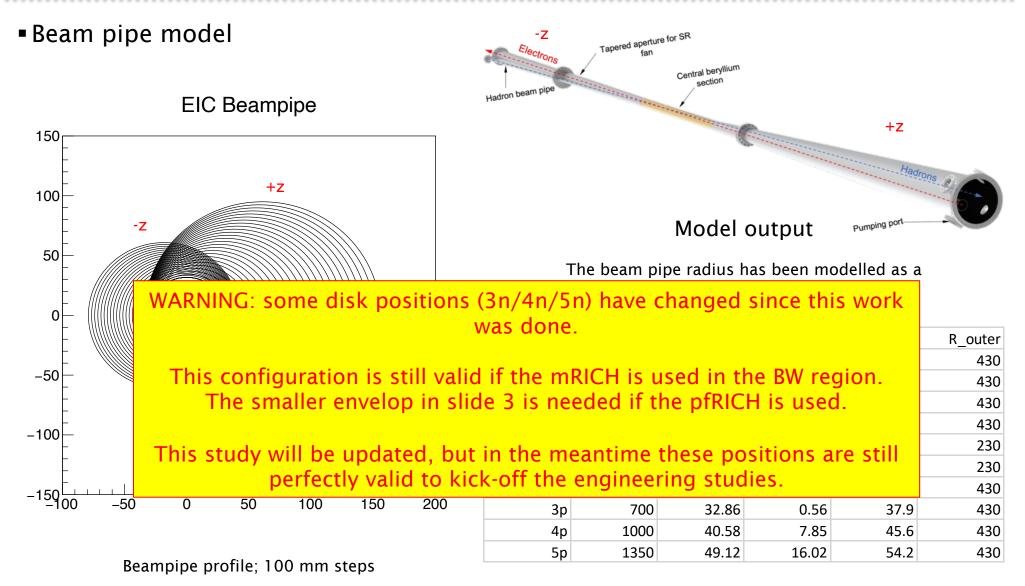


The beam pipe radius has been modelled as a function of z from the original CAD drawings

	Z - ePIC	R_bpipe	x_offset	R_inner	R_outer
5n	-1350	41.08	-5.30	46.1	430
4n	-1000	35.76	-1.81	40.8	430
3n	-700	31.76	0.00	36.8	430
2n	-450	31.76	0.00	36.8	430
1n	-250	31.76	0.00	36.8	230
1p	250	31.76	0.00	36.8	230
2p	450	31.76	0.00	36.8	430
Зр	700	32.86	0.56	37.9	430
4p	1000	40.58	7.85	45.6	430
5р	1350	49.12	16.02	54.2	430

Dimensions are mm

Forward and Backward Disks



Dimensions are mm

Disk Tiling

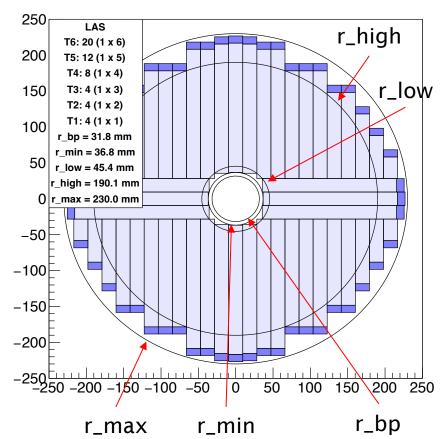
• More details on the disks tiling study and methods in the backup and here <u>https://indico.bnl.gov/event/17073/</u>

r_bp = beam pipe radius r_min = r_bp + 5 mm r_max = outer disk radius r_low = smallest radius with full acceptance r_high = largest radius with full acceptance

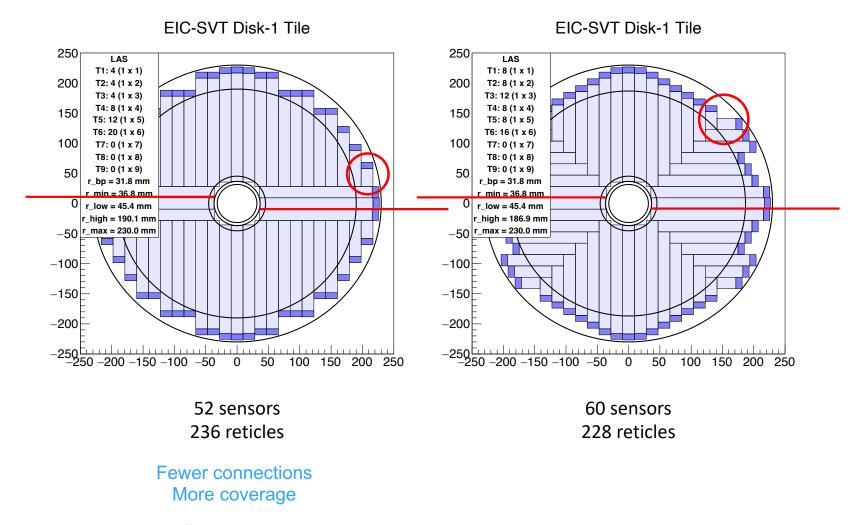
TX: YY $(1 \times X) \rightarrow$ on the disk there are YY Tiles made of one stitched row of X reticules.

Example: T5: 12 (1x5) \rightarrow on the disk there are 12 tiles made of one stitched row of 5 reticules (i.e. 18.85 mm x 150 mm).

EIC-SVT Disk-1 Tile

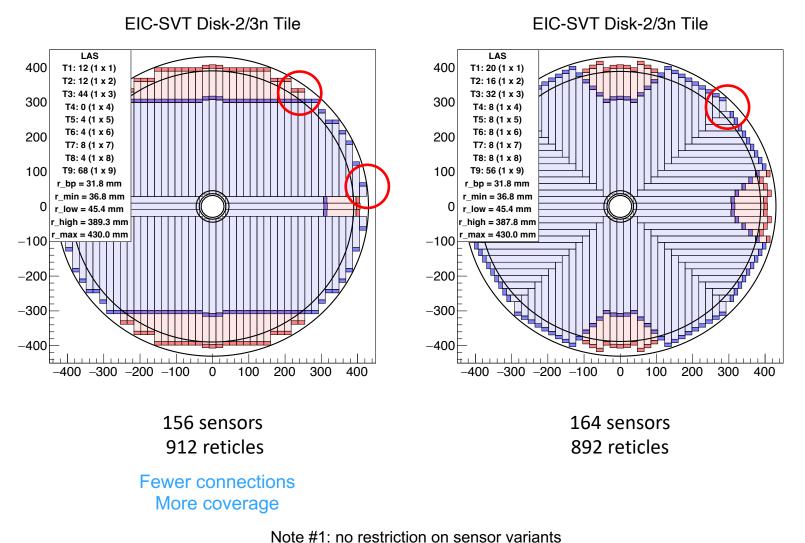


Disk 1 - Tiling Options



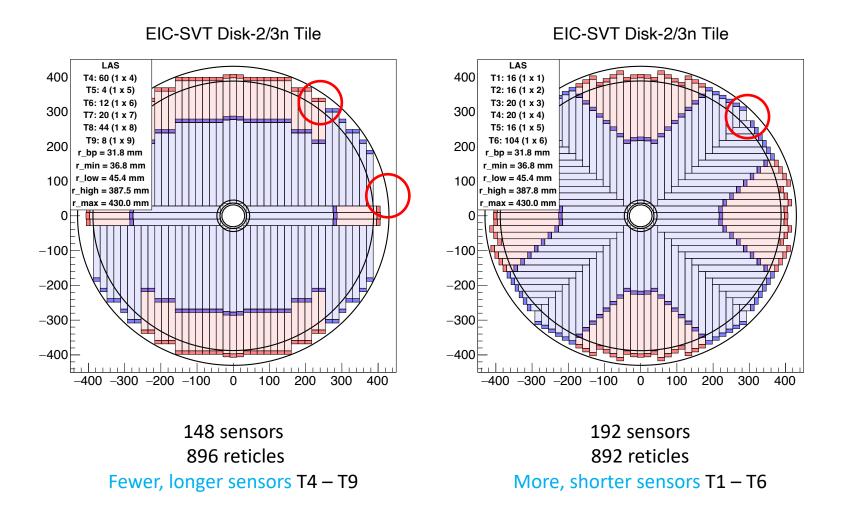
Note #1: no restriction on sensor variants but disk size imposes its own constraint Note #2: lines indicate possible division of disk into two halves for assembly around the beam pipe

Disk 2/3n – Tiling Options



Note #2: Sensors in red on reverse side of disk overlap digital periphery of inner sensors in blue

Disk 2/3n – Restricting Sensor Size



Use picket fence design as default for all disks.

Disk2/3n - Varying Restriction on Sensor Size

LAS 400 T3: 64 (1 x 3) T4: 0 (1 x 4) T5: 4 (1 x 5) 300 T6: 4 (1 x 6) T7: 16 (1 x 7) T8: 16 (1 x 8) 200 T9: 48 (1 x 9) r bp = 31.8 mm 100 r_min = 36.8 mm r low = 45.4 mm high = 389.3 mmT3 - T9max = 430.0 mm-100 -200 -300-400 -400 -300 -200 -100 0 100 200 300 400 EIC-SVT Disk-2/3n Tile LAS 400 T5: 72 (1 x 5) T6: 16 (1 x 6) T7: 48 (1 x 7) 300 T8: 4 (1 x 8) T9: 8 (1 x 9) r_bp = 31.8 mm 200 r min = 36.8 mm r low = 45.4 mm 100 r_high = 389.3 mm max = 430.0 mr T5 – T9 -100 -200 -300-400 -400 -300 -200 -100 100 200 300 400 0

EIC-SVT Disk-2/3n Tile

LAS 400 T4: 60 (1 x 4) T5: 4 (1 x 5) T6: 12 (1 x 6) 300 T7: 20 (1 x 7) T8: 44 (1 x 8) T9: 8 (1 x 9) 200 r_bp = 31.8 mm r min = 36.8 mm 100 r_low = 45.4 mm hiah = 389.3 mm max = 430.0 mn T4 – T9 -100-200 -300 -400

-300 -200 -100

-400

EIC-SVT Disk-2/3n Tile

Use T4 - T9 as default for disks 2 to 5.

Greater prospect of reducing number of sensor types with the simple tiling design

0

100

200

300

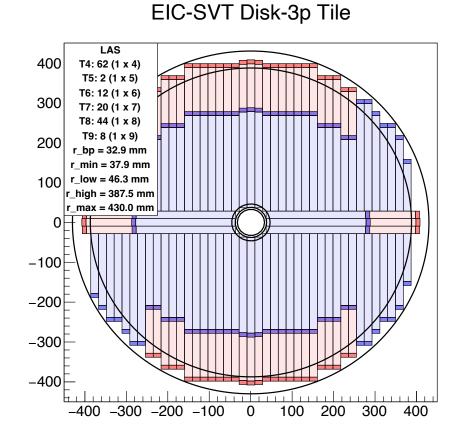
400

However, the reduction in sensor types pushes periphery inwards, adding material due to flex cables running over the outer sensors at larger radii

Note: shorter variants produce more sensors per wafer

Disk 3p

Note: disk center offset from x = 0 to accommodate beam pipe fan out

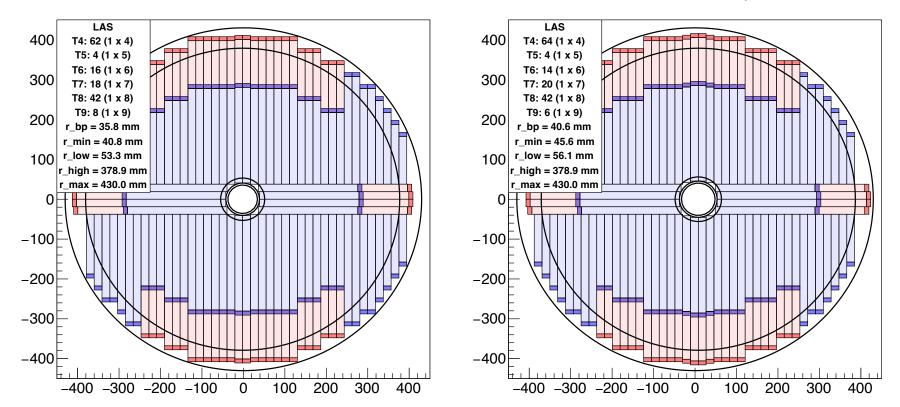


Disk 4n/p

Note: disk center offset from x = 0 to accommodate beam pipe fan out

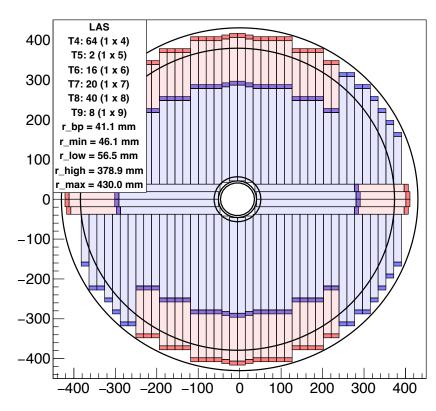
EIC-SVT Disk-4n Tile

EIC-SVT Disk-4p Tile



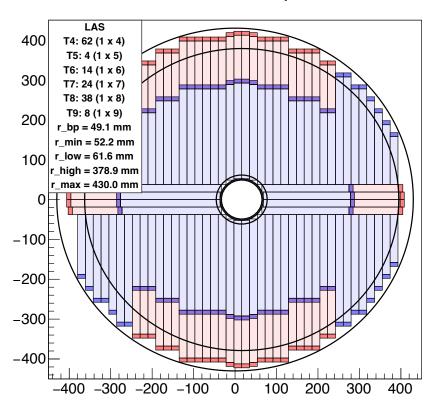
Disk 5n/p

Note: disk center offset from x = 0 to accommodate beam pipe fan out



EIC-SVT Disk-5n Tile

EIC-SVT Disk-5p Tile



BACKWARD									
	T1	Т2	Т3	T4	T5	Т6	T7	Т8	Т9
Disk 1	4	4	4	8	12	20	0	0	0
Disk 2	0	0	0	60	4	12	20	44	8
Disk 3	0	0	0	60	4	12	20	44	8
Disk 4	0	0	0	62	4	16	18	42	8
Disk 5	0	0	0	64	2	16	20	40	8
				FORV	VARD				
	T1	T2	Т3	T4	T5	Т6	Τ7	Т8	Т9
Disk 1	4	4	4	8	12	20	0	0	0
Disk 2	0	0	0	60	4	12	20	44	8
Disk 3	0	0	0	62	2	12	20	44	8
Disk 4	0	0	0	64	4	14	20	42	6
Disk 5	0	0	0	62	4	14	24	38	8

......

Mechanical Design as Implemented in DD4HEP

Basic model for sagitta layers
 44 tilted triangular staves (not 50 or 78)
 Silicon + Al + carbon fiber plates
 No truss structure; cooling pipes, etc.

Support cone design issues

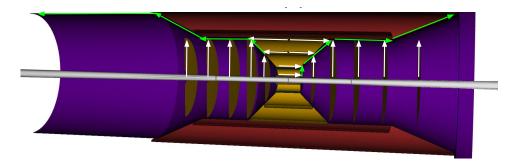
Routing of cables to/from first two vertex layers is assumed to be radially outwards

Implies a 90-degree bend in the FPC

No location identified for the patch panel needed to connect FPC to external cables

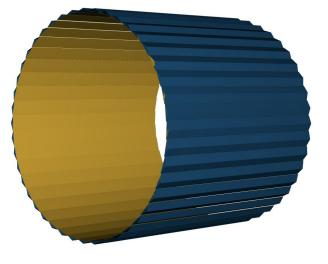
ex and sagitta layers does not ery or FPC

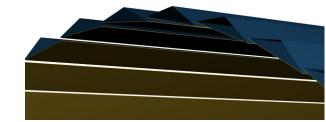
disk is smaller than the radius cone



Figures from Shujie Li (LBNL)

More engineering challenges discussed in Nikki's talk.





Summary

Vertex Layers (L0, L1, L2)

Will use ITS3 wafer-scale sensors

L2 now at R = 120 mm

- R1 R0 = 12 mm
- R2 R1 = 72 mm

For ITS3 the layer spacing is 6 mm Requires new mechanical design

Sagitta Layers (L3, L4)

L3 length (540 mm) can be made with 2 sensors of length 270 mm (9 reticles)

L3 could also made with 3 sensors of length 180 mm (6 reticles) to improve wafer usage

Second option requires services running over the stave; also cooling for the periphery \rightarrow First option as default for now

L4 length (840 mm) can be made with 4 sensors of length 210 mm (7 reticles)

Same comment about services and cooling

Module concepts needed for L3 and L4

Tiling of disks

Method to tile the disks developed Vertical tiles (design #1) are preferred Fewer sensors providing greater coverage Studies of restricted sensor sizes on-going Need to convert this into estimate for the number of wafers needed (with inputs from designers)

Mechanical Design

Need to investigate an ITS2-like stave option for the sagitta layers

Need to address cable routing, cooling and compatibility with EPIC support cone

No conceptual design the disks; not clear that air cooling will work here

Conclusion

. . .

 The proposed configuration is based on The ePIC SVT configuration for the first simulation campaign (Oct/Nov 2022). A reticule size of 18.85 mm x 30 mm. An exercise of how to best tile staves and disks using 1. and 2.

This starting point is not yet informed by

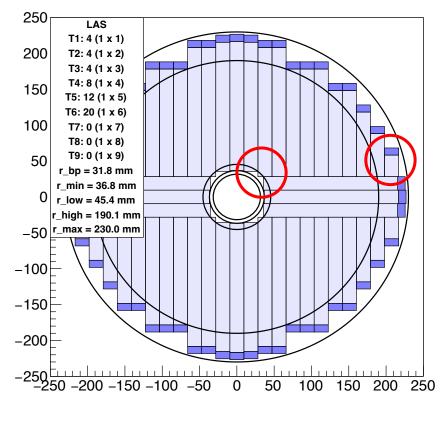
Sensor yield (i.e. stitched rows of 9 reticules might not be possible) → biggest unknown!
Engineering aspects of staves/disks, mechanics, cooling, integration, etc.
Designers input on LAS.

Let's use this configuration as starting point to work on some of these missing inputs and iterate on the SVT design with more information.

Backup

- Aim of the study
 - Investigate sensor (LAS) formats needed
 - Try to restrict the number of variants
 - Try to keep periphery to outer radius of disk
- Tiling strategy
 - Two designs starting with a central cross
 - Design #1 = vertical tiles/sensors (shown)
 - Design #2 = herringbone pattern (alternating vertical and horizontal tiles)
 - No sensor overlap on same side of disk
 - Sensor variants are assumed to be 1 reticle width by up to 9 reticle lengths

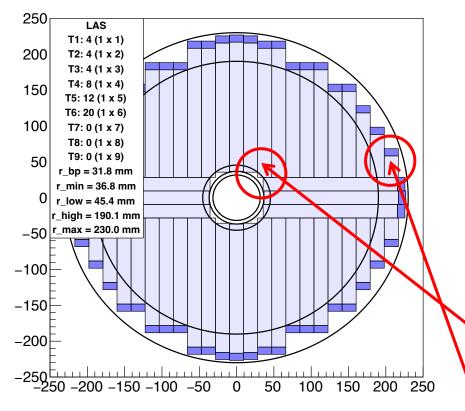




Example: Disk 1 z = +/-250 mm

Disk Tiling Algorithm

EIC-SVT Disk-1 Tile

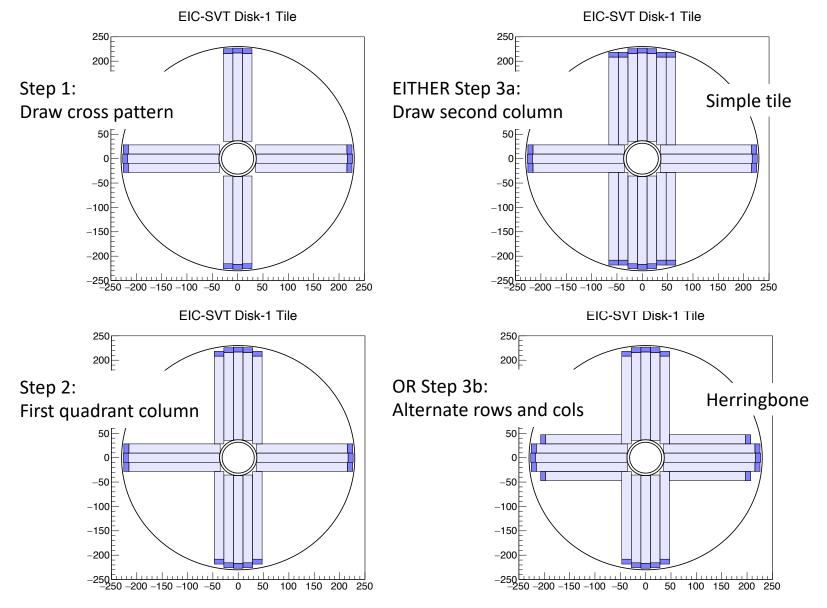


z = +/- 250 mm Central cross = 3 sensors

The algorithm

- Try to keep periphery to larger radii
- Two designs, each based on a central cross pattern smaller than the inner diameter of the disk
- Design #1 = vertical tiles (shown)
- Design #2 = herringbone pattern (alternating vertical and horizontal tiles)
- The minimum disk radius (r_min) is 5 mm larger than the beam pipe radius (r_bp) for bake out
- Sensor and periphery must be contained within the min and max radii of the disk (r_min and r_max).
- For each disk, the algorithm calculates the smallest and largest radii with full acceptance (r_low and r_high)
- The algorithm does not permit any sensor overlap
- Acceptance at small radii could be improved by allowing some sensor overlap; placing overlapping sensors on the reverse side of the disk (in progress)
- Limits on the max and min sensor length can be applied
- Study the number of sensor variants that are needed

Disk Tiling Method



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