EPIC Electronics and DAQ

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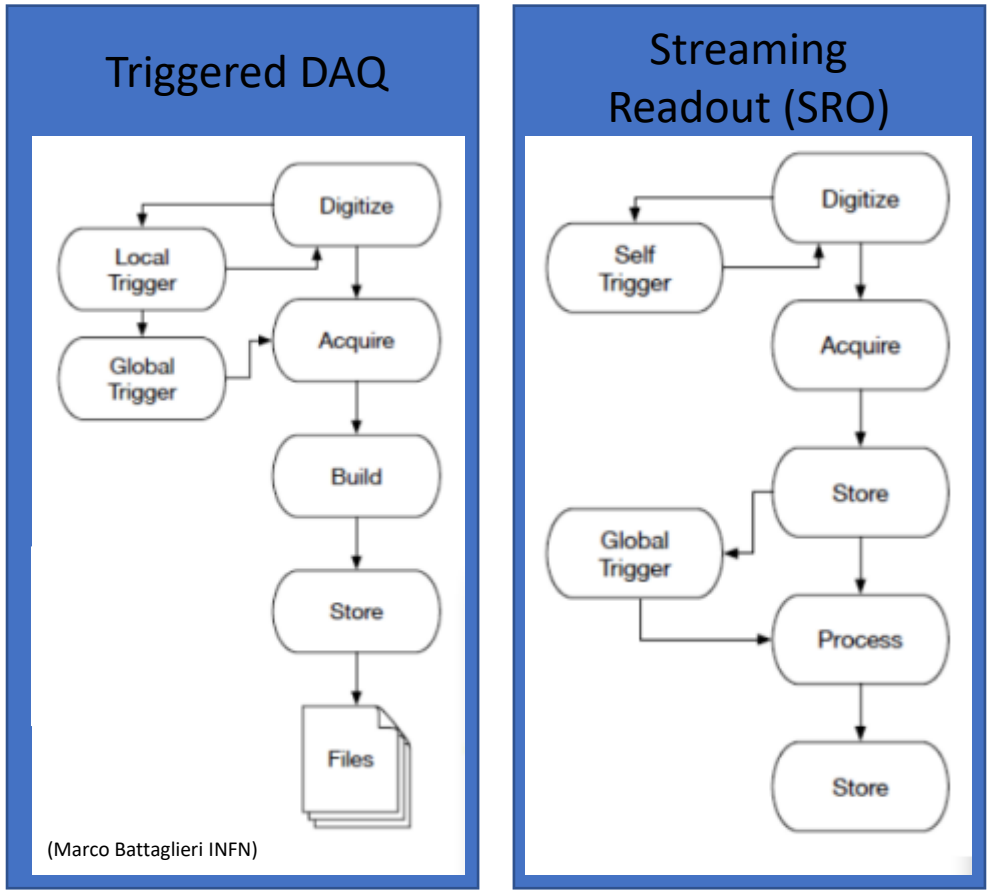
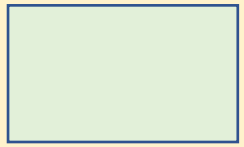
EPIC Streaming Readout



Features of EPIC SRO

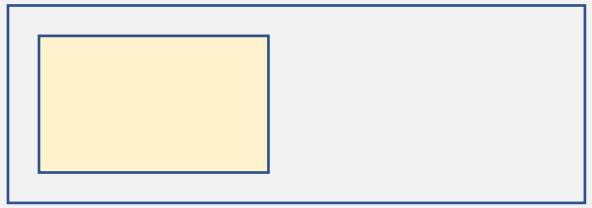
- No global trigger
  - No global trigger electronics
  - Zero-suppress early (ASICs)
- Hits identified by time stamp rather than by event
- Flexibility in event selection
  - Can be performed in CPU, FPGA, or GPU
  - Can be performed with all channels available
  - Can be performed at different times, using different methods, for different purposes
- Cons
  - SRO has greater sensitivity to noise and background

EPIC Electronics / DAQ



Global Timing Unit (GTU)

-Interface between collider, Run Control, & DAM
-Config & Control
-Clock & Timing



Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Shared / (potential variations)	Shared / (FELIX)	COTS / Ethernet
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock &Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control -Processing	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring -Processing
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

Scale and main challenges

Detector Group	Channels				Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD				
Tracking	32B			100k	500	13	15	15
Calorimeters	50M		150k		2050	50	15	15
Far Forward	300M	2.3M	500		174	5	1	1
Far Backward		1.8M	700		113	4	100	2
PID		3M-50M	600k		638	40	3220	45
TOTAL	32B	7.1M-54M	750k	100k	3475	112	3350	78

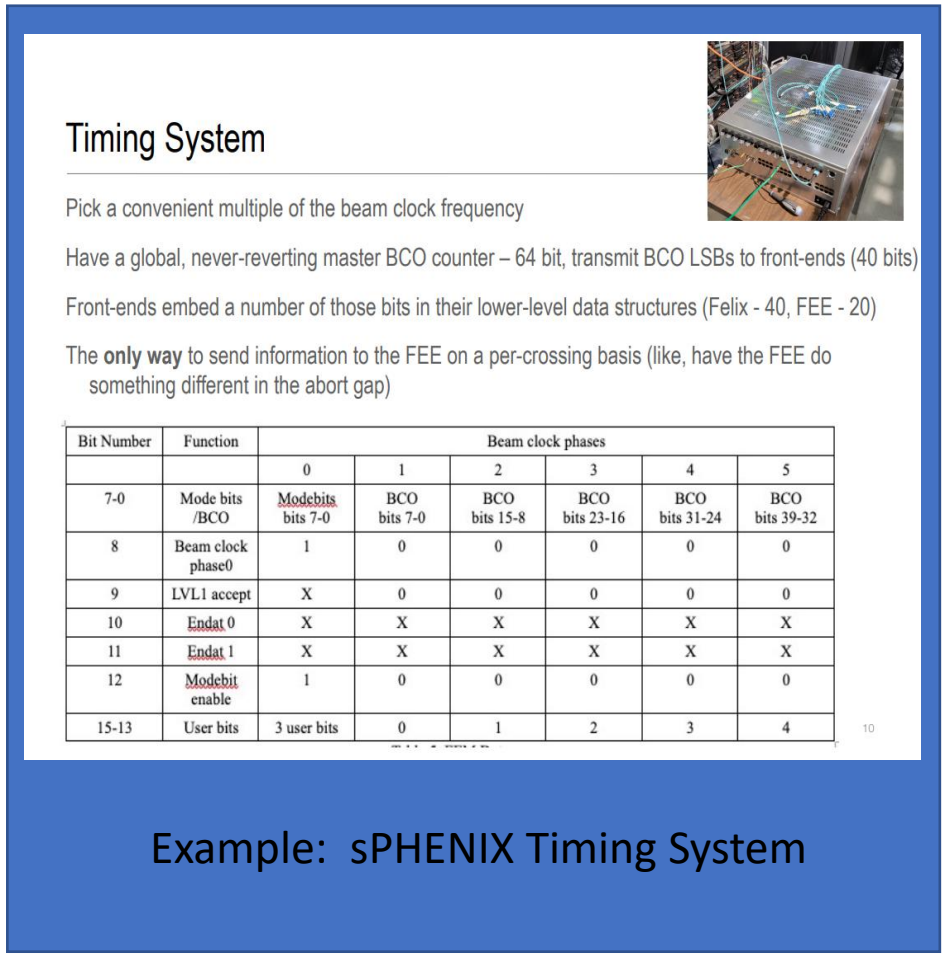
- Function of DAQ is to reduce ~1M channels @100MHz → 100Gb/sec
- The primary strategy is aggressive zero suppression, which is an important requirement for all detector readouts (ASICs, Sensors, FEBs, and RDOs)
- Other secondary strategies include
  - Feature extraction (cluster finding, tracking etc)
  - Noise identification and removal
  - Algorithmic data compression
  - AI/ML to be evaluated for each of the above
  - Software triggering

Full Detector Summary

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2 32B pixels 5,200 MAPS sensors	300	5Gb/sec	6-8	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w its-3 improvements	
MPGD tracking: 3 layers	100k	200	<10Gb/sec	4-5	64 channel SALSA ASIC	Assume 512 Channel (8 ASIC)/FEE
Calorimeters: Forward: LFHCAL pECAL HCAL inset Barrel: HCAL ECAL Imaging Backward: ECAL	 60k 25k 8k 3k (25k?) 8k 50M pixels 25k	 950 400 125 50(400) 125 (note) 400 2050(2400)	15Gb/sec	50	SiPM using HGCROC &/or FPGA bases boards with FLASH ADC	
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 6 30 64 42 10 10 10 2	<1Gb/sec	5	 MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters (Up/Down) Photon Detector	 1.3M 480k 700	 80 32	 100Gb/sec (<1 Gb/sec to tape)	4	 AC-LGAD / EICROC AC-LGAD / EICROC PMT / SiPM	 40cmx40cmx500um 30cmx20cmx500um Possible tracking layers
PID-TOF	3M-50M	240-500	6Gb/sec	6-12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov: dRICH pfRICH (if selected) mRICH (if selected) DIRC	 300k 225k 74k	 200 150 288 288	 1830Gb/s (<20Gbps to tape) 1380Gb/s (<15Gb/s to tape) 11Gb/sec	 20 14 5 6	 SiPM / ALCOR SiPM / ALCOR HDSoC64	 Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML) 12 boxes x 24 sensor x 4 asic x 64 ch

Timing System

- Timing System must synchronize data between detectors. This requires ~1ns resolution
- Timing System must provide high resolution 5ps phase stability to actual bunch crossing persisting over power cycles for selected detectors
  - Plan is reconstructed clock transmitted via DAM boards
- Timing system is the only source for real-time global information
  - Beam information
  - Control zero-suppression, feature finding, AI/ML algorithms
  - Flow Control (time frames, start, stop, common busy, triggering)
- Timing System Protocol
  - Expect about 100bits / BX
    - 64 bits BX, 30 bits for control & commands
    - Modes for configuration / firmware uploads
- Data protocol
  - DAQ defined header for time windows
  - Internal data format agnostic



Timing System

Pick a convenient multiple of the beam clock frequency

Have a global, never-reverting master BCO counter – 64 bit, transmit BCO LSBs to front-ends (40 bits)

Front-ends embed a number of those bits in their lower-level data structures (Felix - 40, FEE - 20)

The **only way** to send information to the FEE on a per-crossing basis (like, have the FEE do something different in the abort gap)

Bit Number	Function	Beam clock phases					
		0	1	2	3	4	5
7-0	Mode bits /BCO	Modebits bits 7-0	BCO bits 7-0	BCO bits 15-8	BCO bits 23-16	BCO bits 31-24	BCO bits 39-32
8	Beam clock phase0	1	0	0	0	0	0
9	LVL1 accept	X	0	0	0	0	0
10	Endat 0	X	X	X	X	X	X
11	Endat 1	X	X	X	X	X	X
12	Modebit enable	1	0	0	0	0	0
15-13	User bits	3 user bits	0	1	2	3	4

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Example: sPHENIX Timing System

Expected DAM Board

Tasks:

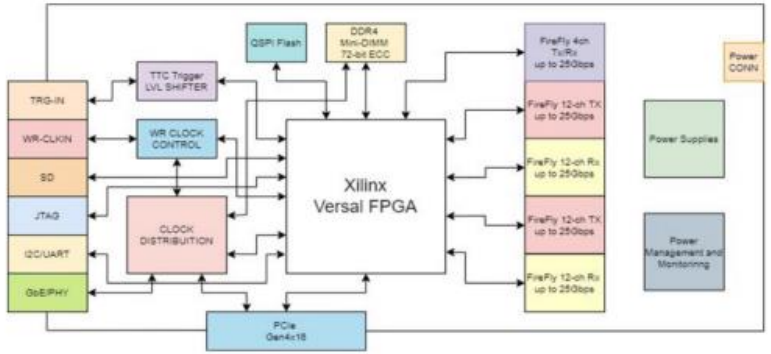
- Potential reconfiguration of firefly
- Firmware development
  - Clock and timing system
  - EPIC formats
  - Upstream configuration and Firmware handling
  - Software Triggering
  - Potential AI/ML in FPGA
- BNL board designed for Atlas (Hao Xu), but we will need to manage of procurement and fabrication

Next Generation FELIX

Prototype: FLX-182

FPGA: Xilinx Versal Prime XCVM1802-1MSEVSVA2197
production device

- PCIe Gen4 x16: PL and CPM compatible
- 24 FireFly links with 3 possible configurations
  - 24 links @25 Gb/s
  - 24 links @10 Gb/s (CERN-B-Y12)
  - 12 links @25 Gb/s + 12 links @10 Gb/s
- 4 FireFly links with 2 possible configurations
  - LTI interface
  - 100GbE
- Electrical signals on front panel
  - 3 inputs and 3 outputs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART

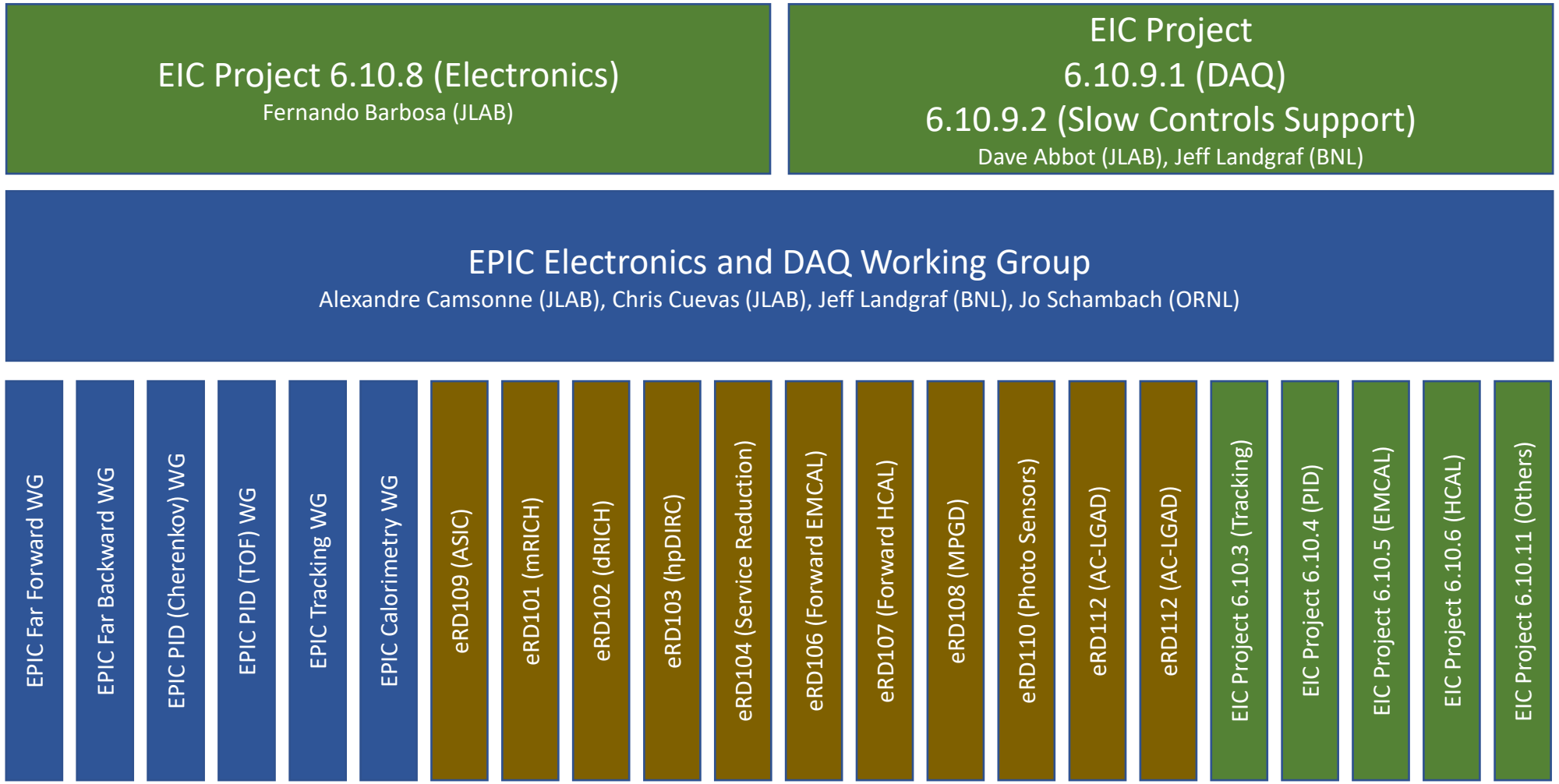


Block diagram of FLX-182

Notes: The Xilinx Versal Prime is a SoC.- Dual Core ARM Cortex
Power usage ~133W. No power through PCIe.
Can be implemented as a stand alone device (no Server)

Electronics / DAQ Related Group Structure

(This is *NOT* an org chart!!!!!)



There are many groups with effort & stakes defining the electronics

- Effort towards defining each detectors specific readout chain and responsibilities is starting
- Need for central coordination/tracking of the electronics projects and (aspirationally) the Electronics and DAQ WG is supposed to take on this role

To Get Involved:

Email: eic-projdet-daq-l@lists.bnl.gov
Meetings: https://indico.bnl.gov/category/409/
Upcoming Workshop, Dec 9th: https://indico.bnl.gov/event/17450/