R&D on Time-of-Flight for ePIC

Brookhaven™
National Laboratory

U.S. DEPARTMENT OF ENERGY

Project Goal: Completing the readout chain for an AC-LGAD based TOF

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Background of the planned project

- Project Context:
  - AC-LAGD for future detectors: ATLAS RP@HL-LHC, LHCb upgrade, ALICE3, NA62, PIENUX, TRIUMF, and space missions PAN, EIC RP, **EIC TOF** (R&D ongoing)
  - For front end electronics (FEEs) Application Specific Integrated Circuits (ASIC) are being developed to handle granularity & low timing contribution (R&D ongoing e.g. EICROC)
  - AC-LGAD and ASICs are best choice for future Highly Granular Timing Detectors (HGTD) such as barrel and forward Time of Flight (TOF) for ePIC.
  - A complete readout (RO) chain **R&D is missing** (FLEX, on/off-detector electronics)
- What is needed:
  - **Development of the readout chain for TOF (and processing architecture)**
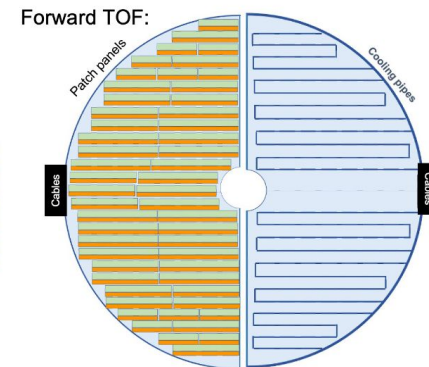
Background of the planned project
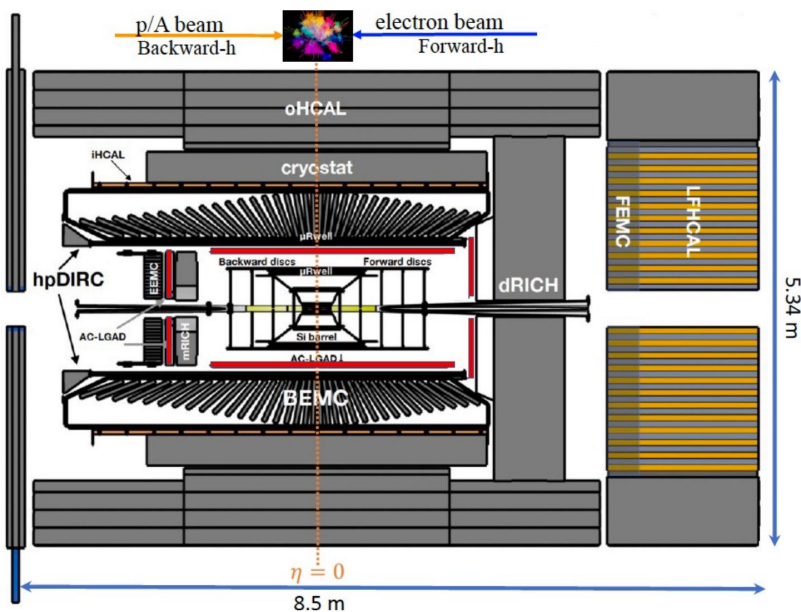
barrel TOF @ePIC
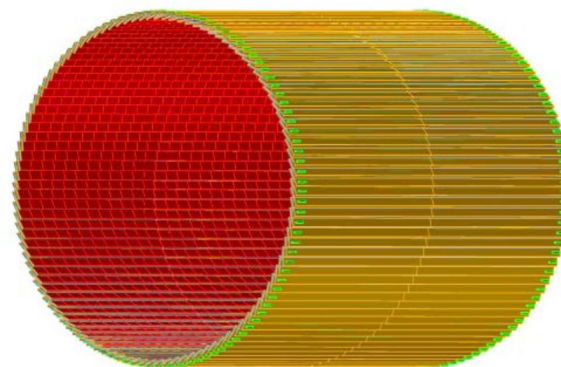
Stepping stone: STAR IST design
288 tilted staves, each 135 cm long
Sensor: AC-LGAD strips
Area: 11 m^2, Time Res: 30 ps,
Pos Res: 30μm in r-φ
Rad length: 0.01 X_0

forward TOF@ePIC

Stepping stone: CMS
Endcap Timing Layer design,
Sensor: AC-LGAD pixel
Area: 2.2 m^2
Time Res: 25ps
Pos Res: 30μm in x-y
Rad length: 0.08

Active R&D focused working group TOF@ePIC & LGAD- consortium (eRD112)

3

Background of the planned project

AC-LGAD: designed and produced by BNL and KEK/Tsukuba with Hamamatsu Photonics (HPK, Japan)

ASIC EICROC first design schematic, IJCLab (Orsay), Ecole Polytechnique/Omega and CEA (Saclay), submission (March 2022) to TSMC French funding is being used, next Nov 2022
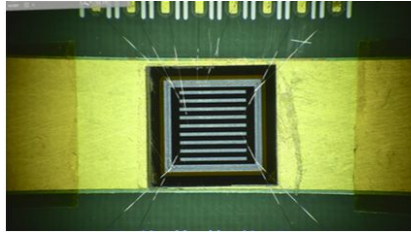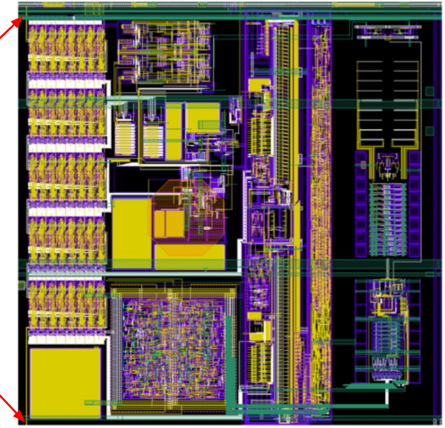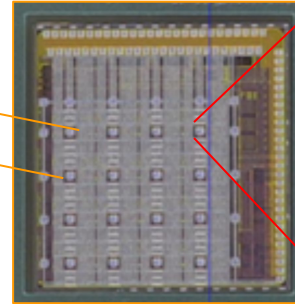
BNL 5-200   BNL 10-200

EICROC0 4x4

Heller et al:
https://arxiv.org/pdf/2201.07772.pdf
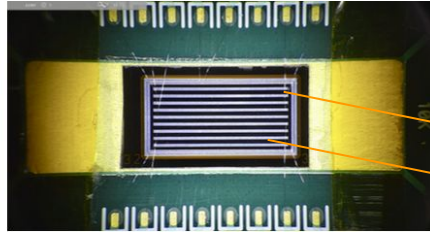
AC-LGAD: AC-coupled Low Gain Avalanche Diode
EICROC: Application Specific Integrated Circuit for AC-LGAD@EIC

| Slow control | PA +discri | TOA TDC | 8b 40M ADC |

Time Res. <30 ps, Pos. Res. 3-30 μm, Rad Length< $0.01\ X_0$, long strip sensors (500 μm pitch). We plan to procure wire-bonded ASIC+sensor from BNL

Engineering design: 4x4, 500 μm pitch

We plan procure prototype ASICs mounted on PCB from French group and perform testing

4

Signal extraction and readout of AC-LGAD device

When radiation hits, charge sharing happens between multiple strip: characteristic of AC-LGADs
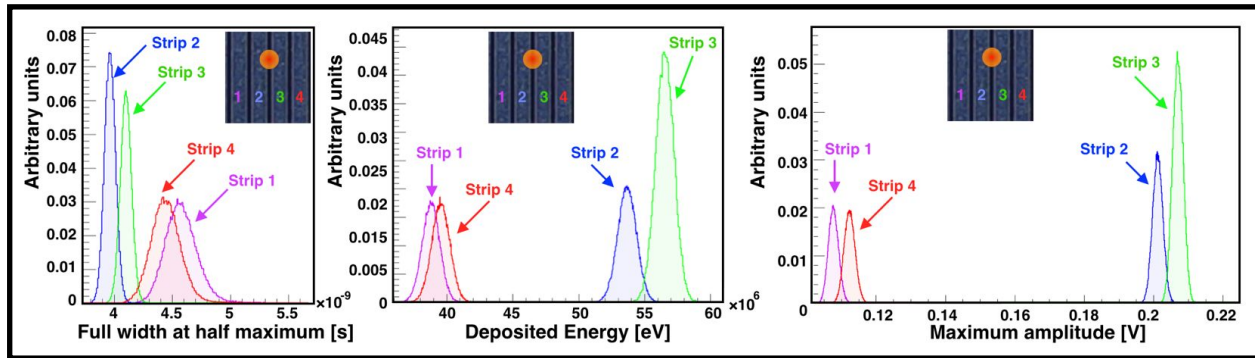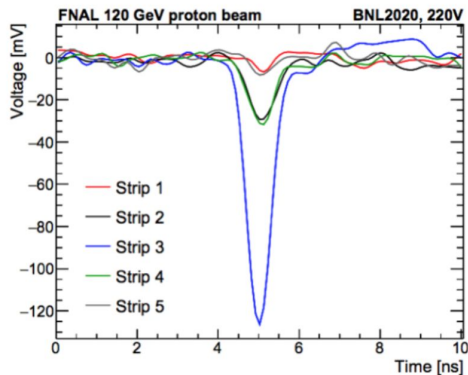
Fast rise time

Information of hit manifest on amplitude, width & integral of pulse correlated across many strips: no clear pattern, complicates position res.
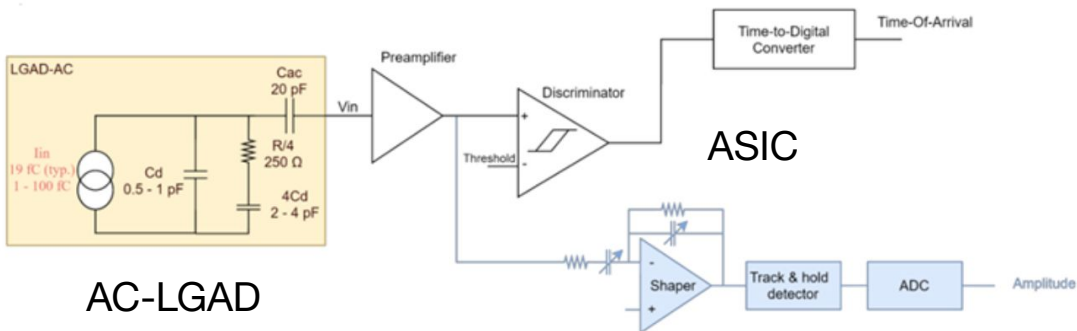
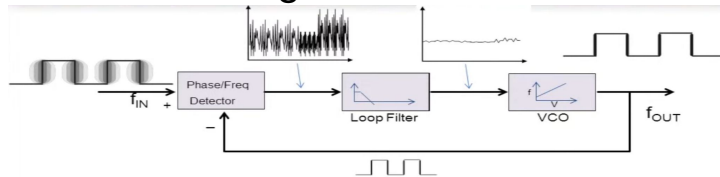ASIC

AC-LGAD

Jitter & loss of information in the readout electronics

Clock cleaning

Achieving 30 ps timing resolution is challenging

Outline of what we want to do

- Project Description:

   Develop the readout chain from the dedicated ASIC to downstream off-detector electronics. We will start by procuring a Xilinx Dev Kit and characterizing it to read the EICROC0 and EICROC1 mounted on the PCB developed by the French team. For the first step the sensor is not essential and we will only study the basic performance of the chip. The first tests of functionality of the FEEs will focus on noise studies, time walk and jitter and compatibility with the TOF requirements. Along this line we will also explore various timing chips ("clock cleaners and jitter removal") which is a critical component for any TOF based detector.

Complete chain: ATLAS HGTD as a stepping stone
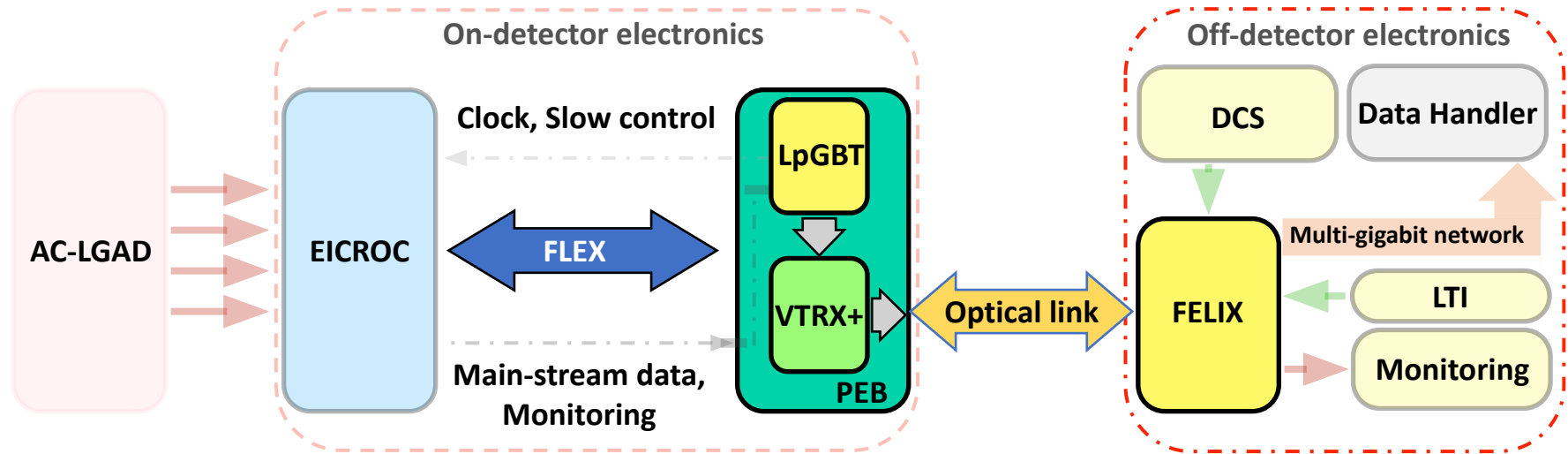
PEB: Peripheral Electronic Board
LPGBT: Low Power GigaBit Transmission chip
VTRX+: Versatile Link+ optical module
DCS: Detector Control System
LTI: Local Trigger Interface
FELIX: Front End LInk eXchange

Example of a readout chain

We will use ATLAS HGTD as a stepping stone to develop the electronics and data flow architecture

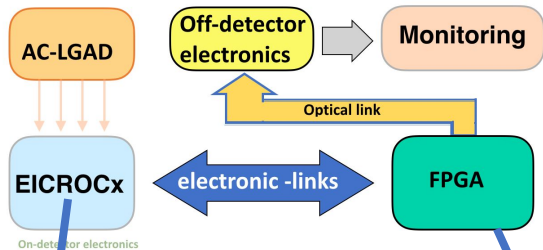# The readout chain: ATLAS HGTD as a stepping stone
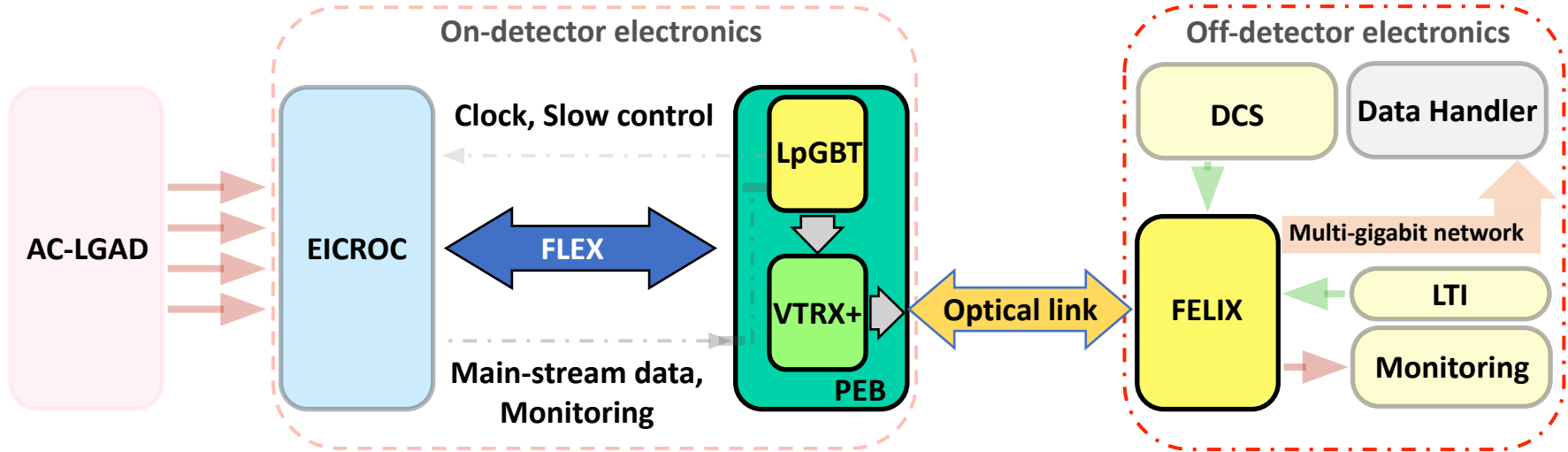
We will use a simplified version of this for our readout chain development with several modifications such as LpGBT → FPGA, PEB→ RDO
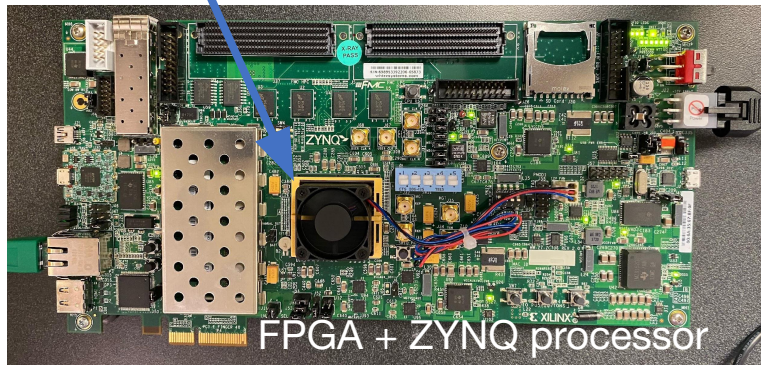
Our simplified setup for TOF@ePIC R&D
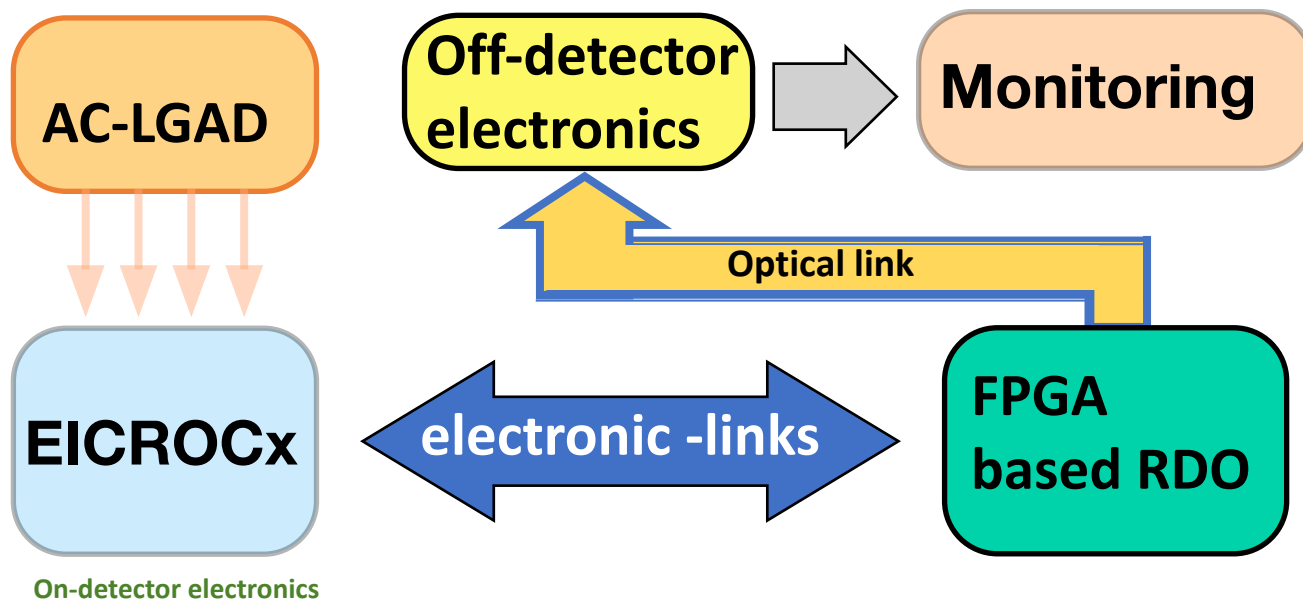
Key development and optimization of the readout chain: Compatibility with EICROCx, TOF specific low jitter timing system, Jitter cleaning, transmission of clock through FELX cable, streaming readout of the mainstream data
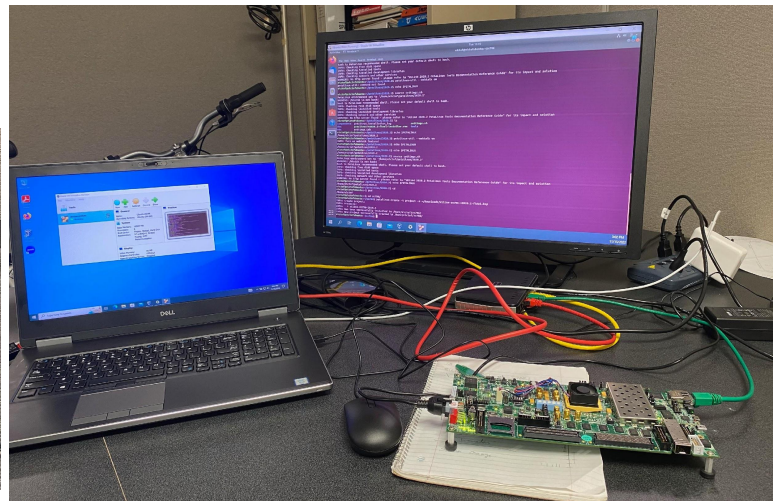
Progress so far at BNL with Xilinx dev kit

AC-LGAD → EICROCx (On-detector electronics)

Off-detector electronics → Monitoring

Optical link

electronic -links

FPGA

ASIC at BNL

EICROC0 on PCB

Xilinx dev kit at BNL

FPGA + ZYNQ processor

Read out board development setup at BNL
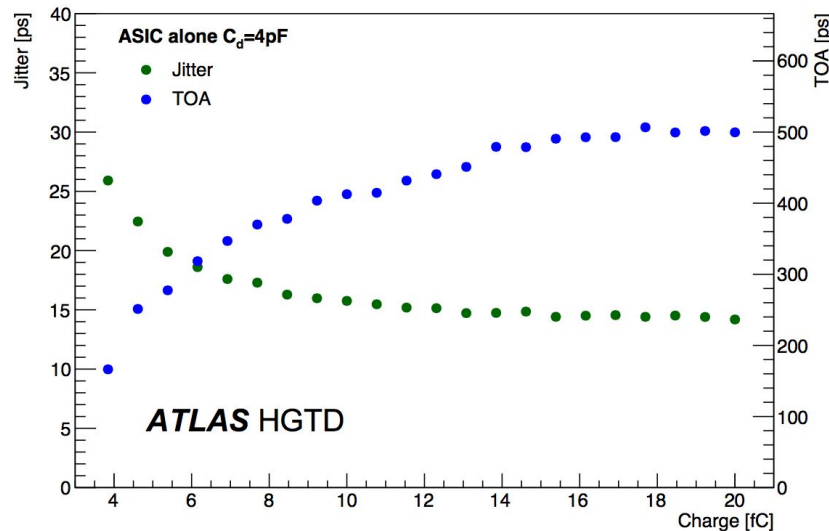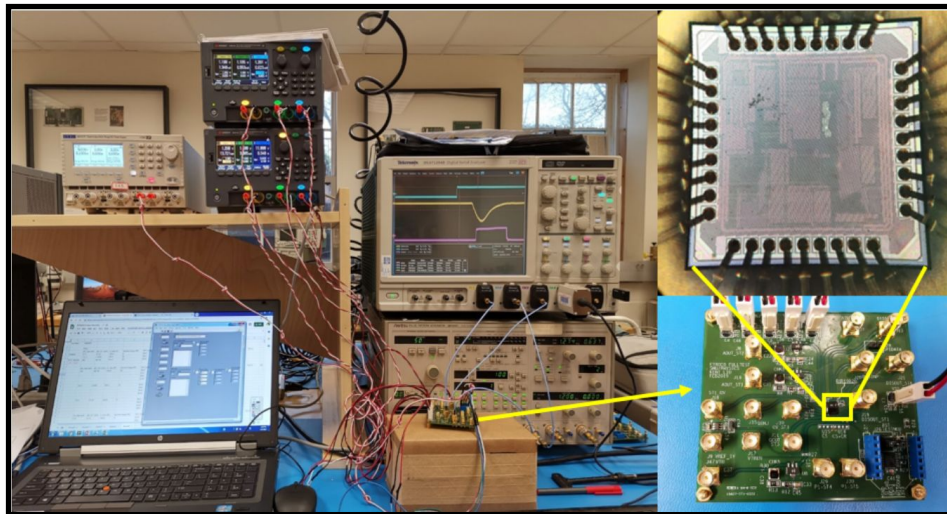
What we have so far for the first step of R&D:

1) One Xilinx dev. kit (ZYNQ processor + FPGA),

2) EICROC0 on a PCB

We also have one wire bonded sensor + ASIC
(not essential for the first step of development)

Coming soon: test stand in Physics Room- 1-227

ATLAS-TDR-031:
https://cds.cern.ch/record/2719855

Example of ETROC0 test stand: https://arxiv.org/abs/2012.14526

Key areas of testing: Timing resolution, noise studies, time walk and jitter cleaning, change of efficiency with input charge, bandwidth suitability for high luminosity environment, and power dissipation per area. Compatibility with EICROCx, global clock distribution.

We will provide input for future ASIC prototype submissions

Summary

- Deliverable for FY 2023:
    Development of the preliminary prototype of an integrated readout board that supports the first iterations of the EICROCx.
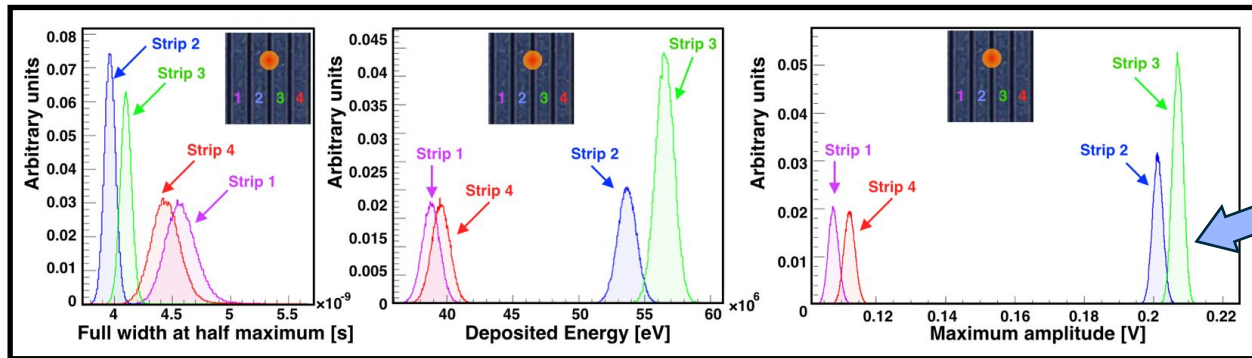
- Ultimate Plan:
    Design the overall architecture of the hardware including, the design of the cable, the optimization of streaming data, and the interface of the timing and control signals
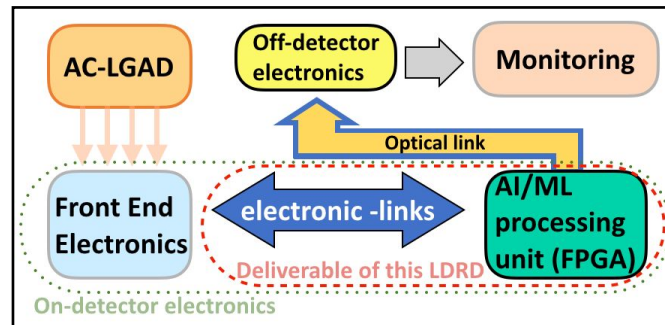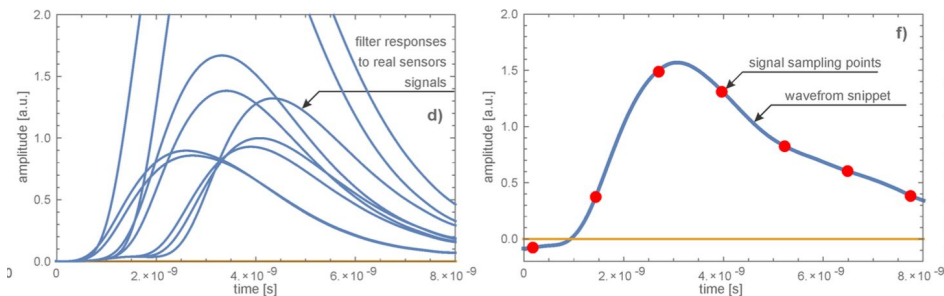
- Other futuristic opportunities:
    Using AI/ML to improve the readout performance

Other opportunities: Using AI/ML to improve R/O

Previous R&D only used this information from up to 4 strips

- Train AI/ML regressors to target high level observables.
  ‣ Convolutional Neural Networks (CNN) capable of reproducing standard LGADs waveforms demonstrated
  ‣ Capable of lossless data-compression, coping with high throughput of HEP/NP experiment
  ‣ FGPA based implementation is realistic
  ‣ Correlated signals from multiple electrodes of the sensors → improvement hit's position accuracy.