

# EPIC DAQ WG Agenda (11/17/2022)

- Upcoming schedule
- Standardization of component names poll results
- Readout Chain Definition Initiative
- RDO & Timing development proposal
- EPIC collaboration meeting at JLAB (Jan 9 – 11, 2023)
- Update on Workshop (Alexandre)

# Upcoming Schedule

- Nov 24<sup>th</sup>, No DAQ WG Meeting (Thanksgiving)
  - Dec 1<sup>st</sup>, DAQ WG Meeting
  - Dec 6<sup>th</sup>, Project Review (Calorimetry)
  - Dec 8<sup>th</sup>, No DAQ WG Meeting (Workshop)
  - Dec 9<sup>th</sup>, Workshop
  - Dec 15<sup>th</sup>, DAQ WG Meeting
  - Dec 22<sup>nd</sup>, likely no DAQ WG Meeting (vacations...)
  - Dec 29<sup>th</sup>, likely no DAQ WG Meeting (vacations...)
  - Jan 5<sup>th</sup>, DAQ WG Meeting
  - Jan 9-11 Collaboration Meeting
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- Jan 31 – Feb 3<sup>rd</sup>, Project OPA Status Review – Confirm CD-2/3a plans (Formal change control becomes required)
  - June 2023, Preliminary Design and Director's Reviews (first draft pre-TDR)
  - October 2023, DOE CD 2/3a OPA Review and ICR (requires pre-TDR)
  - January 2024, DOE CD 2/3A ESAAB Approval

# Standardization of Component Names Poll Results

## Winners:

Readout Board: RDO

Data Aggregation Module: DAM

Global Timing Unit: GTU

1. What should we call the "Electrical Optical Interface" (The green shaded component in today's presentation)

[More Details](#)

Electrical Optical Board (EOB)	1
Front End Processor (FEP)	7
Readout Board (RDO)	8
Readout Unit (ROI)	2
Aggregator (AGG)	1



2. What general term should we use for the "DAM" boards

[More Details](#)

FELIX	2
Data Aggregation Module (DAM)	10
Sample Aggregation Module (S...	3
Receiver Board (RB)	4



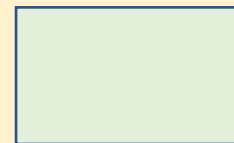
3. What term should we use for the timing system components laying between the collider and the DAM board

[More Details](#)

Timing System	3
Timing and Control (TAC)	5
Clock and Command Distributio...	5
Global Timing Unit (GTU)	6

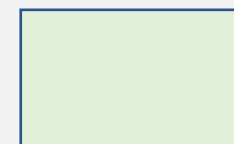
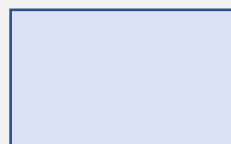
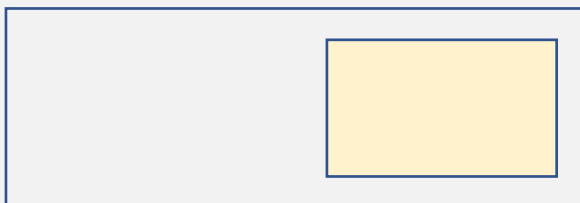


# EPIC Electronics / DAQ



Global Timing Unit (GTU)

- Interface between collider, Run Control, & DAM
- Config & Control
- Clock & Timing



Name	Adapter	Sensor	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Shared / (potential variations)	Shared / (FELIX)	COTS / Ethernet
Function	<ul style="list-style-type: none"> <li>-HV/Bias distribution</li> <li>-HV divider</li> <li>-Interconnect routing</li> </ul>	<ul style="list-style-type: none"> <li>-Multi-Channel Sensor</li> </ul>	<ul style="list-style-type: none"> <li>-Amplification</li> <li>-Shaping</li> <li>-Digitization</li> <li>-Zero Suppression</li> </ul>	<ul style="list-style-type: none"> <li>-Communication</li> <li>-Aggregation</li> <li>-Formatting</li> <li>-Data Readout</li> <li>-Config &amp; Control</li> <li>-Clock &amp; Timing</li> </ul>	<ul style="list-style-type: none"> <li>-Computing Interface</li> <li>-Aggregation</li> <li>-Software Trigger</li> <li>-Clock &amp; Timing</li> <li>-Config &amp; Control</li> </ul>	<ul style="list-style-type: none"> <li>-Data buffering and sinking</li> <li>-Run Control</li> <li>-Calibration Support</li> <li>-QA / Scalers</li> <li>-Collider Feedback</li> <li>-Event ID/Building?</li> <li>-Software Trigger</li> <li>-Monitoring</li> </ul>
Attributes	<ul style="list-style-type: none"> <li>-Sensor Specific</li> <li>-Passive</li> </ul>	<ul style="list-style-type: none"> <li>-MAPS</li> <li>-AC-LGAD</li> <li>-MCP-PMT</li> <li>-SiPM</li> <li>-LAPPD</li> </ul>	<ul style="list-style-type: none"> <li>-ASIC/ADC</li> <li>-Discrete</li> <li>-Serial Link</li> </ul>	<ul style="list-style-type: none"> <li>-FPGA</li> <li>-Fiber Link</li> </ul>	<ul style="list-style-type: none"> <li>-Large FPGA</li> <li>-PCIe</li> <li>-Potentially Ethernet</li> </ul>	

# Readout Chain

## Definition

## Initiative

1. Define/Document Readout Chains
2. Define who is responsible for designing them
3. Our WG will coordinate... Know who is doing the work, know the status, ensure that the electronics works together, fits with the RDO protocols, etc...

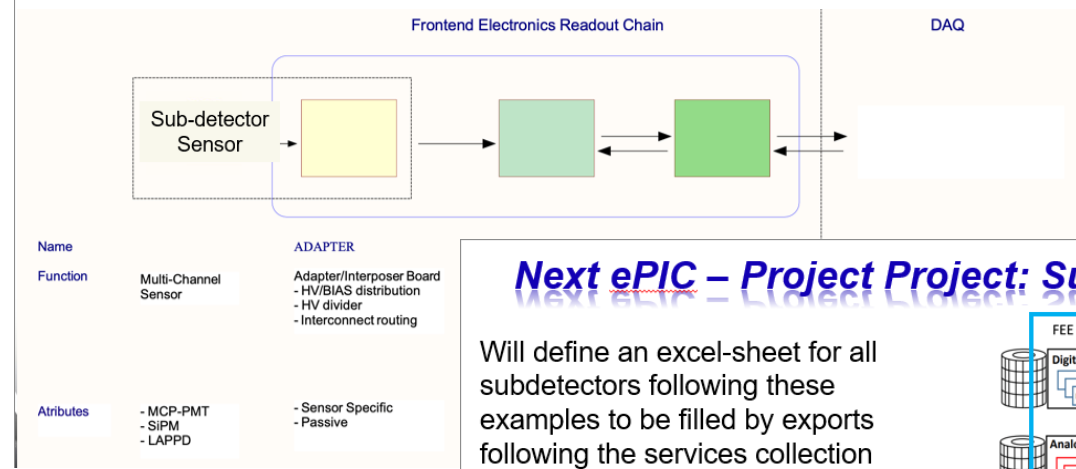
### Next ePIC – Project Project: Subdetector Readout Chains

Collaboration between ePIC DAQ/Electronics WG and Project Electronics & DAQ CAMs

Goal:

define readout chain for each subdetector

- determine synergies between different subdetectors
- determine what support is needed from the project in design of front-end-electronics

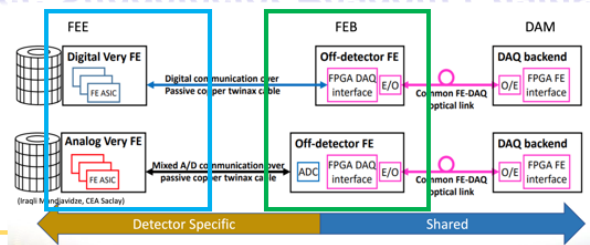


### Next ePIC – Project Project: Subdetector Readout Chains

Will define an excel-sheet for all subdetectors following these examples to be filled by exports following the services collection

Streaming Data Test Stand  
E. Jastrzebski, JLab, 11/9/2022

Detector name	Streaming Data Test Stand
Sensor type	Prototype GEM (Mississippi State University)
Sensor details	triple GEM, 240mm x 240mm x 16mm
# Sensors	768 strips (384 X, 384 Y), 400µm pitch
# Readout channels	714 strips instrumented (357 X, 357 Y)
GEM HV	-4KV @ 737 uA (iseg SHQ 126L supply)
Readout ASIC	SAMPA V4, 32 channels
ASIC details	Charge sensitive amplifier: 20 mV/FC, 30 mV/FC sensitivity Shaping circuit: 160 ns peaking time (4 <sup>th</sup> order semi-Gaussian) ADC: 10 bit resolution, sampling up to 20 MHz Digital output: 11 serial e-links (up to 320 Mbps each), max 3.52 Gbps Power: 1.25V (600mW)
ASIC modes	Streaming, triggered DAS - Raw ADC samples, all channels (5 MHz sampling) DSP – threshold zero suppression (up to 20 MHz sampling)
Front-end card (FEC)	ALICE TPC (LHC Run 3) – 5 SAMPA/FEC, 5 FECs Each FEC connected to GEM via 4 x 40 signal ribbon cables (18")
FEC Data Transport	Dual optical links (CERN GBTx – VTRx), 4.48 Gbps each
System Timing	Global clock (40 MHz), sync, trigger through GBT downlink
Readout Unit	C-RORC (ALICE/ATLAS LHC Run2) modified for use with GBT link PCIe Gen2 (40 Gbps)
Patch panel	No / YES # channels per board
Design-Workforce:	ePIC collaboration group / EIC Project / both



**Sensor detector specific**

**FEB: detector specific**

**FEP: hopefully one board common to many subdetectors**

# RDO & Timing Development Proposal

- We have more definition of intended activities needed as proposed by Tonko, Jo, and others.
  - Agreement that needs to be started soon, so let's get this moving
  - Mostly similar but some differences, for example whether Versa development Kit for FELIX stand-in, Wait for actual FELIX board, Use Artix for FELIX stand-in.
  - Multiple people want to be involved
  - Need some specialized lab equipment, potentially, but this equipment is available in collaborators labs
  - Do we need explicit engineering help or no?

# Collaboration Meeting

- Jan 9<sup>th</sup> – 11<sup>th</sup> at JLAB
- Plenary sessions only, hybrid
- Plan is 1 hour slots for each working group to organize, with contributions from working group members
  - Readout Chain Definitions and responsibilities
  - Possible data volume studies
    - We need to start paying attention to the simulation campaigns and organize data volume and background studies.
    - Can detector contacts consider expected models for bits/hit, reasonable cuts, expected charge sharing, noise models?
  - Timing system studies
  - RDO prototype plans
  - DAM plans
  - Other plans to communicate?

# Workshop Update (Alexandre...)