LFHCal electronic proposal

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Electron-Ion Collider

Brookhaven National Laboratory · Jefferson Lab · U.S. Department of Energy Office of Science

Readout electronics requirements

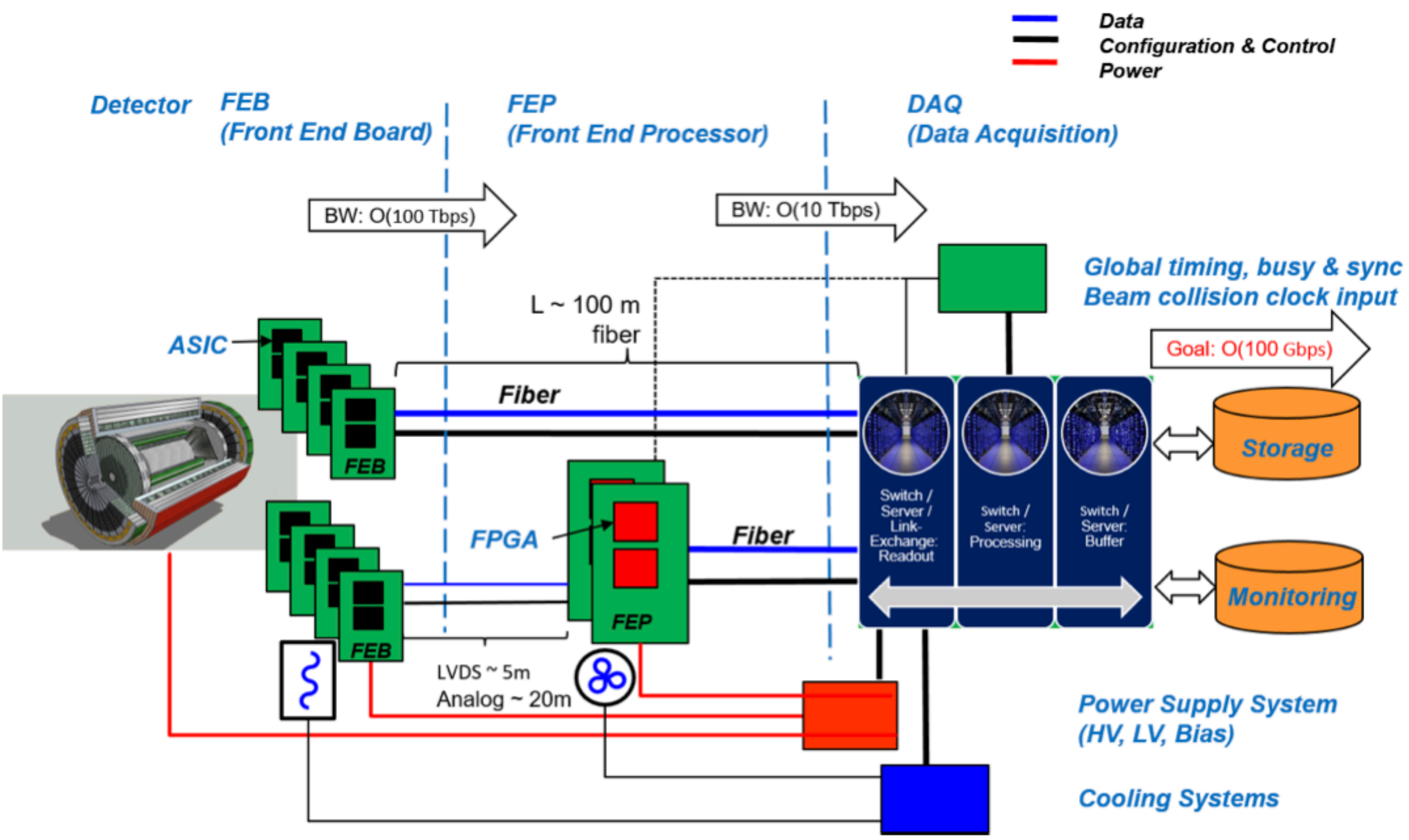


Figure 11.134: Possible scheme for the EIC Readout Architecture

EIC Yellow Report, 2103.05419

AI/ML tools can be implemented to further enhance the detector performance

Yellow report place requirements on the readout system:

- Streaming readout:
  - Calorimeters usually are not streaming (ALICE, sPHENIX)
- Online reconstruction of events:
  - Online four-vector reconstruction and PID of particles

Requirements:

- SiPM readout:
  - 60 pF to 5 nF capacitance
- Large dynamic range >= 14-bit:
  - 2.5 MeV to 100 GeV
- ASIC - signal amplification, processing, readout
  - Cost effective
  - Has to be radiation tolerant
  - Compact

H2GCROC3 architecture

Existing ASIC for CMS, ALICE detectors

Overall chip divided in two symmetrical parts:
- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

Measurements:
- Charge:
  - ADC peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution
  - TDC: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - Time of arrival, 10 bits (25ps)

Data flow:
- DAQ path:
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- Trigger path:
  - Sum of 4 or 9 channels, linearization, compression to 7bits
  - 4 x 1.28 Gbps links

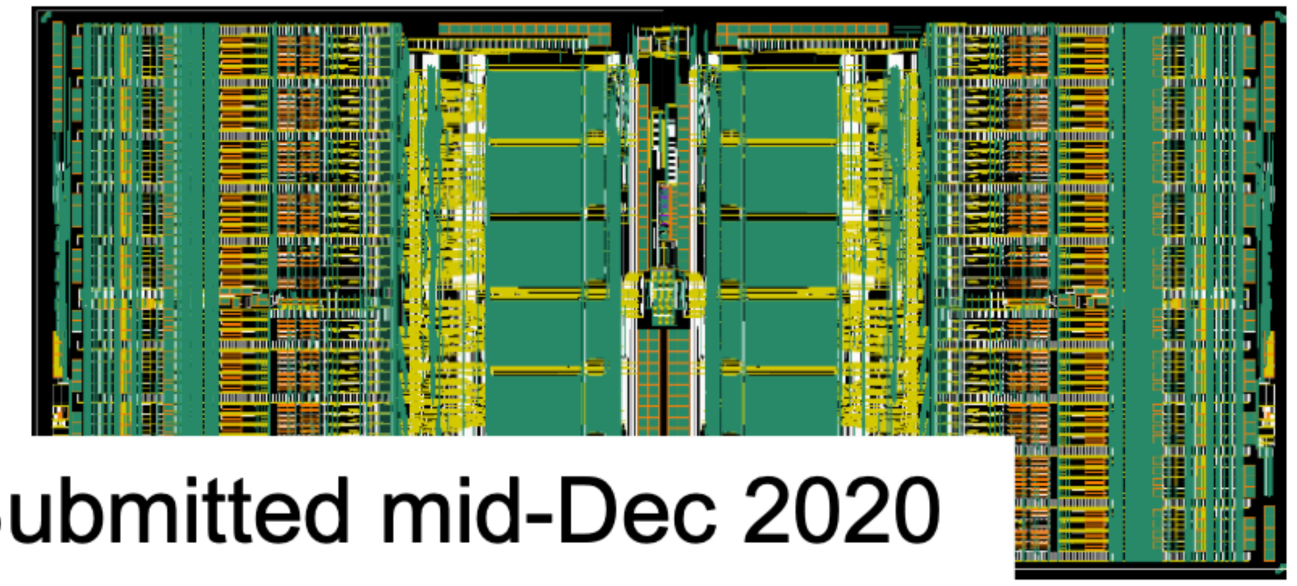
Control:
- Fast commands, 40MHz and 320MHz clock
- I2C for slow control

AGH

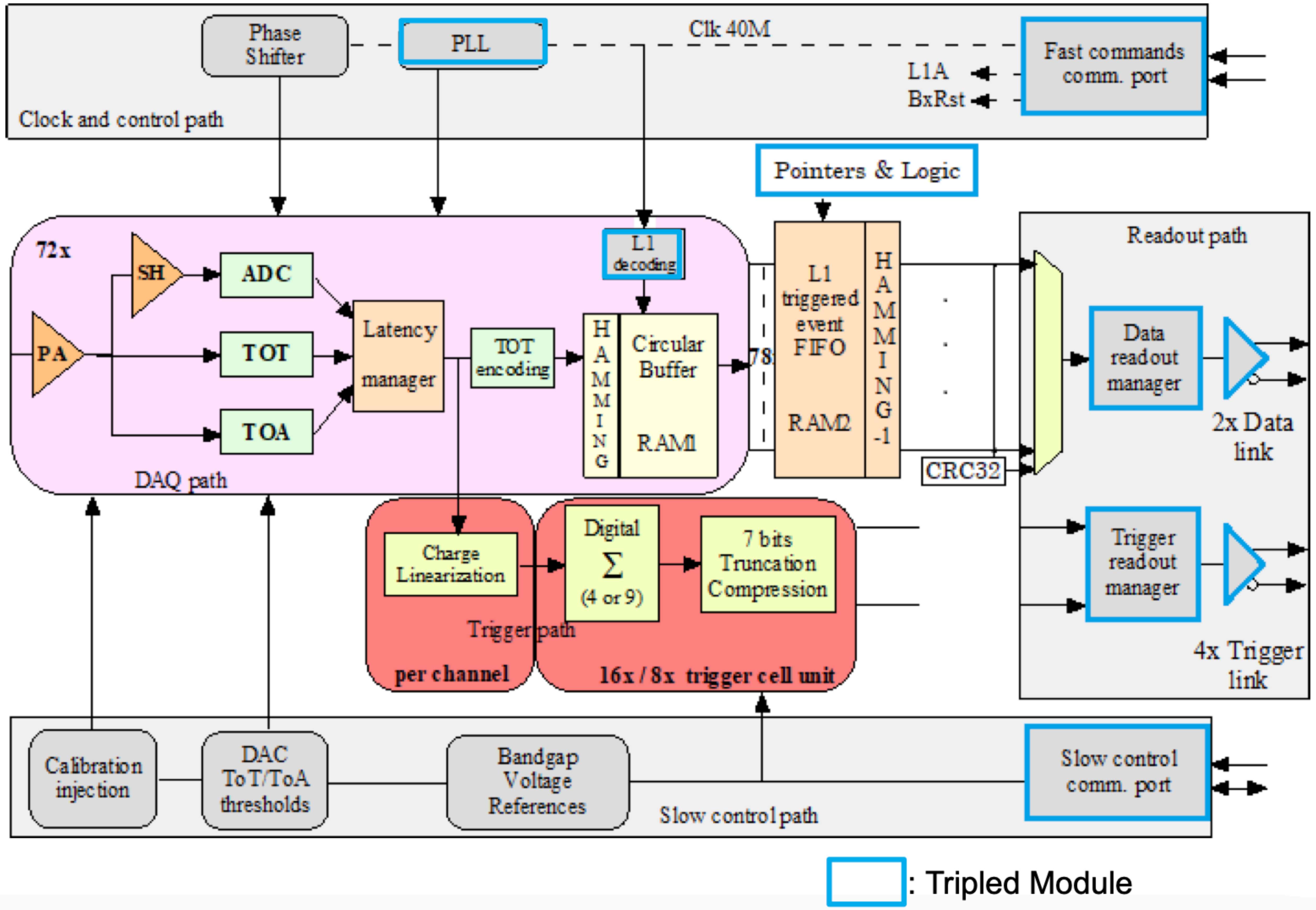
CERN

Irfu

OMEGA Microelectronics



Submitted mid-Dec 2020



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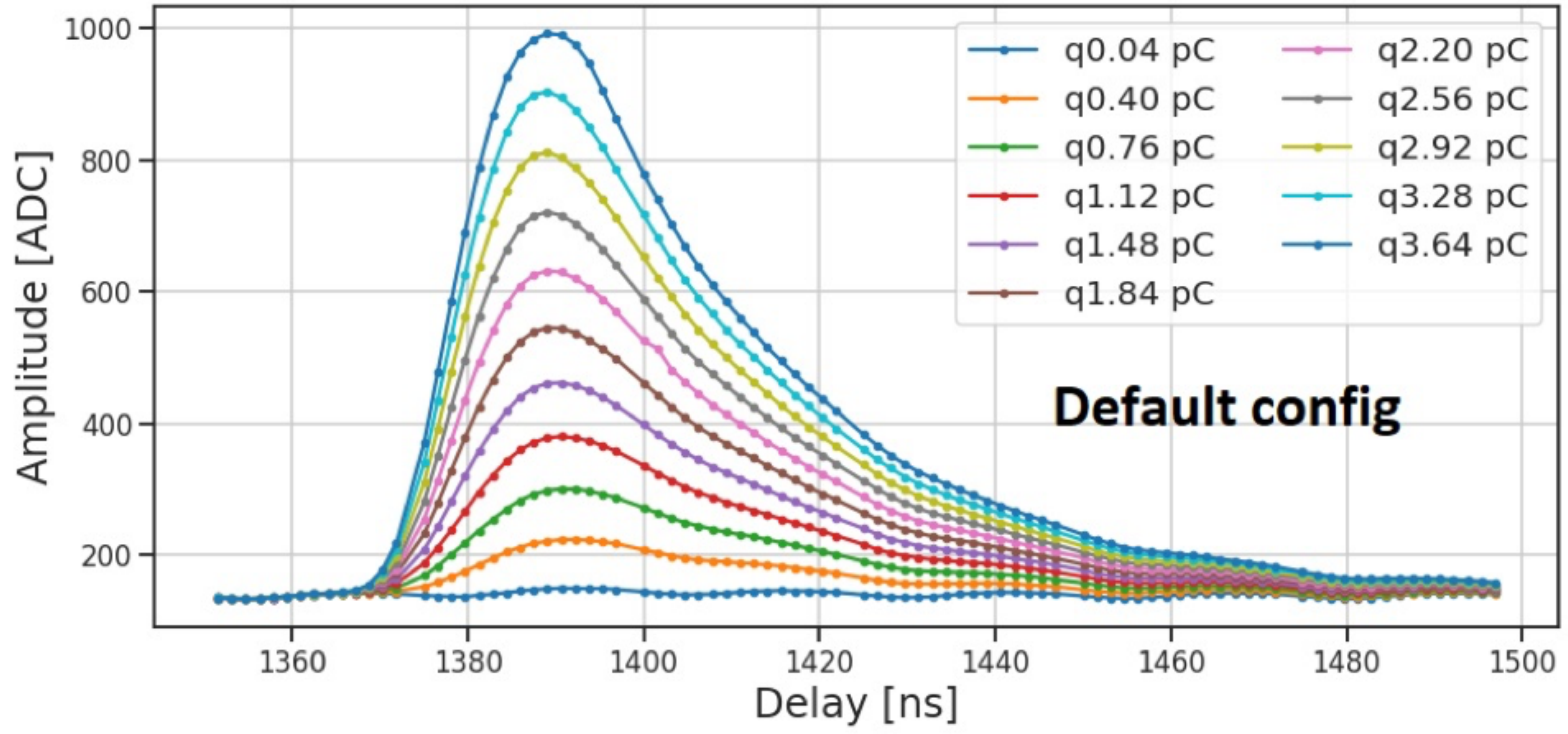
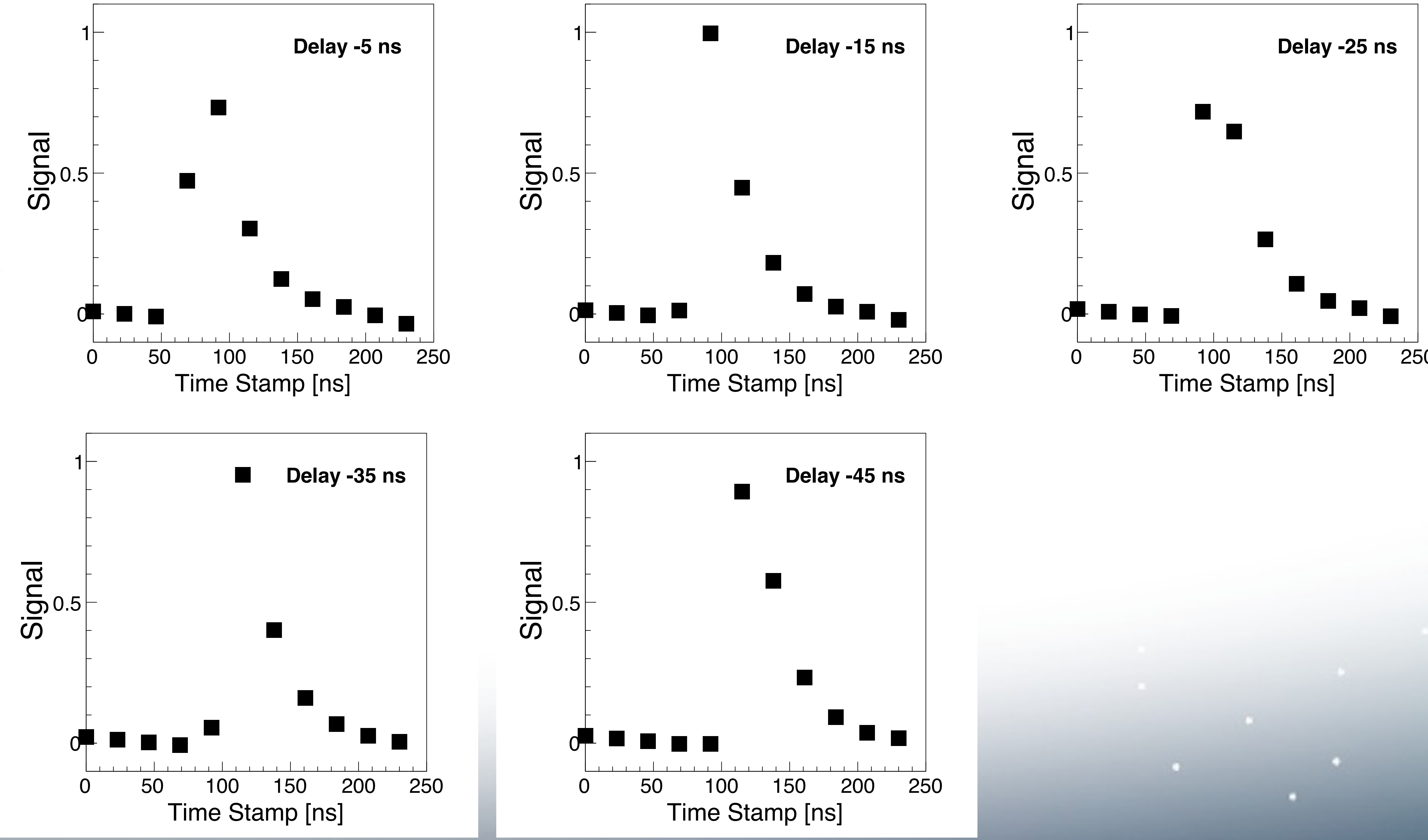
HGCROC use in EIC



Signal from the shapers:

- SiPM response of the H2GCROCv3 (from CMS)
- Default configuration used

Can it be used with the EIC 100 MHz clock?



There are 5 different phases of the signal sampled with the 40 MHz clock:

- The new version of the H2GCROCv3 can read out multiple consecutive bunch crossings
- For good signal reconstruction, we plan to save 3 (or 4) samples for each signal
- Total: 3 ADC, 3 TOA and 3 TOT values, 32bitx3 words for each physics signal

We can reconstruct the phases (using TOA) and the shower shape (ADC+TOT template fit) for the EIC 100 MHz clock

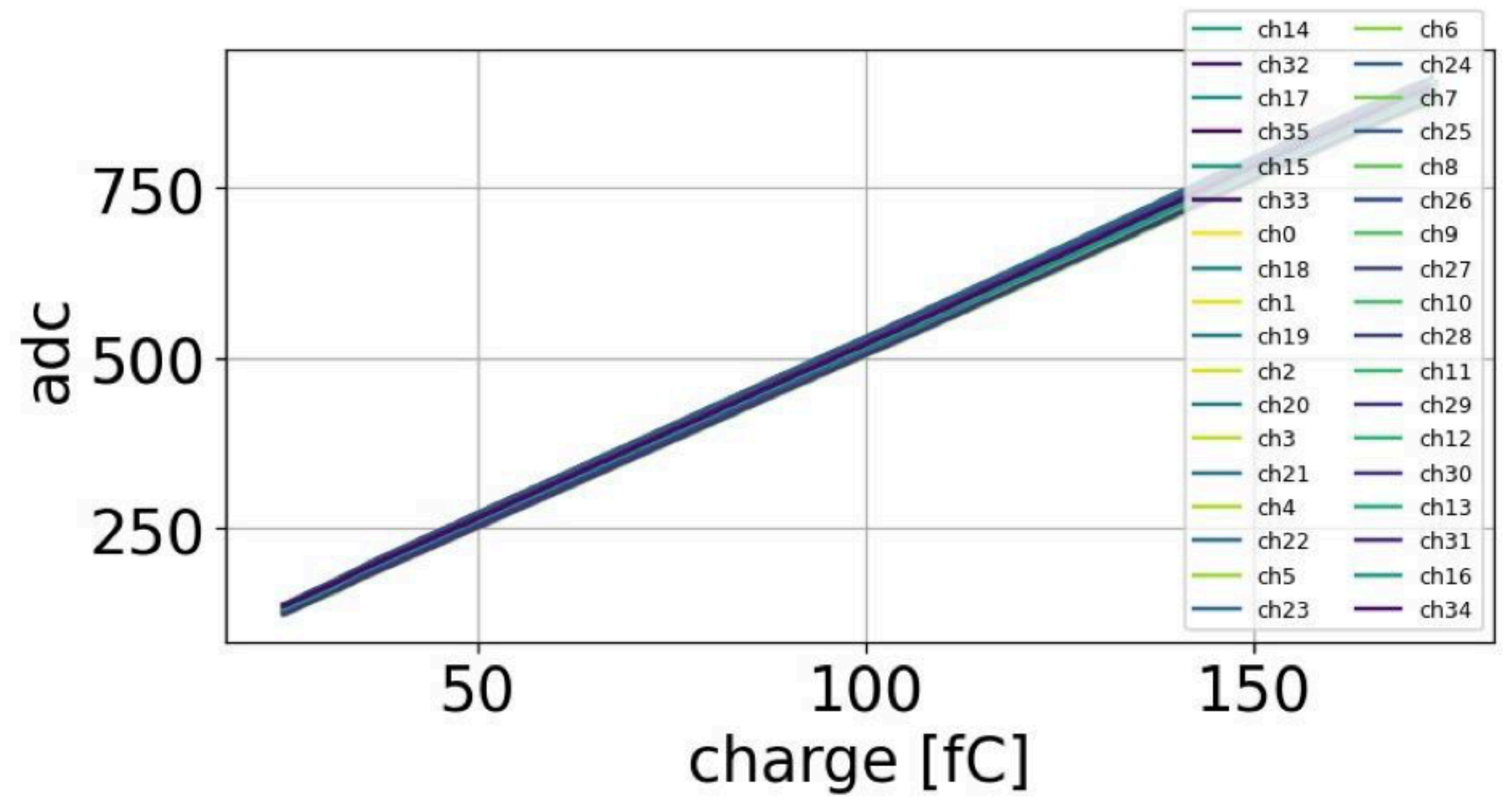
ADC data and noise

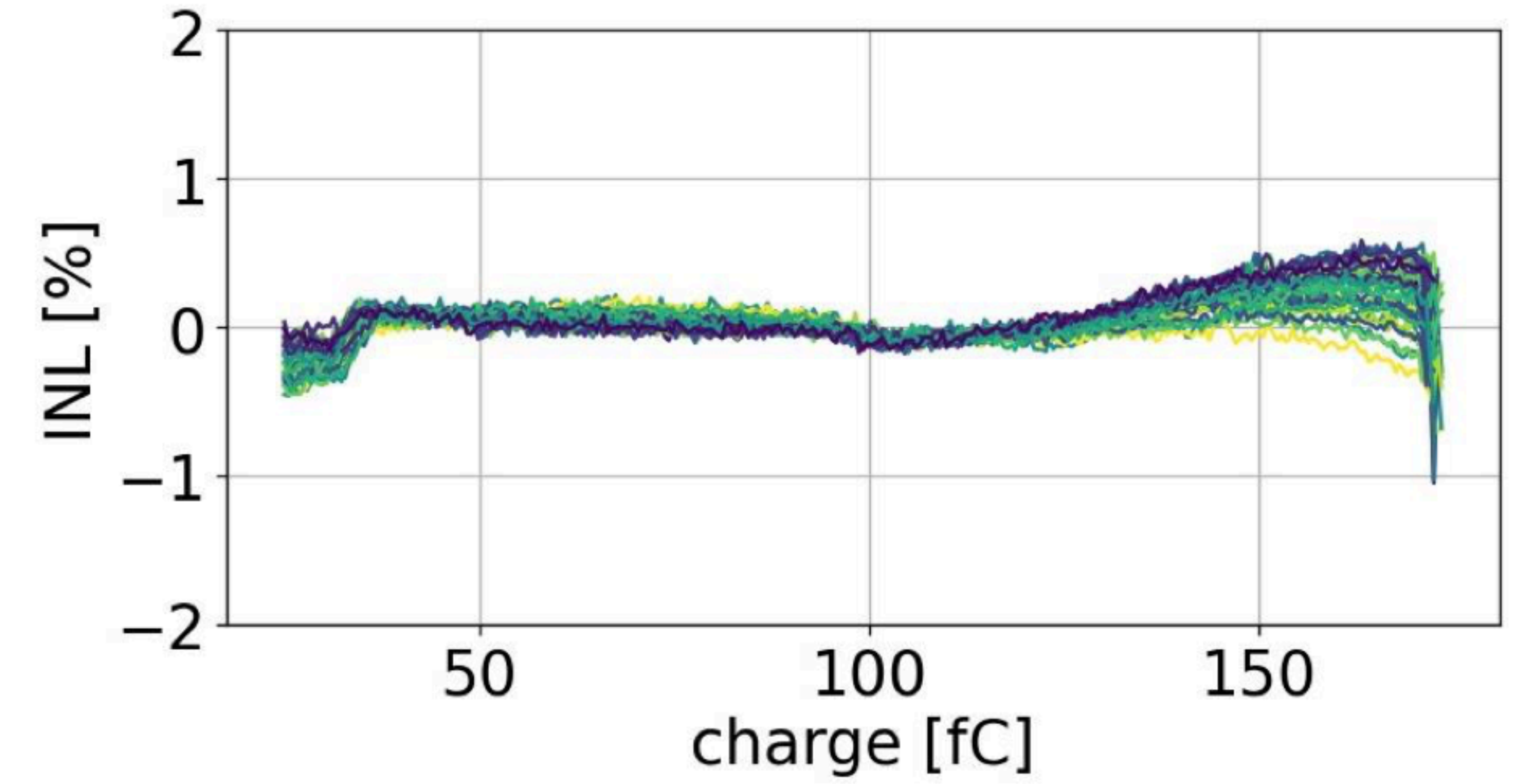
Two 10-bit DAC to globally set the pedestal to desired level (minimum)
5-bit reduce the dispersion from individual channels

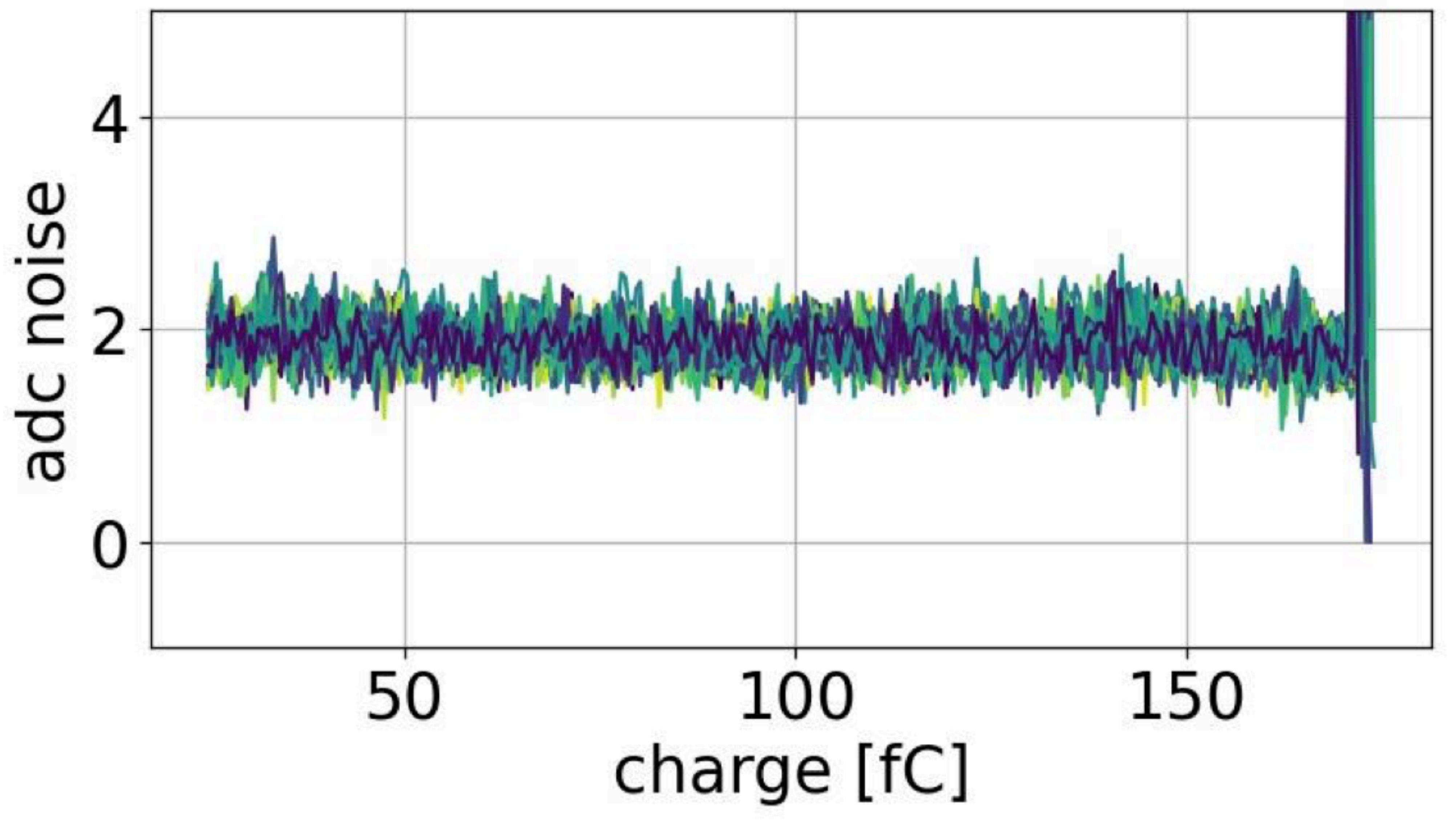
Very good linearity < 1%

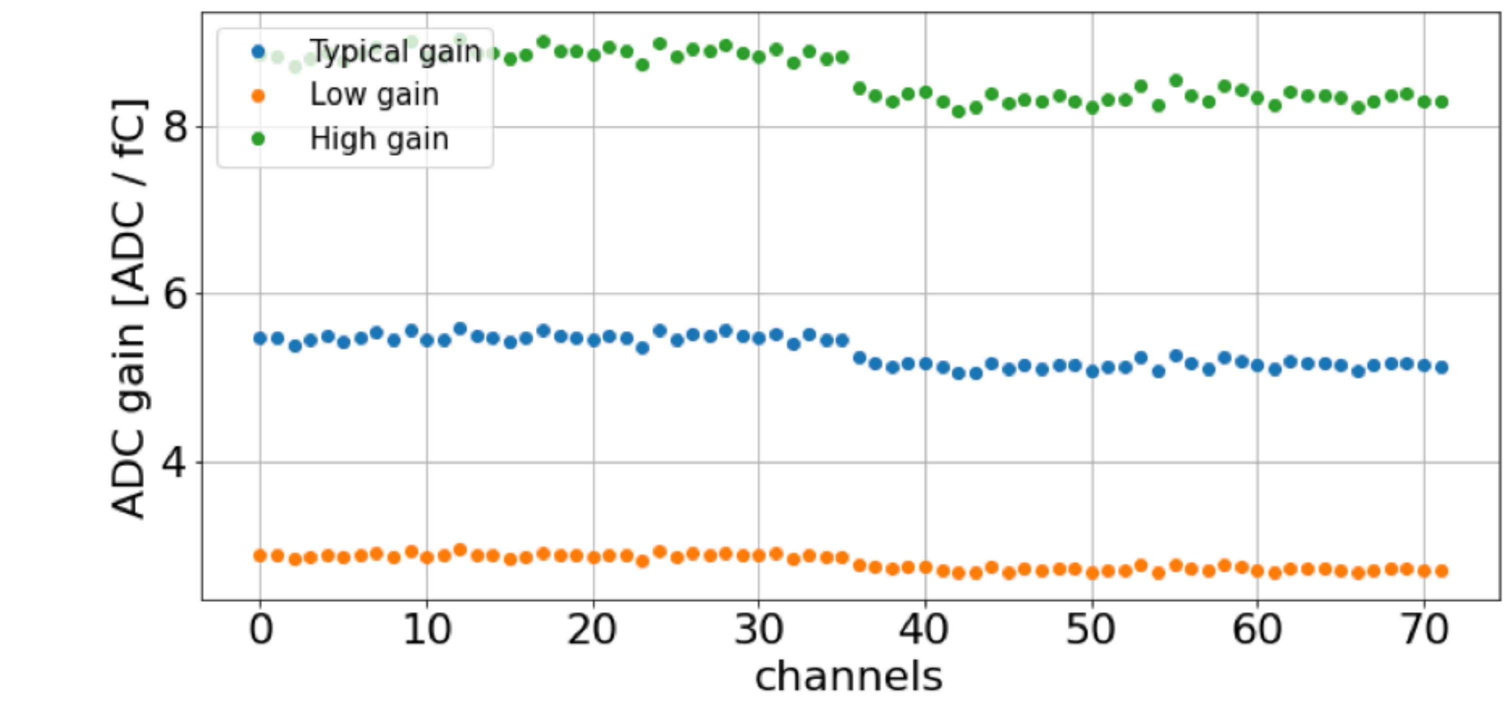
- 1.6 fC linearity (~1 MIP) for the typical gain

0.3 fC resolution on 50 pF input capacitor







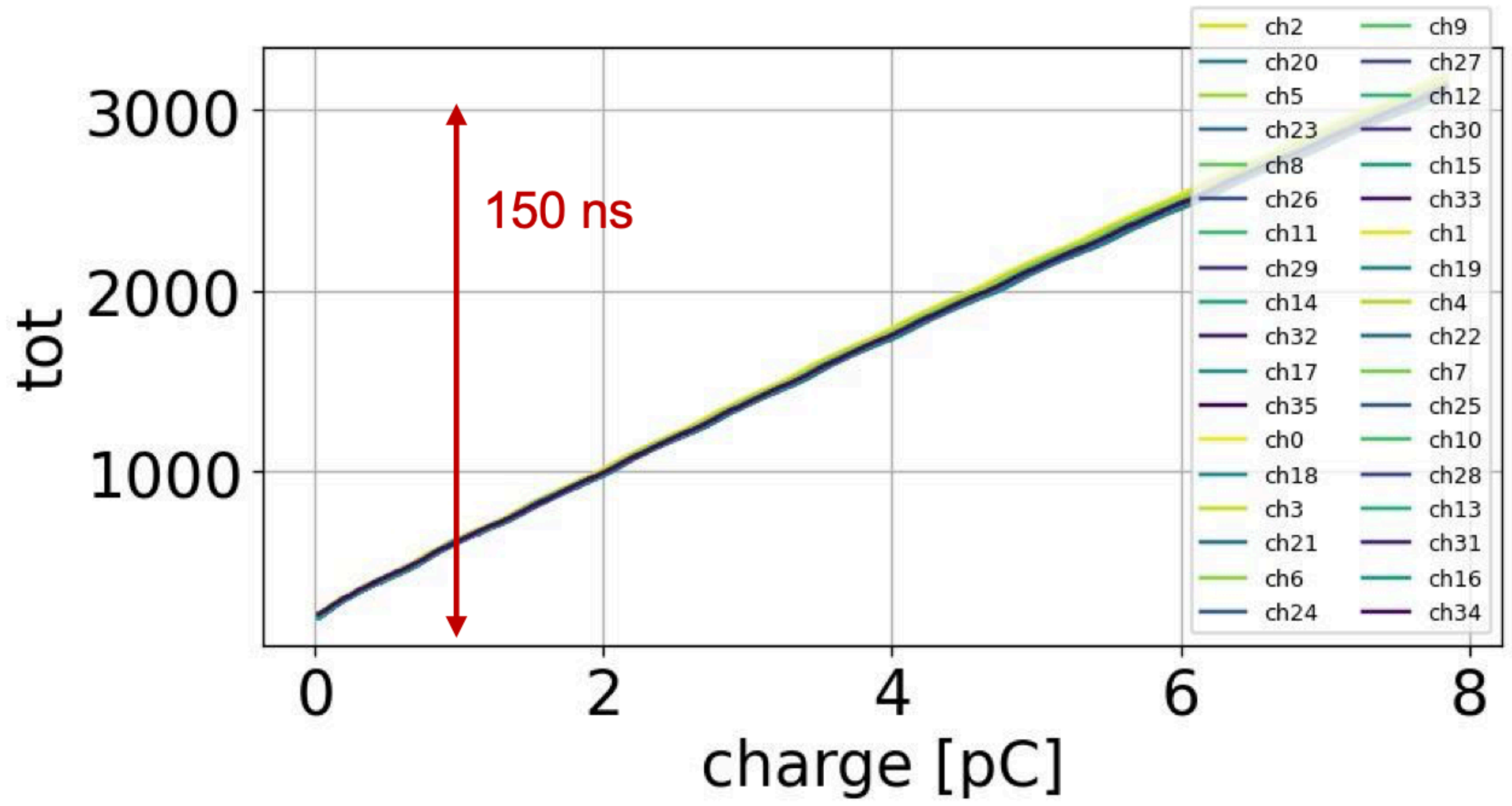


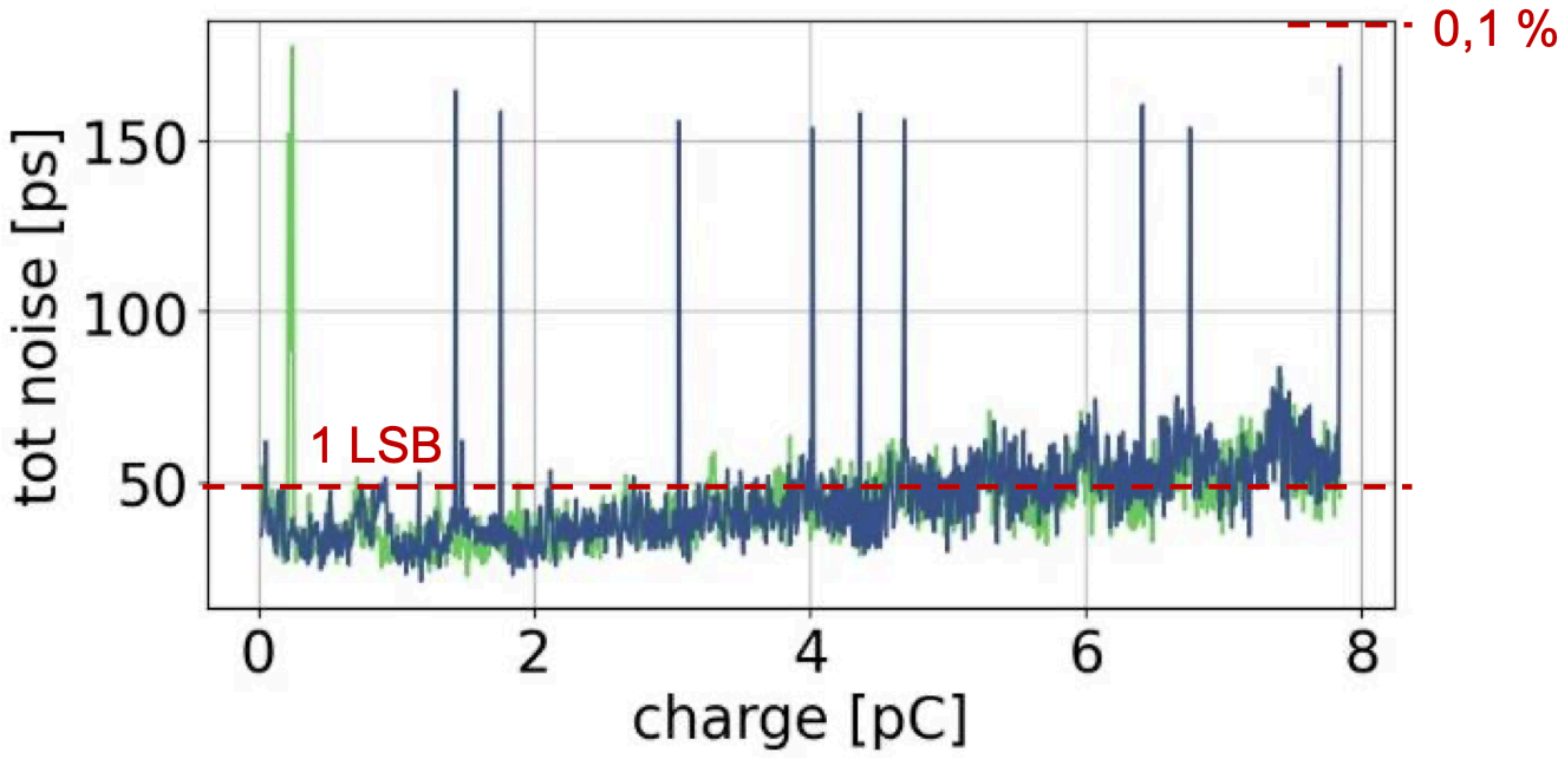
TOT range

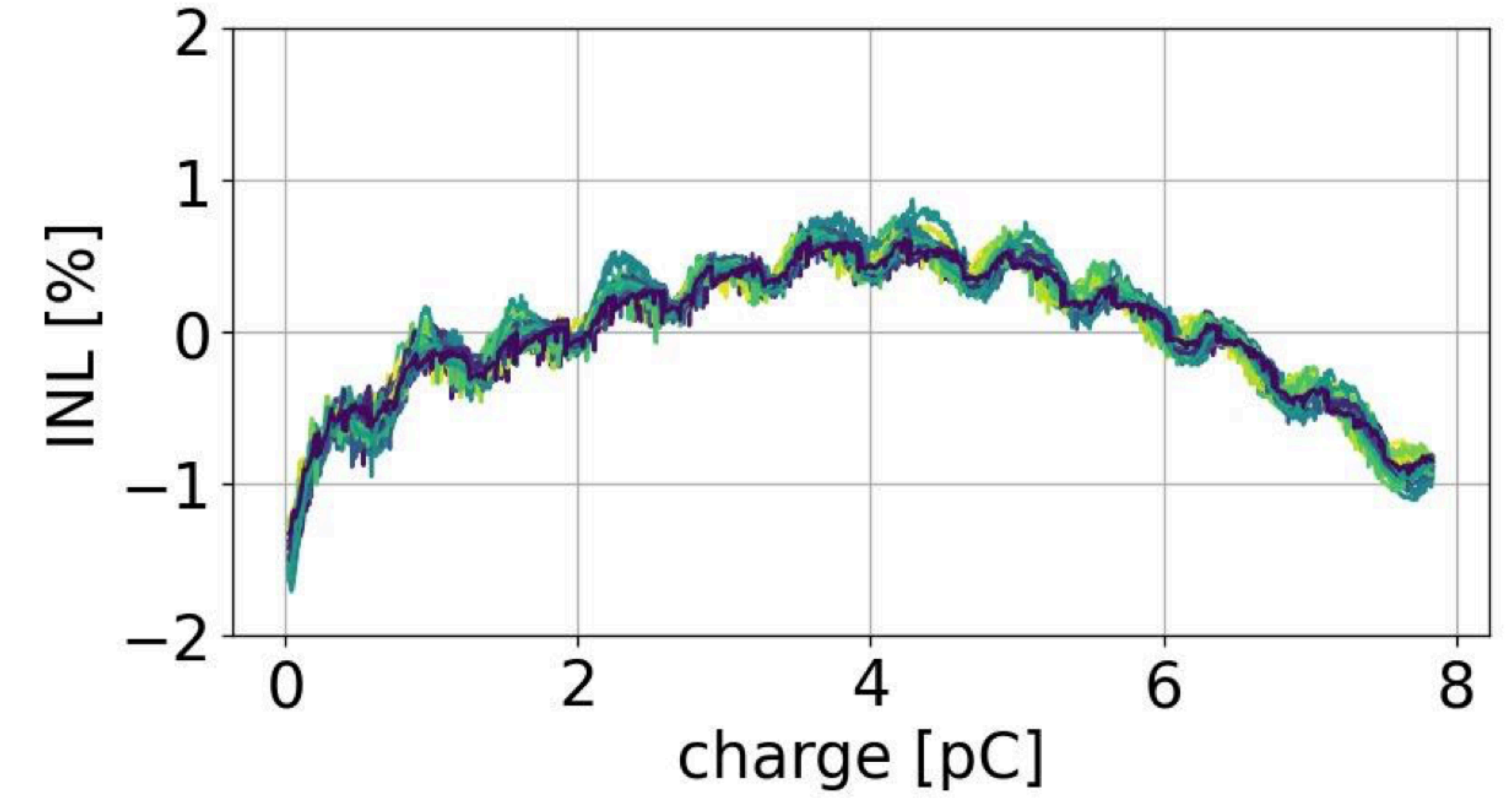
Once the ADC is saturated, the TOT takes over:
Range in silicon is 160 fC to 10pC, in SiPM 16pC to 320pC
50 ps binning

Very good linearity in the ToT:

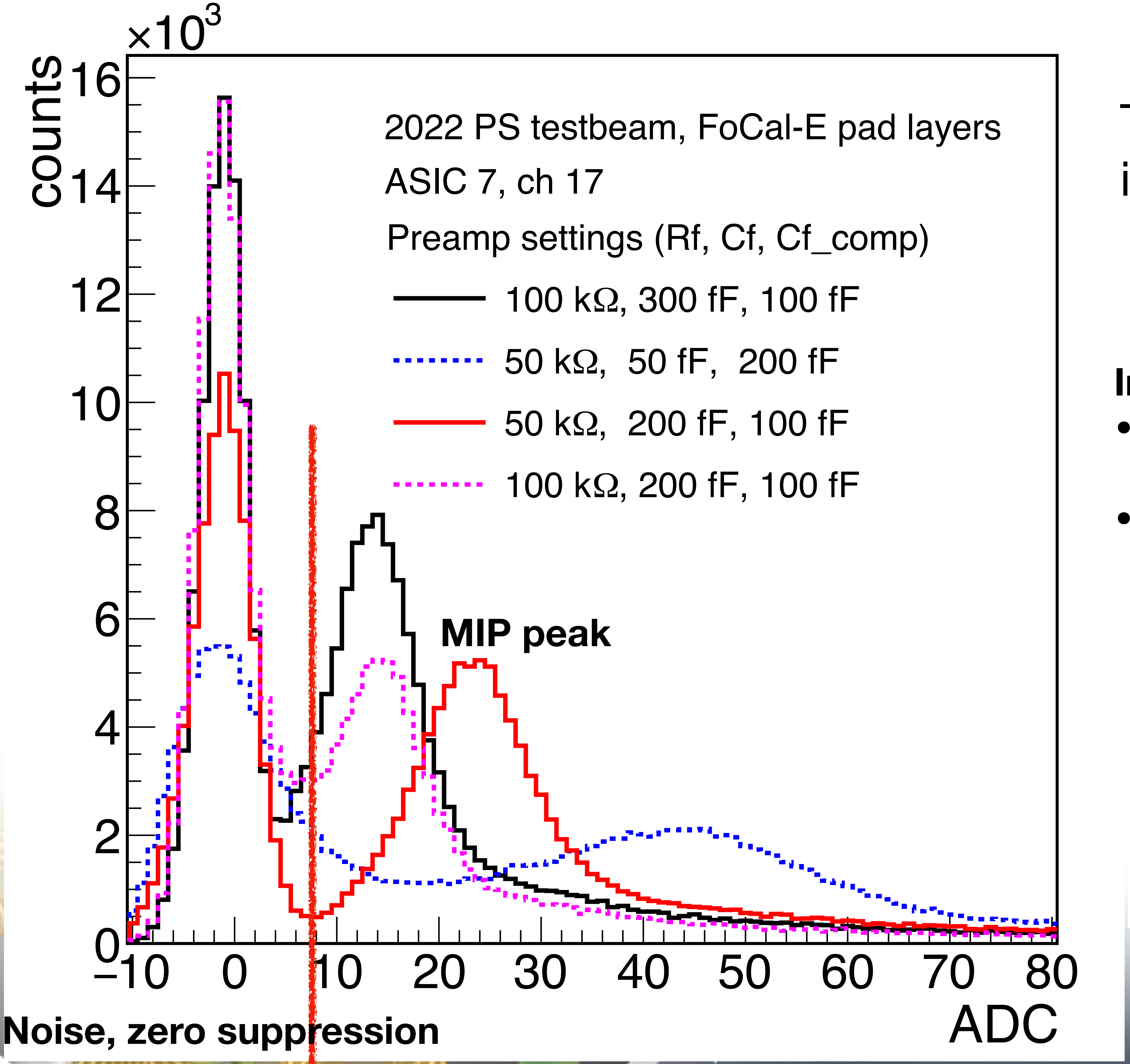
- 99.9% up to 200pC, 99% in full range
- Small residual wriggles on TOT from the digital noise on preamplifier input
- Resolution is about 50ps (the peaks are outliers which were fixed)







Calibration of the detector



The data is obtained with the HGCROCv2 in PS 2022 June with silicon sensor

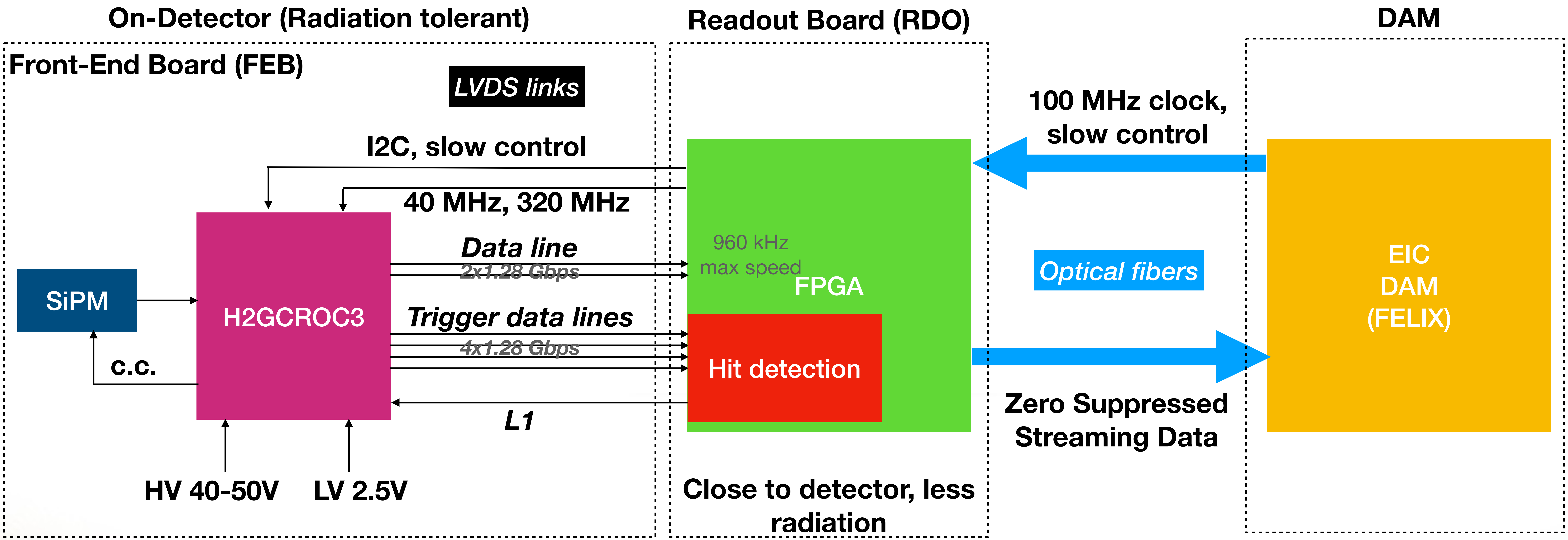
In addition, the H2GCROCv3 contains:

- 6-bit current conveyor to adjust the SiPM bias voltage:
  - Adjust the voltage for individual channels
- Different preamp settings

Cd (pF)	5, 10, 20	At the conveyor output and at the preamp input. To ensure the preamp stability.
Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50, 100, 200, 400	Same purpose than Cf capacitors but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table 1.1: Values for Rf, Cf and Cd

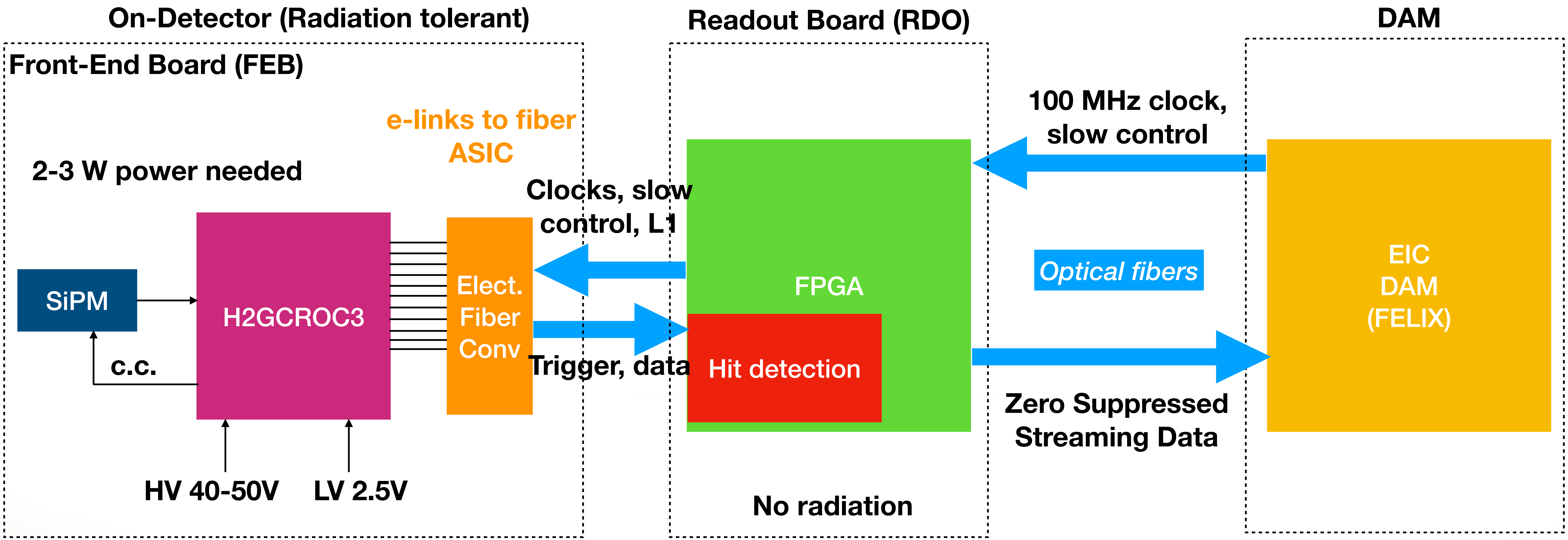
LFHCal readout hierarchy



Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

LFHCal readout hierarchy - Service reduction



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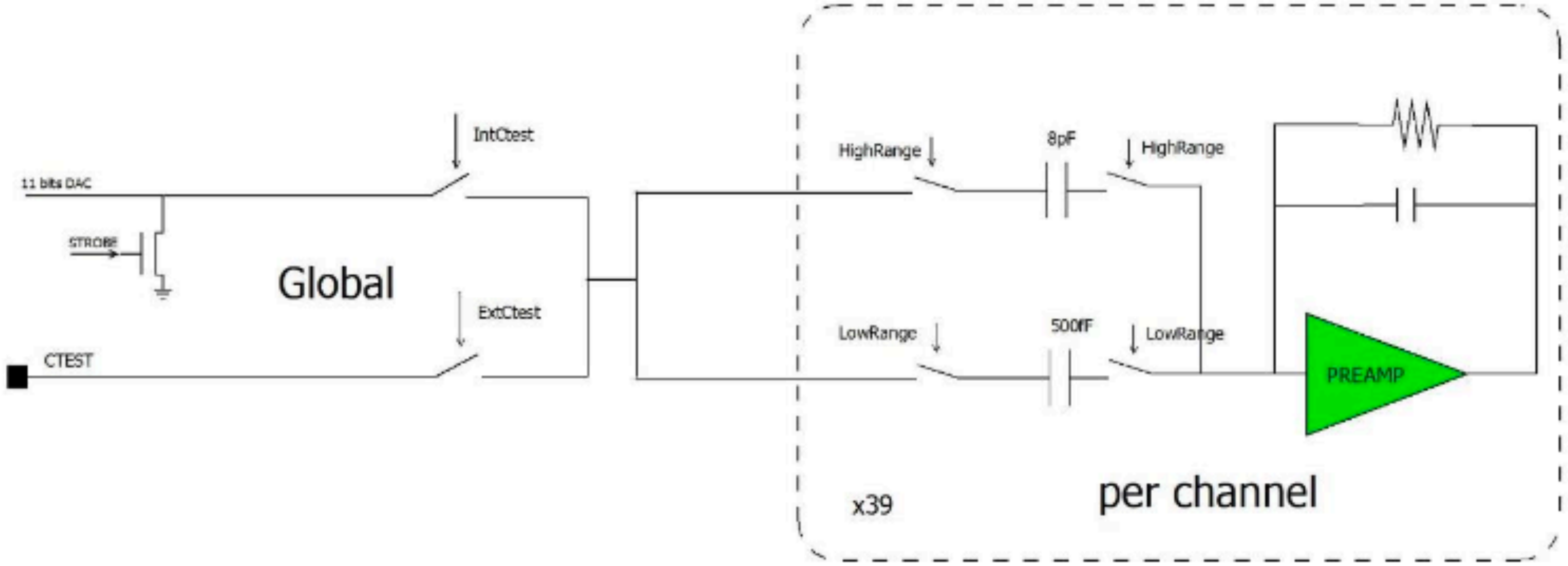
Service reduction for H2GCROC3 would allow significant simplification on the cabling

Internal Calibration Circuit



Internal Calibration circuit implemented in the H2GCROCv3:

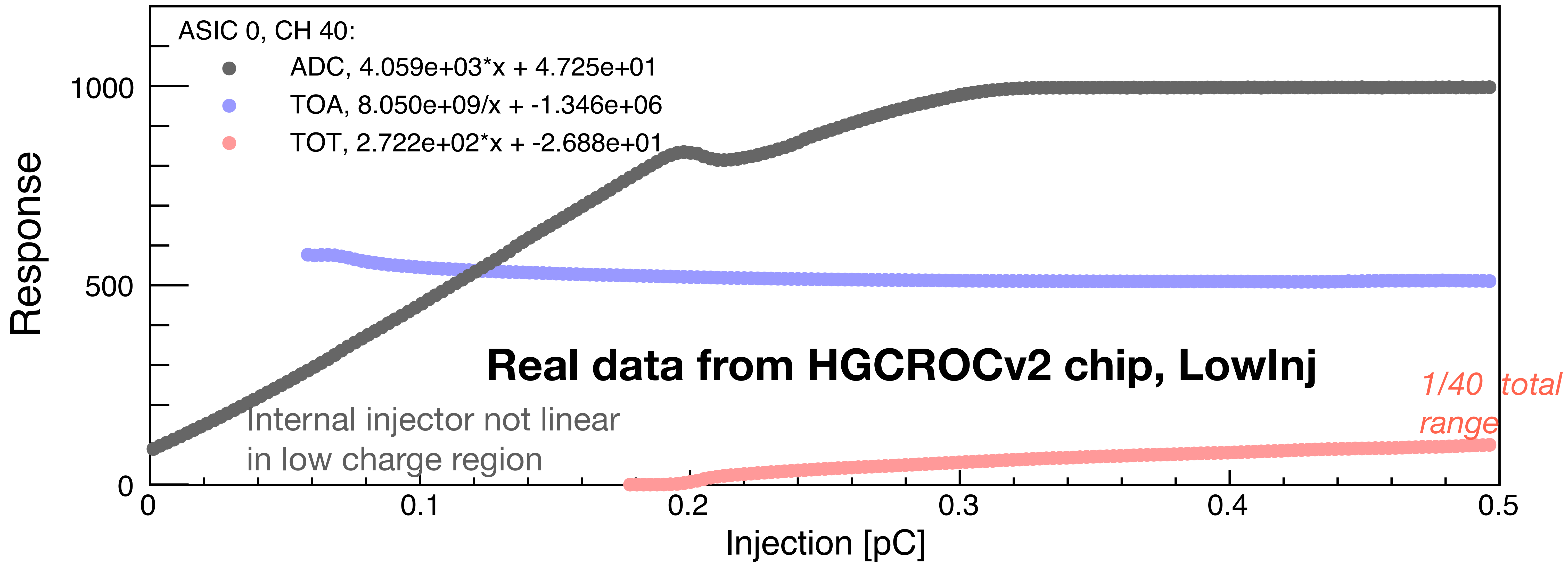
- Almost the full dynamic range. Reference voltage 0-1V:
  - 0.5 pF Low Range: 0 - 0.5 pC
  - 8 pF High Range: 0- 8 pC

Calibration circuit injection value of 11-bit:
Can be used to identify the thresholds for TOA and TOT, check linearity, etc.

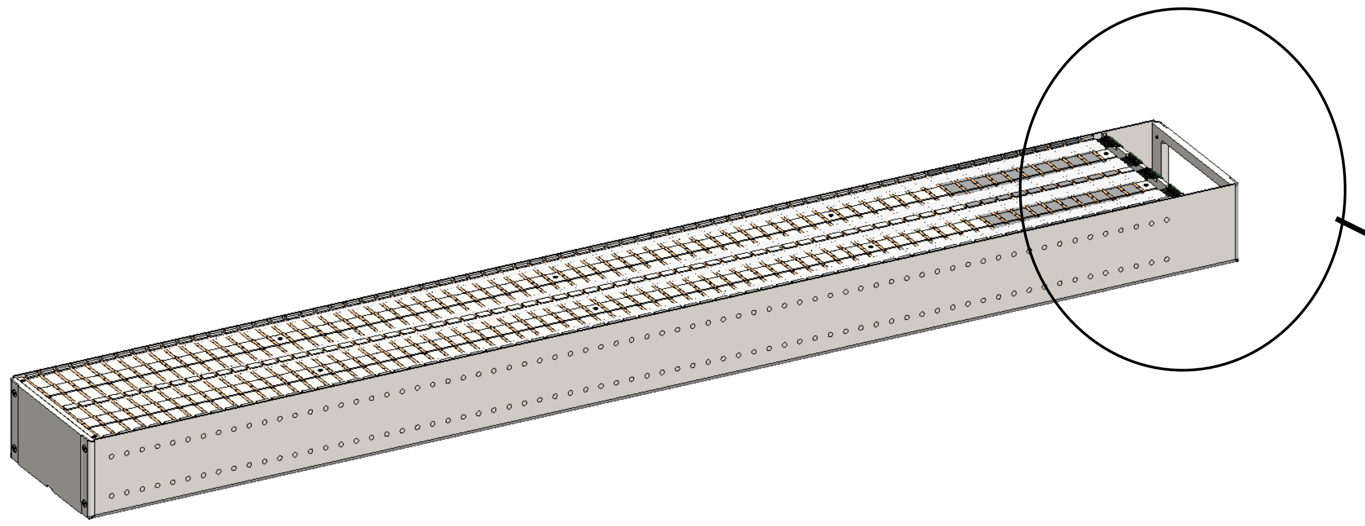
Dynamic range of the HGCROC:

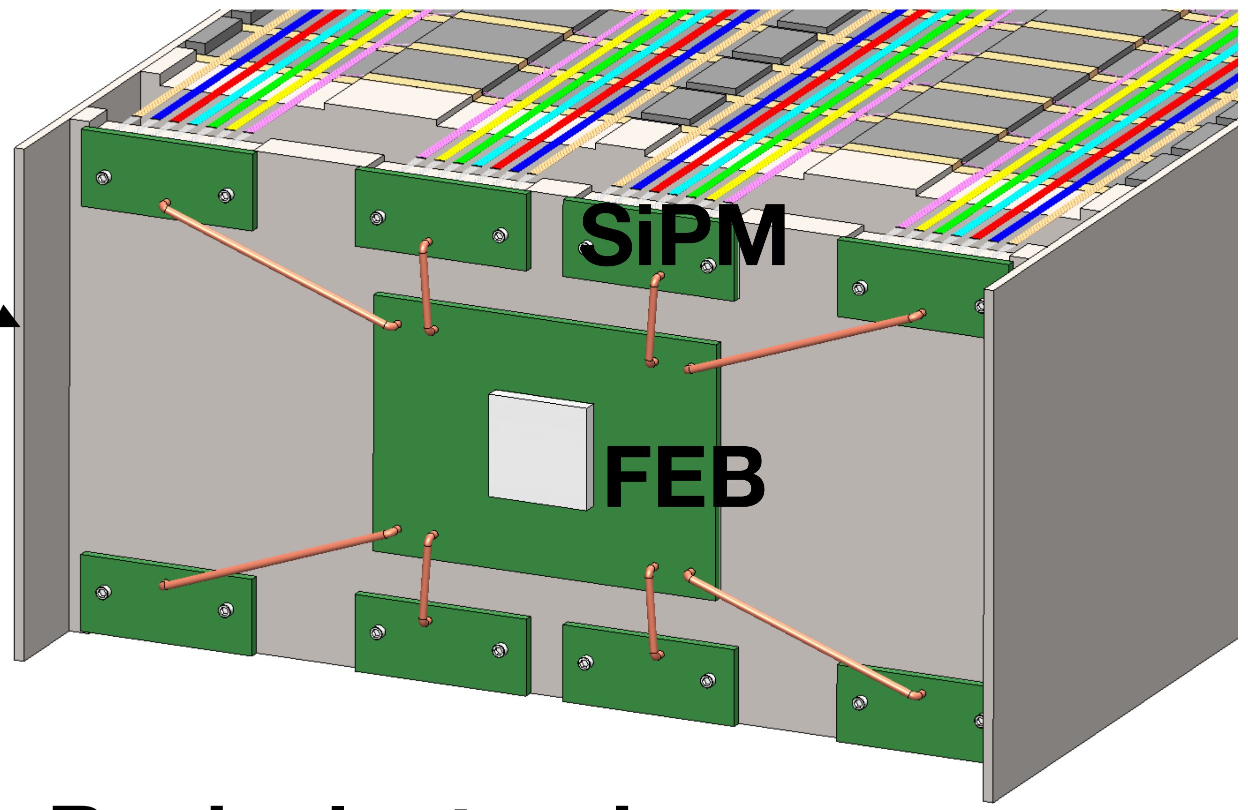
- Real data from the v2 chip
- Silicon variant
- ADC set to saturate around 850:
  - Small dip in the ADC happens when the TOT circuit comes online
  - TOT values are shown only to 100 (out of the 4095 range)
  - TOA have a small walk from threshold to 0.18 fC, then it is stable

We are currently working on the same data for the H2GCROCv3 chip



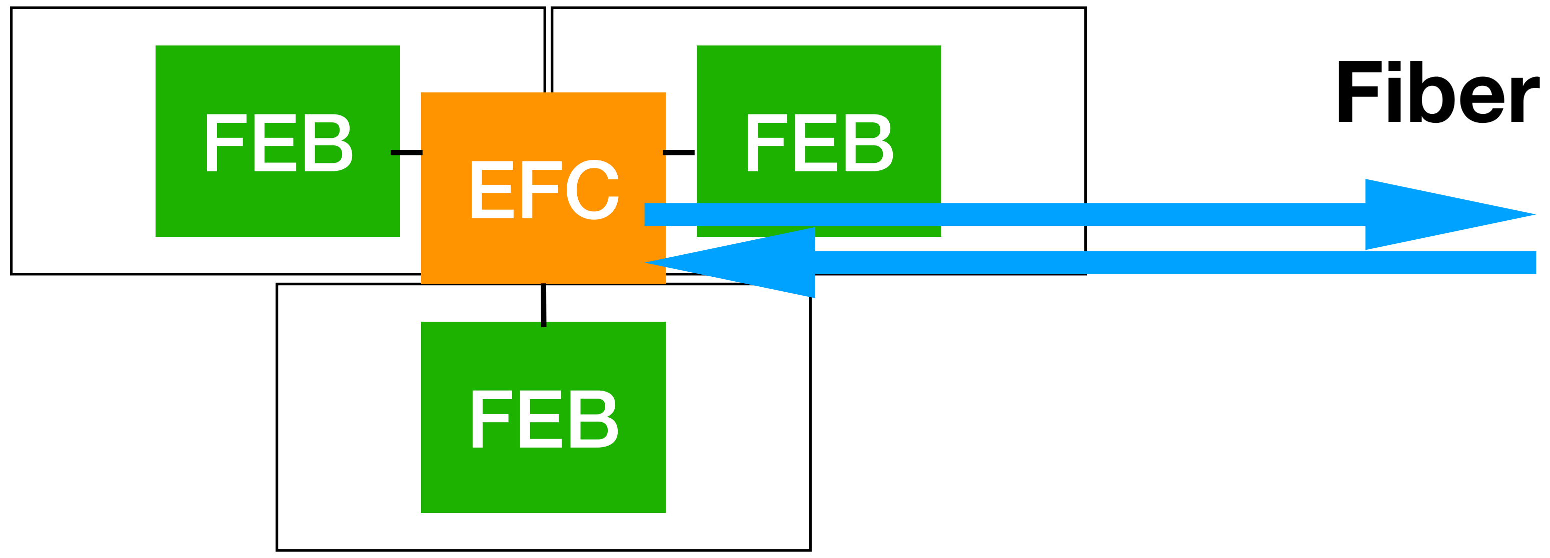
Placement, mechanics



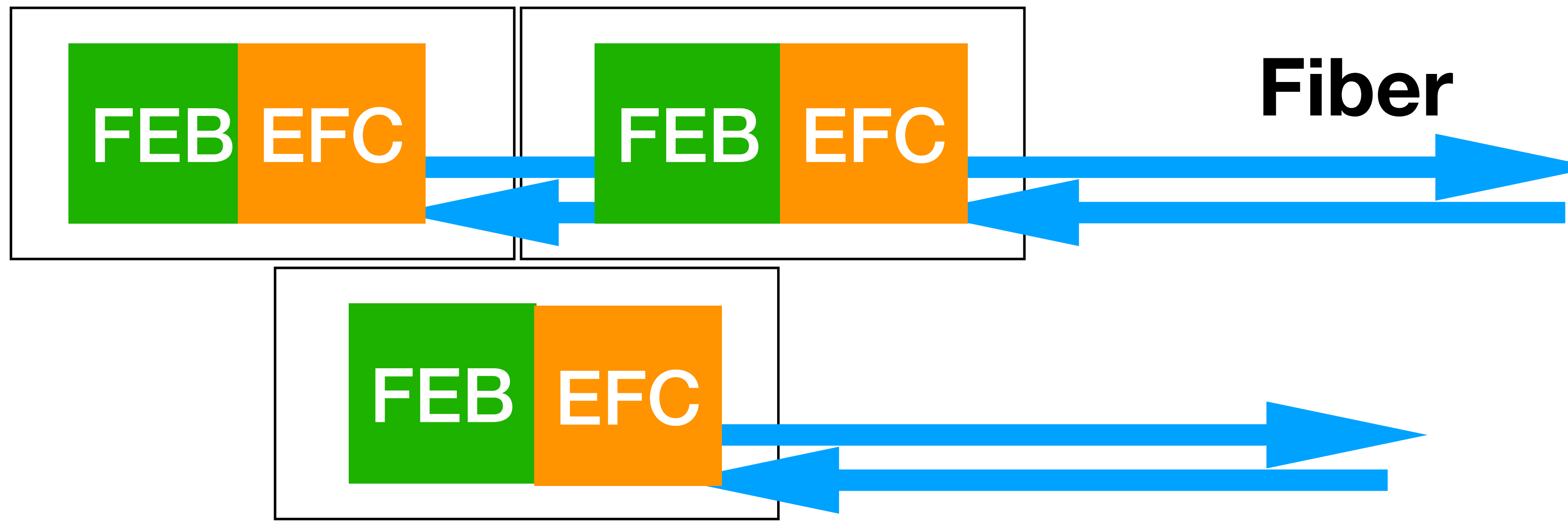


Back electronics

Option A - multiple FEB served with FC

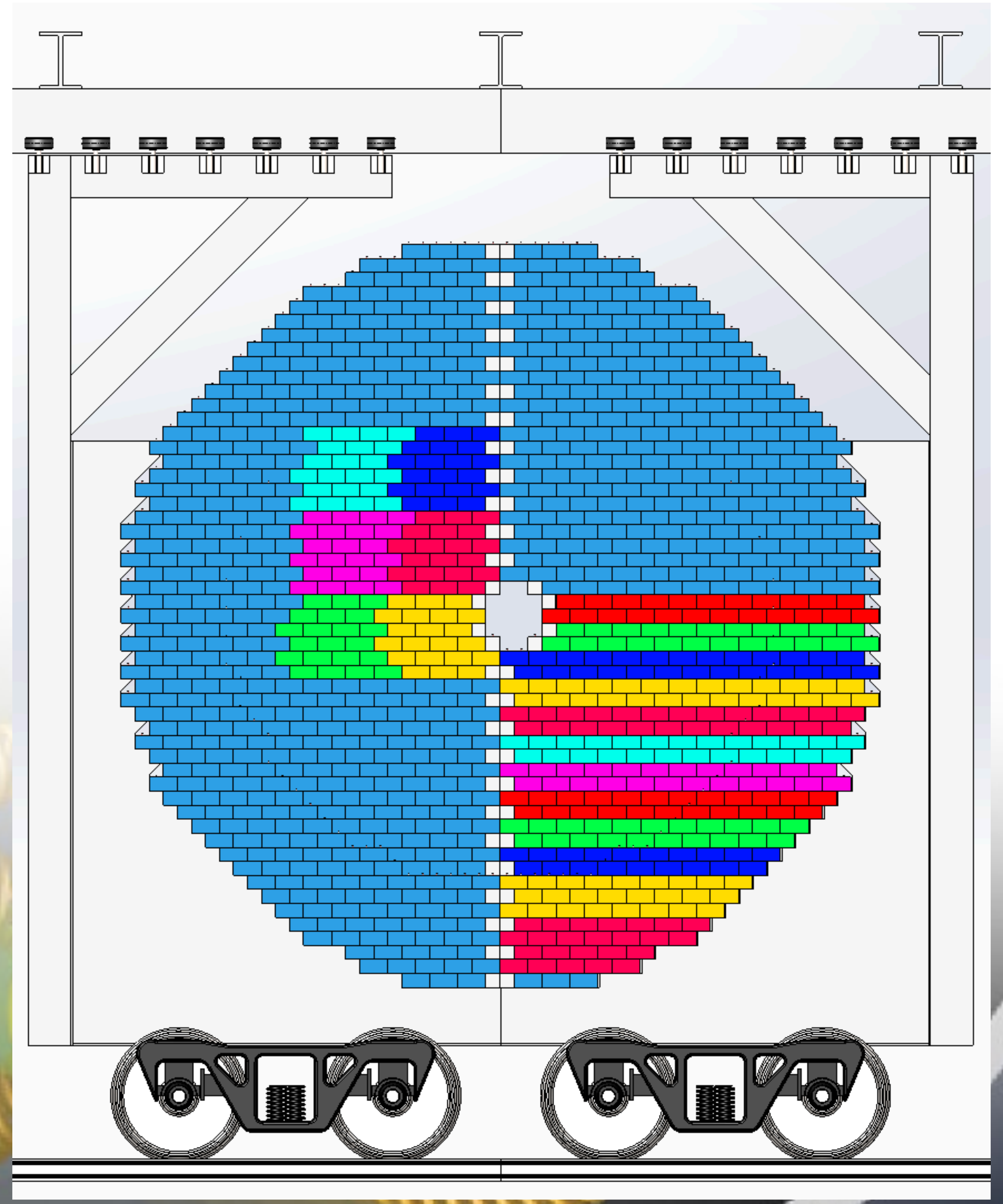


Option B - one FEB + FC board



Placement of the Readout Board (RDO)

Option A: Spider-design



Option B: Snake-design

Option C: (with EFC only) FPGA in rack off detector

Very compact design
Radiation tolerant
Low power (2W/ASIC)
Cost effective

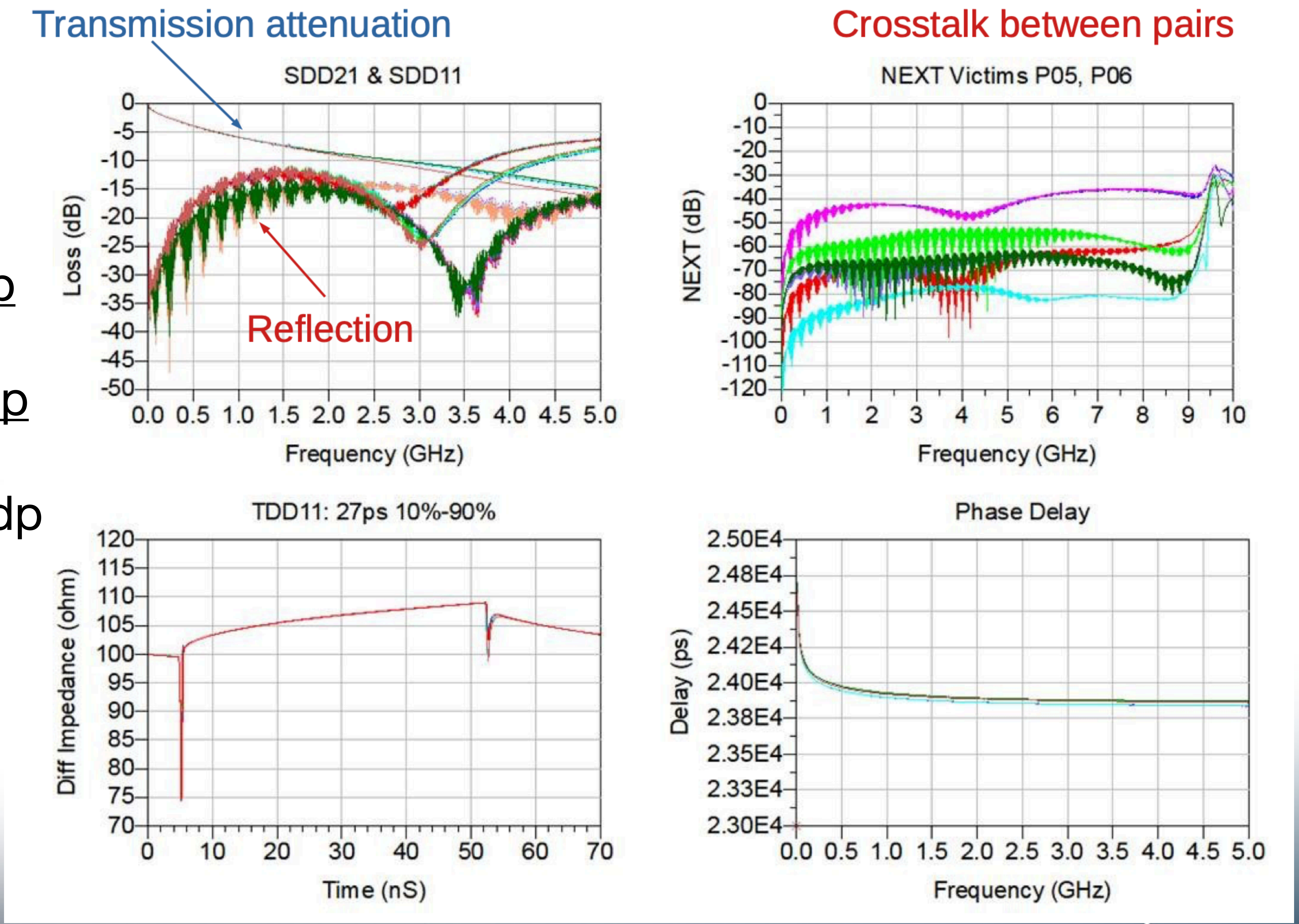
Cable options for the LVDS links

Twinax cables look ok

A. https://www.samtec.com/products/erdp
- ERF8 and ERM8 connectors

B. https://www.samtec.com/products/eqdp
- QTE-DP and QSE-DP connectors

C. https://www.samtec.com/produc ts/hqdp
- QTH-DP and QSH-DP connectors



Planned R&D needed to extend to more detectors

The list of calorimeters in EPIC:

- **LFHCAL - 64k**
- **FEMC - 19k**
- **Barrel EMCal:**
  - **SciGlass - 9k**
  - **Imaging calorimeter - 4k for SiPM**
- **Barrel HCal - 1.5 k or 7.7 k**
- **EEEMC - 3k**
- **Backward HCal - 16k**

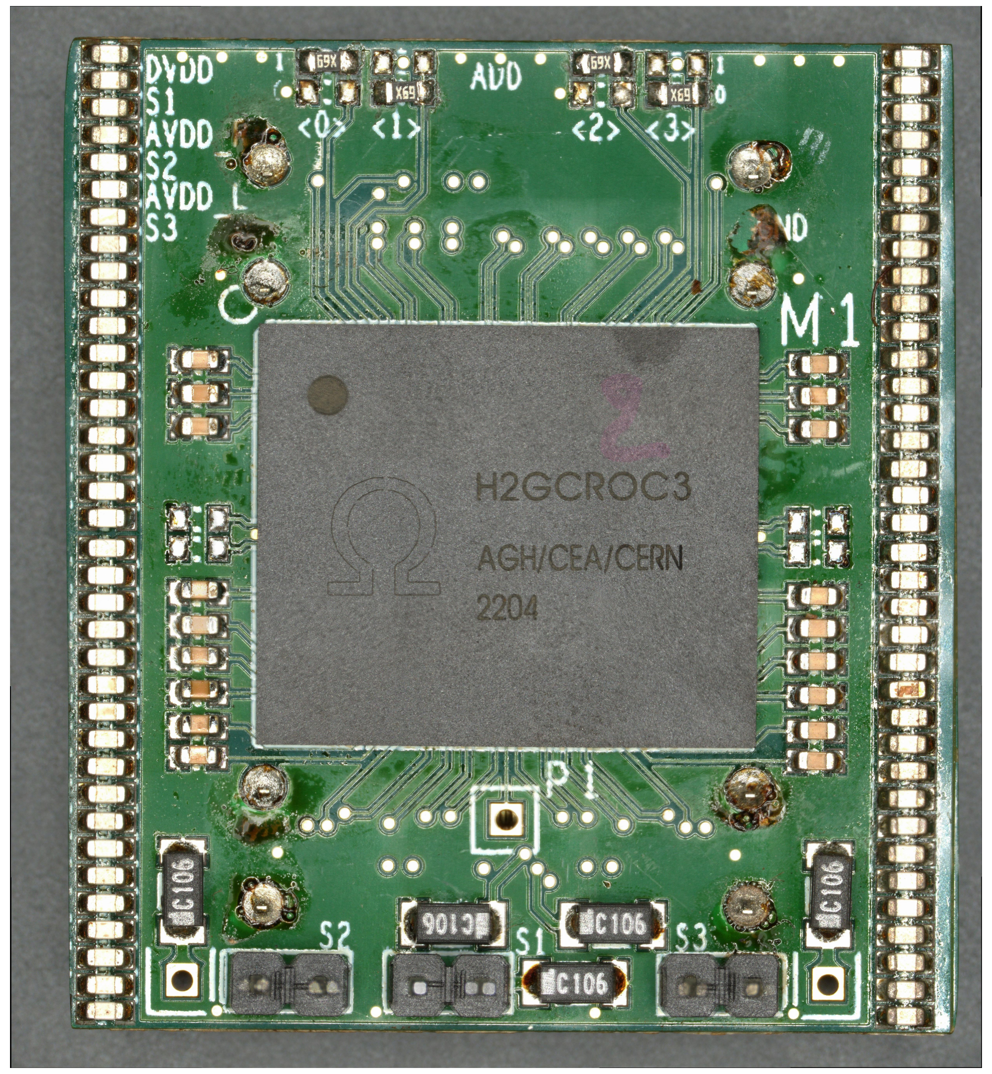
Why would we want to use this ASIC?

- Large radiation tolerance (for years)
- 20 euro/chip (need 1100 of them for LFHCal)
- Low power consumption (20mW/channel, 2kW for LFHCAL)

Which detectors need a preamplifier on FEB?

H2GCROC3 R&D:

- First data is almost ready to present (ongoing)
- First test beam planned in March-April with PS/SPS at CERN with SiPM
- Investigation of multiple SiPM inputs (4x4 array planned to use in SciGlass)



One ASIC over all Epic calorimeters

Chip on testboard at ORNL. Started working on it at ORNL

Paris-Omega team offered further development of the chip if we need

Summary

Multiple experiments plan to use the ASIC:
- HGCAL at CMS
- FoCal at ALICE (ORNL is involved in this project)

The ASIC already exists and @ ORNL

Initial investigation shows the H2GCROC3 would be capable at EIC (without modification):
- Signal shape can be sampled at 40 MHz
  - 3-4 samples are enough
  - 5 possible phases
- Consistent with streaming readout requirement
- Proposed architecture on the readout scheme

H2GCROC3 provides:
- For all SiPM readout
- 22-bit dynamic range (10 ADC, 12 TOT):
  - Different gain setups to accommodate wide range of sensitivities
- Internal calibration circuit
- Providing timing information
  - TOA could help in timing of the calorimeters - primary identify
  - Need further study for track matching, combining with timing detectors

Test in 2023

Yellow report place requirements on the readout system:
- Streaming readout:
  - Calorimeters usually are not streaming (ALICE, sPHENIX)
- Online reconstruction of events:
  - Online four-vector reconstruction and PID of particles

Requirements:
- SiPM readout:
  - 60 pF to 5 nF capacitance
- Large dynamic range >= 14-bit:
  - 2.5 MeV to 100 GeV
- ASIC - signal amplification, processing and readout
- Readout 50 kHz

Backup

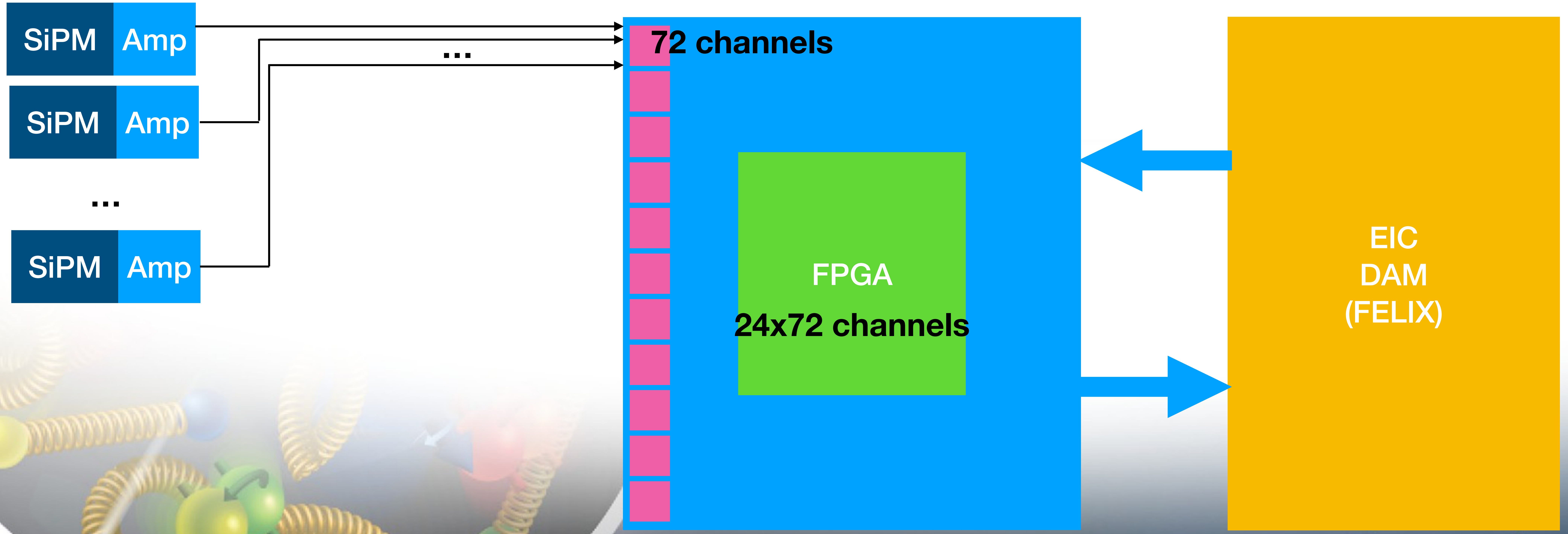
A lot of additional documents can be found:
https://cernbox.cern.ch/s/IQTGIljPwnQyjQx

Implementation for other detectors

On-detector SiPM + ASIC + FC already discussed:
- FEB is RadHard, can be adopted to all calorimeter readout

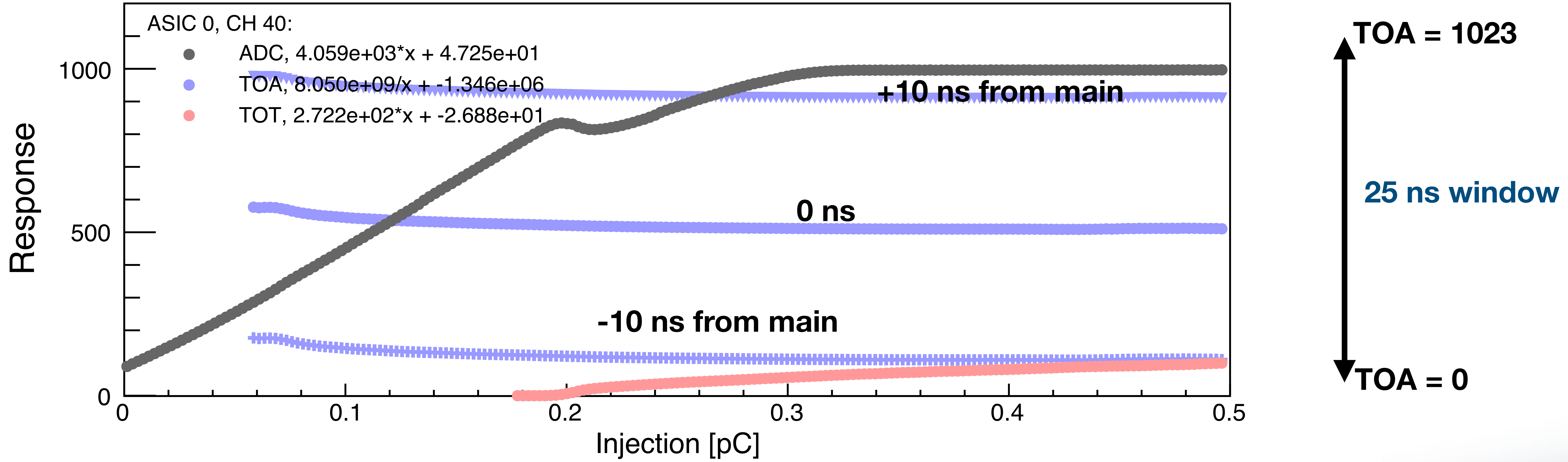
Off-detector readout electronics:
- Only SiPM on the detector
- An amplifier is needed on the detector (R&D is needed)
- FEB+RDU is combined off the detector

For detectors avoiding ASICs on the FEB (Heating, cabling or other consideration)



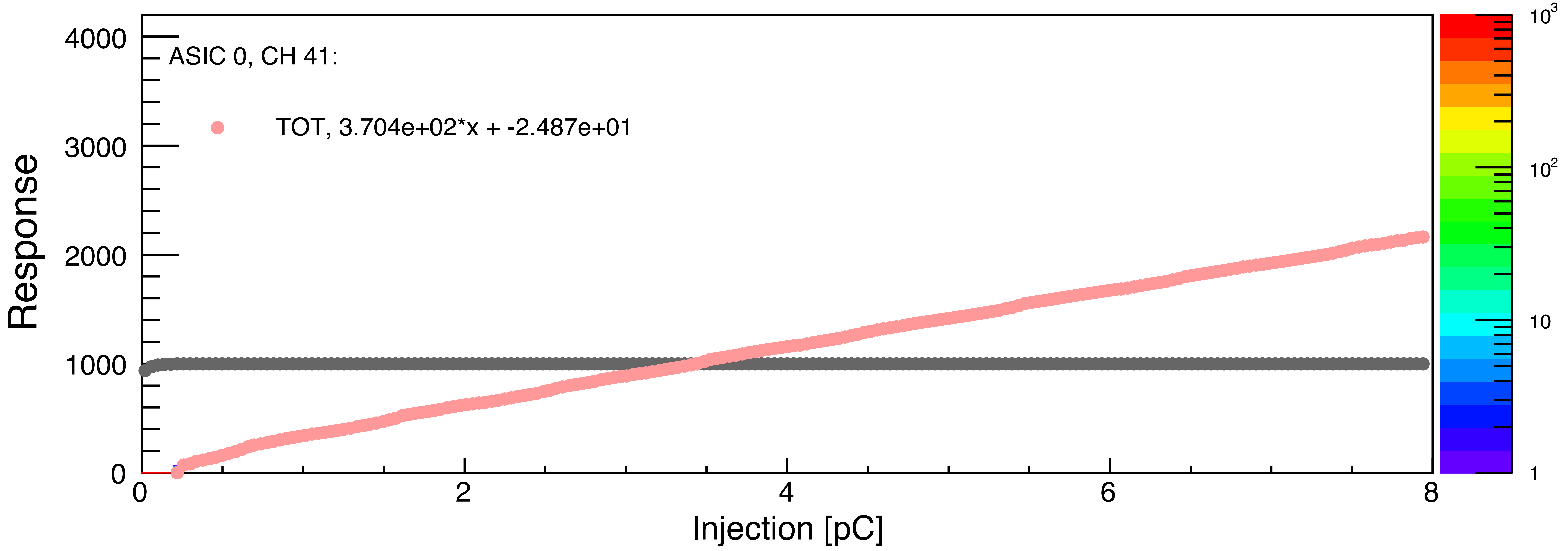
TOA with the 5 phases

Identification of EIC phase with the TOA?
This is just estimation based on some of the knowledge of the chip



The other two phases +20 and -20ns would be in the different buffer

High injection



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