

Timepix status

For far backward working group meeting, 8th Dec 2022

UK EIC Consortium

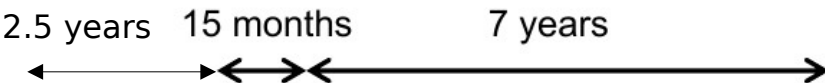
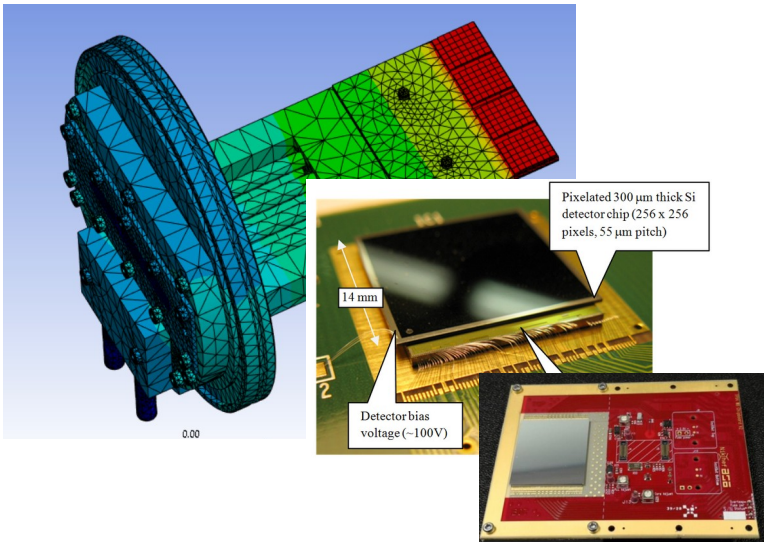
Current Project

2.5 years. R & D. **£3M**

- WP1 MAPS, Central Det (Bham, DL, + ...)
- WP2 **Timepix** (Glasgow, DL)
- WP3 Polarimetry (York)

WP2 Timepix

Is there a role for Timepix at EIC ?
D1. Report by Xmas ... summarised here.



NOTE: US Financial Years (FY) = Oct-Sep

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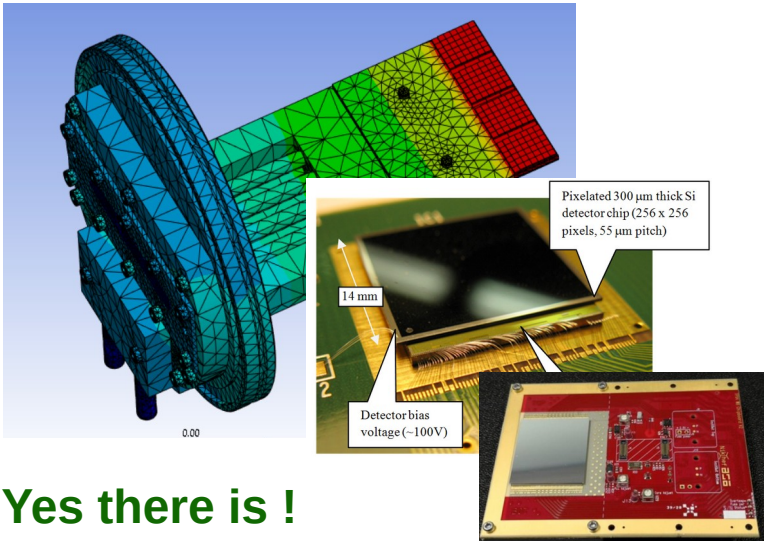
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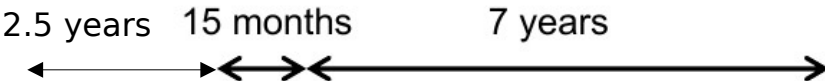
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Yes there is !



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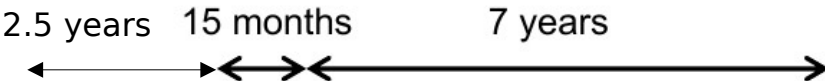
New proposal

7 years. Design and Construction. **£35M**

- WP1 MAPS, Central Det (Bham, DL, + ...)
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- WP3 Polarimetry (York)
- WP4 Accelerator (CI, DL, +)

WP2 Low Q² Tagger / Timepix

Design and build Low Q² Tagger (tracker)



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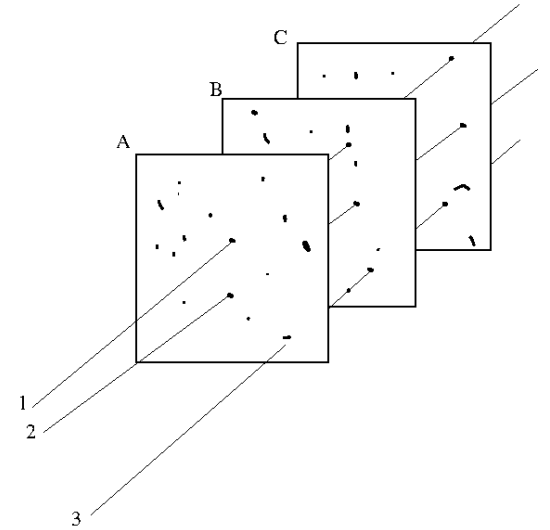
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Glasgow: Simon Gardner, Derek Glazier, Ken Livingston, Dima Maneuski, Ross McGarrie
Daresbury: Mos Kogimtzis, James Lawson, Carl Unsworth

-
- Physics case - established**
- Design – well underway**
- Tagger 2**
z=38 m
- Tagger 1**
z=20 m
- Beamline Magnets**
- Interaction Point**
z=0 m
- Calorimeter**
8x8 array of crystals
length=60 cm
- 4 Tracking Layers**
Size=24x15 cm
Separation=30 cm
- Timepix4 for tracking**
- Luminosity system exit window**
- Drift Vacuum**
- XYZ**
- energy (keV)**
- Pixel No. Y**
- Pixel No. X**
- large blob**
- ridge**
- straight tracks**
- curly tracks**
- small cluster**
- multiple tracks**
- X. Llopart et al 2022 JINST 17 C01044**
- B. Bergmann, et al. NIM A, 2020. 978:164401**

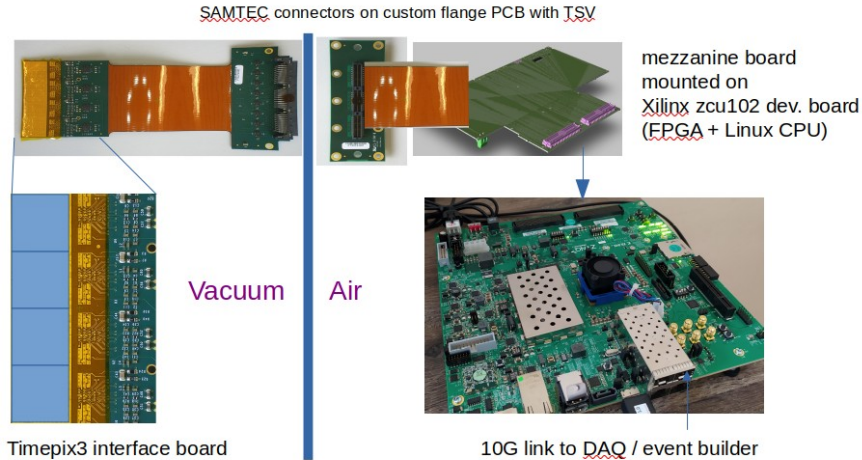
WP2 – Timepix

- **Calorimeter not required for Low Q^2 Tagger** – removed from simulation and design
- **What's required** of a pixel tracker?
- **Position resolution** good enough for physics needs ($\sim 50\mu\text{m}$ adequate)
- **Segmentation** good enough to separate out tracks. ($\sim 50 \times 50 \mu\text{m}$ pixels)
- **Vacuum compatibility**. Cooling. Readout. Beam impedance.
- **Rate capability**.
 - In a bunch crossing:
 - **~ 10 electrons tracks** from the interaction point almost all Brem.
 - These are unrejectable! Need physics - exclusivity, kinematics ...
 - 12ns between bunches \Rightarrow **pixel hit rate per layer = 2.5 GHz**
 - Assume same rate from synchrotron BG.
 - Total rate per layer = **5GHz**. At 64 bits per pixel = **320 Gb/s**. **Very big**. Timepix4 + SPIDR4 can do this.
- Use **FPGA based clustering** to find MIPS. Store only MIPS clusters (x, y, time, energy, width) = 80 bits
- 2 tagger, 4 layers, Trigger Rate 500kHz \Rightarrow **Rate to DAQ = 3.2 Gb/s**. **Very manageable**.



WP2 – Timepix

Timepix3

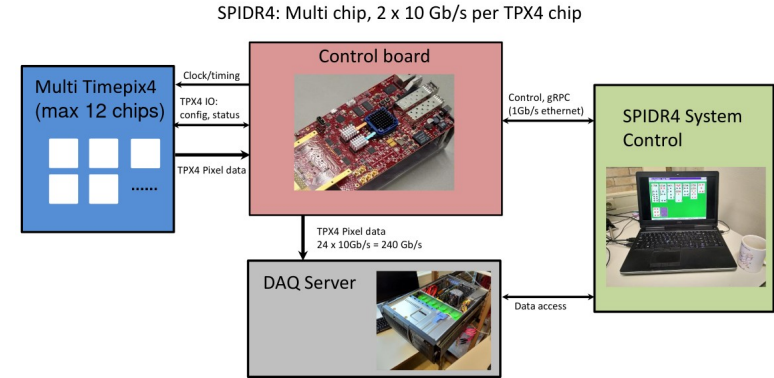


Developed by:
Glasgow Group: Ken Livingston, Dima Manuelski, Simon Gardner
Daresbury Group: Mos Kogutis, James Lawson, Carl Unsworth

Availability of Timepix4 for tracking applications is driving hardware and software development.

SPIDR4 + DAQ tools look set to be the de facto standard
Closest to *off-the-shelf* technology

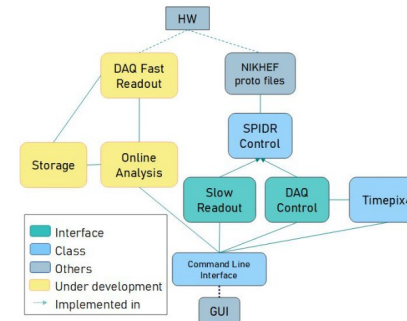
Timepix4



Martin Fransen (martinfr at nikhef.nl), Gridpix brainstorm April 2020

18

Build your own DAQ



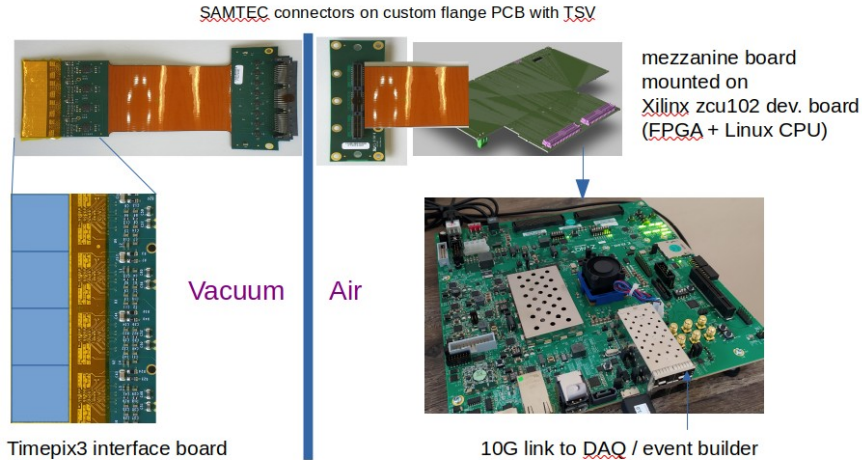
You can use this software also with a hardware read-out system different from SPIDR4.
You only have to write the following 4 methods to:

- Read a Timepix4 Register
Operations to read a register through SC/I2C
Takes register address and returns vector of bytes
- Write a Timepix4 Register
Operations to write a register through SC/I2C
Takes register address and vector of bytes
- Configure the DAQ
Operations to configure the control board
Flexibility: desired configuration as xml file
- Read DAQ Monitoring Information
Operations to read back the control board
Flexibility returning configuration as xml file



WP2 – Timepix

Timepix3

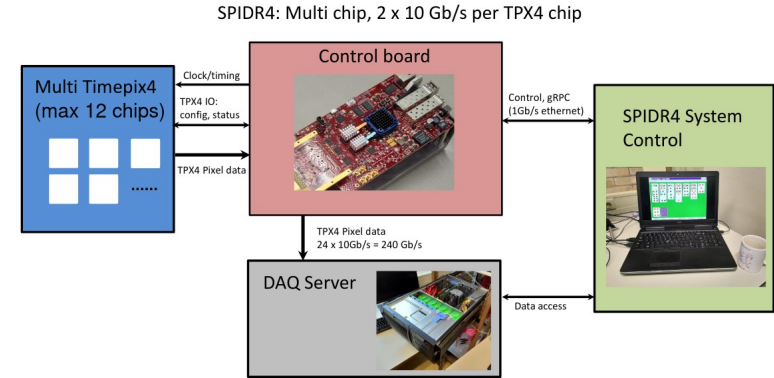


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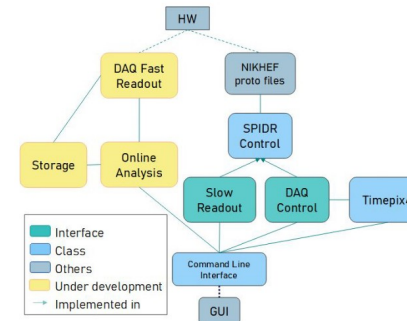
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WP2 – Timepix or something else

An attempt to compare apples with bananas
... please let me know better.

	Requirement	Timepix4	AC-LGAD	MAPS
Readout	—	SPIDR4	EICROC	Direct ?
Pixel Size (μm)	$\sim 50 \times 50$	55×55	500×500	20×20
Sensor thickness (μm)	—	100	50	20
Detector size (pixels)	—	512×448	64×64	?
Detector area (cm^2)	—	6.94	10.24	?
Layer Area (cm^2)	~ 100	$83 (3 \times 4 \text{ Timepix4})$	$92 (3 \times 3)$?
Power consumption (W/cm^2)	As low as possible	1.0	0.4	0.15
Timing resolution (ns)	< 12	0.2	0.03	9
Minimum threshold (fC)	—	1.2	2.0	0.48
Individual pixel thresholds	—	Yes	Yes	No
Pixel hits in MIPS cluster	—	3	30	5 ?
Rate (various units)				
Hits/pixel/s (max)	$\sim 7 \times 10^3$	$\sim 10.7 \times 10^3$?	?
Hits/detector/s (max)	$\sim 1.7 \times 10^9$	$\sim 2.5 \times 10^9$?	?
Bits/detector/s (max)	$\sim 27.0 \times 10^9$	$\sim 160 \times 10^9$?	?
Bits/layer/s (integrated)	$\sim 320 \times 10^9$	$> 240 \times 10^9$?	

Used elsewhere in ePIC

MAPS: for Central Tracker.

Great pos. resolution, very application specific, poor timing, Rate capability? Low power. **Much development needed.**

AC-LGAD for Roman Pots

Very good timing, good pos resolution, big clusters, Rate ? Medium power. **Much development needed.**

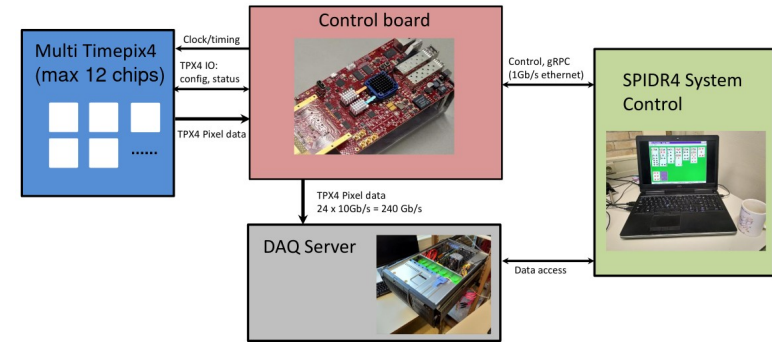
Timepix4 + SPIDR4

Adequate timing, good pos resolution, good cluster size, high rate, high(ish) power. **Available already.**

Hybrid upgrade sensor from standard Si to Inverse LGAD (<30ps).

Timepix4

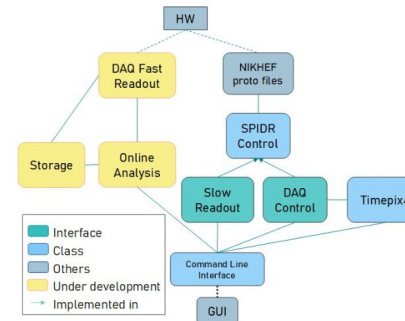
SPIDR4: Multi chip, 2 x 10 Gb/s per TPX4 chip



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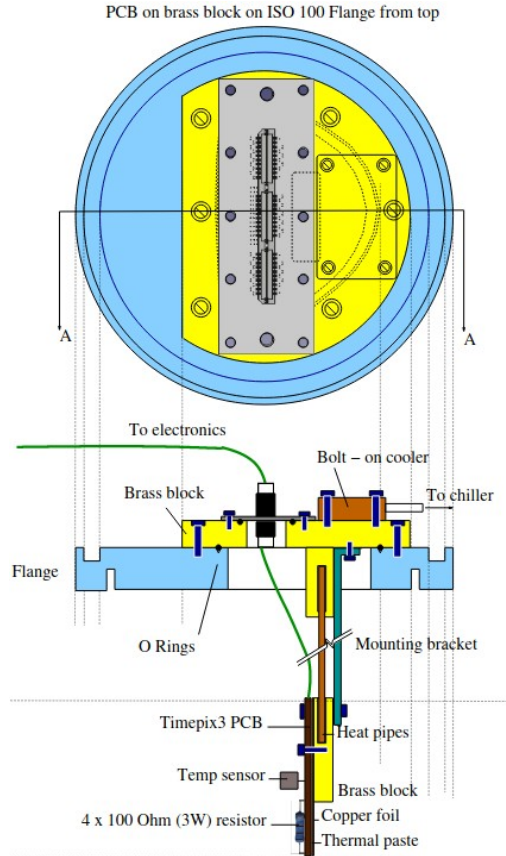
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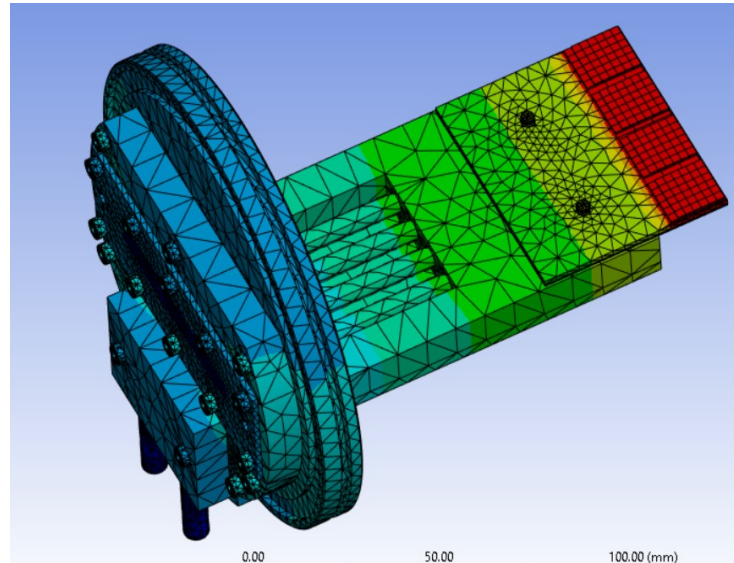
WP2 – Timepix

.. but timepix3 DAQ readout and test rig still essential for development



Real **connectors**, vacuum **feedthroughs**, **heat pipes**
PCB with **temp sensors**. **Resistors** to mock up ASIC heat.
Developed in CAD as **special flange** for ISO 100 mount.
Currently in Glasgow workshop.

To be tested in 10-5 mbar with **external mounted chiller**.
Cooling **modelled in ANSYS**.



WP2 – Timepix

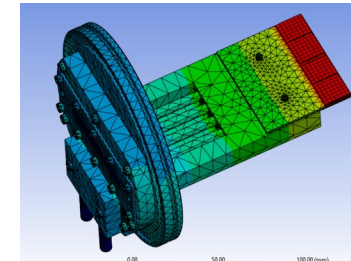
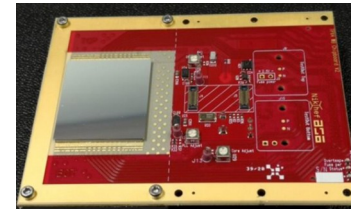
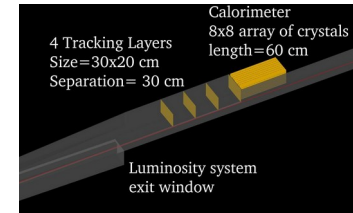
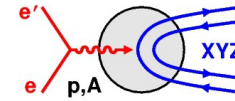
Summary

Strong physics case for low Q^2 tagger.

Design implemented needs more simulation and adjustment

Timepix4 + SPIDR4 looks like the best solution (but other options still being evaluated)

Development for structure, cooling, beamline
Continue with Timepix3 setup.



Links / Refs

Timepix4: X. Llopart et al 2022 JINST 17 C01044

SPIDR4: <http://www.nikhef.nl/~s01/SPIDR4-MF-GP-apr2020.pdf>

SPIDR4 DAQ: <https://indico.cern.ch/event/1215762/contributions/5137274/>

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Deadline 10th Feb 2023

We hope to say:

Far Backward Tagger is now part of the design.

We will lead the development of the pixel based tracker, working with Far Backward Group.

Cost and design based on Timepix4 + SPIDR4

New proposal

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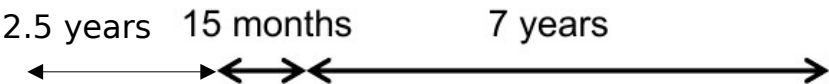
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