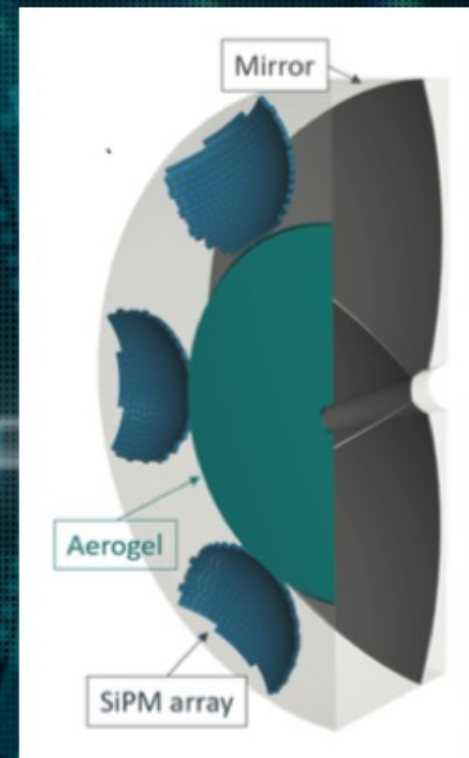
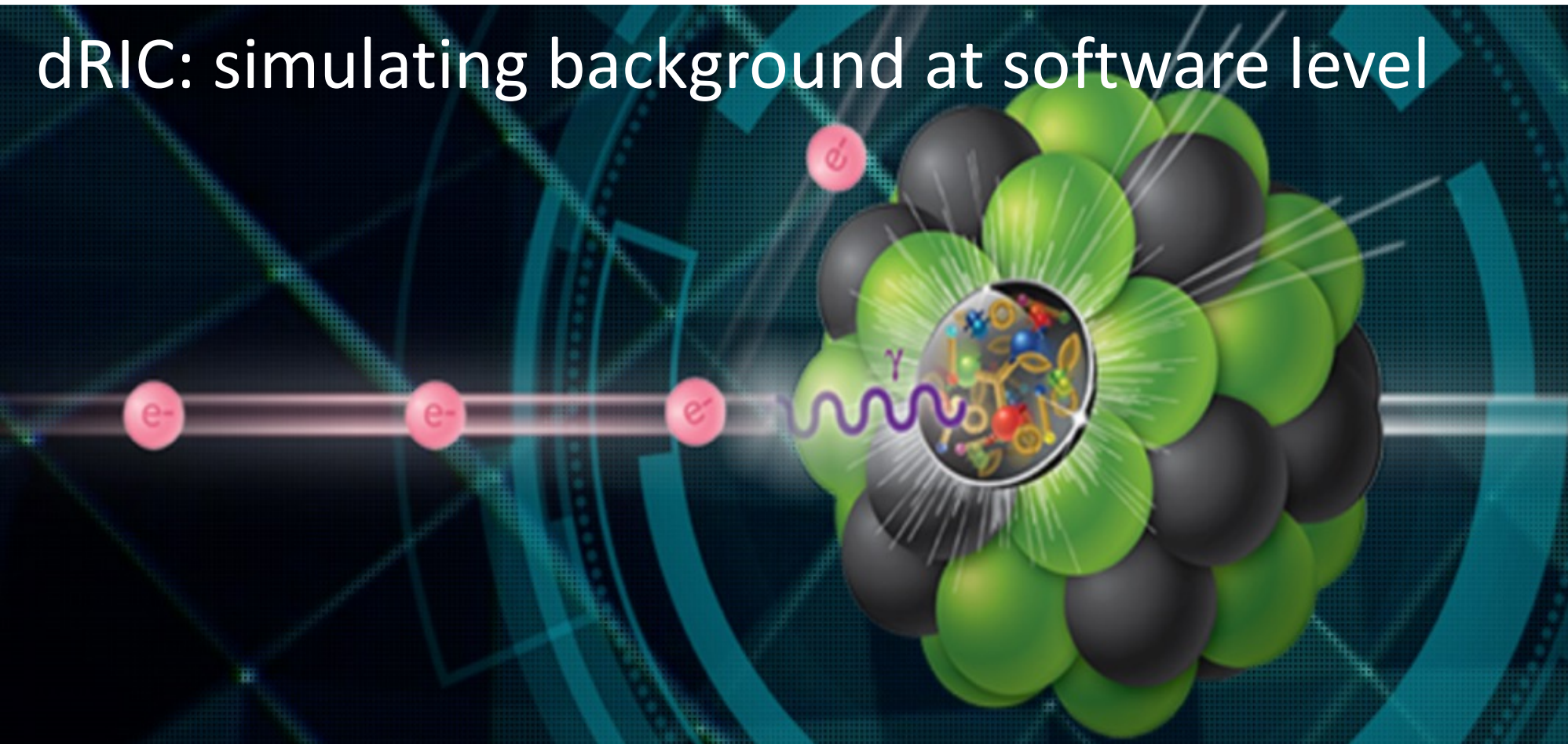
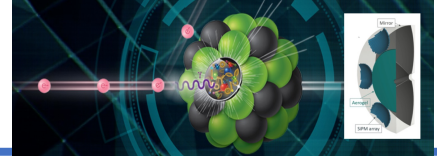


# dRIC: simulating background at software level



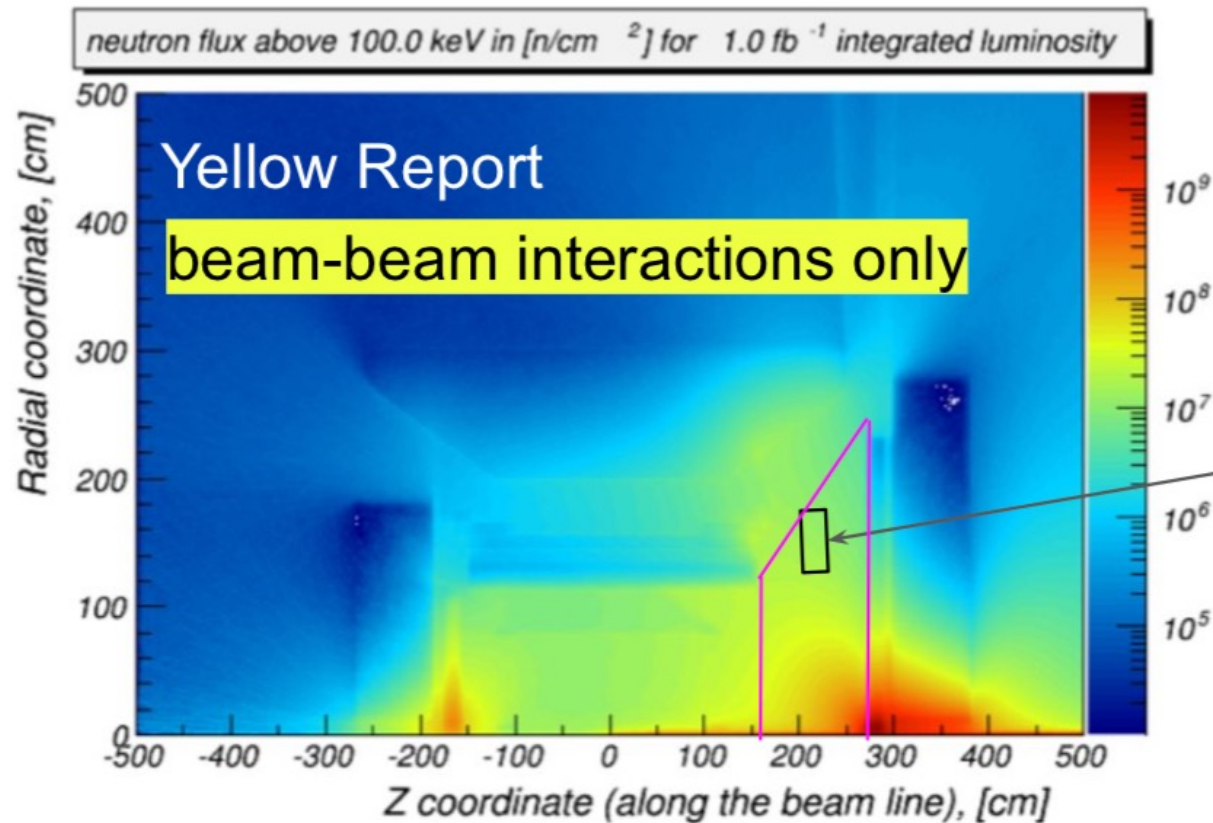
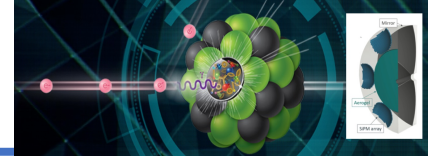
P. Antonioli – INFN Bologna

# Why it is important?



- dRICH with SiPM is expected having increasing background (DCR) with radiation load
  - We now have a much clearer view of what could be the DCR level following radiation damage + annealing
- however we need to have an indication of which would be the maximum DCR we can “tolerate” “by software” i.e. when we start to lose the possibility to identify rings and/or how much resolution worsens with increasing background

# How much radiation?



potential location of photosensors:

$\approx 1\text{--}5 \cdot 10^7 \text{ n}/\text{cm}^2$  every  $1 \text{ fb}^{-1}$

$10^{11} \text{ n}/\text{cm}^2$  1-MeV  $n_{\text{eq}}$  is a "true maximum"

- 30 weeks @  $10^{34} \text{ cm}^{-2} \text{ s}^{-1} = 100 \text{ fb}^{-1} \rightarrow 1\text{--}5 \cdot 10^9 \text{ n}/\text{cm}^2$
- $10^{11} \text{ n}/\text{cm}^2$  would be reached in  $O(10+)$  years at full  $\mathcal{L}$ !

A moderately hostile environment:

$10^9$  1-MeV  $n_{\text{eq}}/\text{cm}^2 \rightarrow$  most of the key physics topics

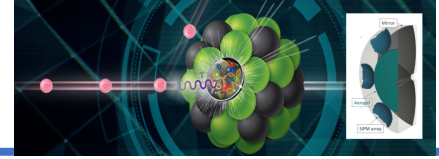
$10^{10}$  1-MeV  $n_{\text{eq}}/\text{cm}^2 \rightarrow$  GPD and more statistically eager topics

$10^{11}$  1-MeV  $n_{\text{eq}}/\text{cm}^2 \rightarrow$  may be we will never go here...

Can we use SiPM for a Cherenkov detector up to  $10^{11}$  1-MeV  $n_{\text{eq}}/\text{cm}^2$  fluence?



# Electrically induced annealing techniques



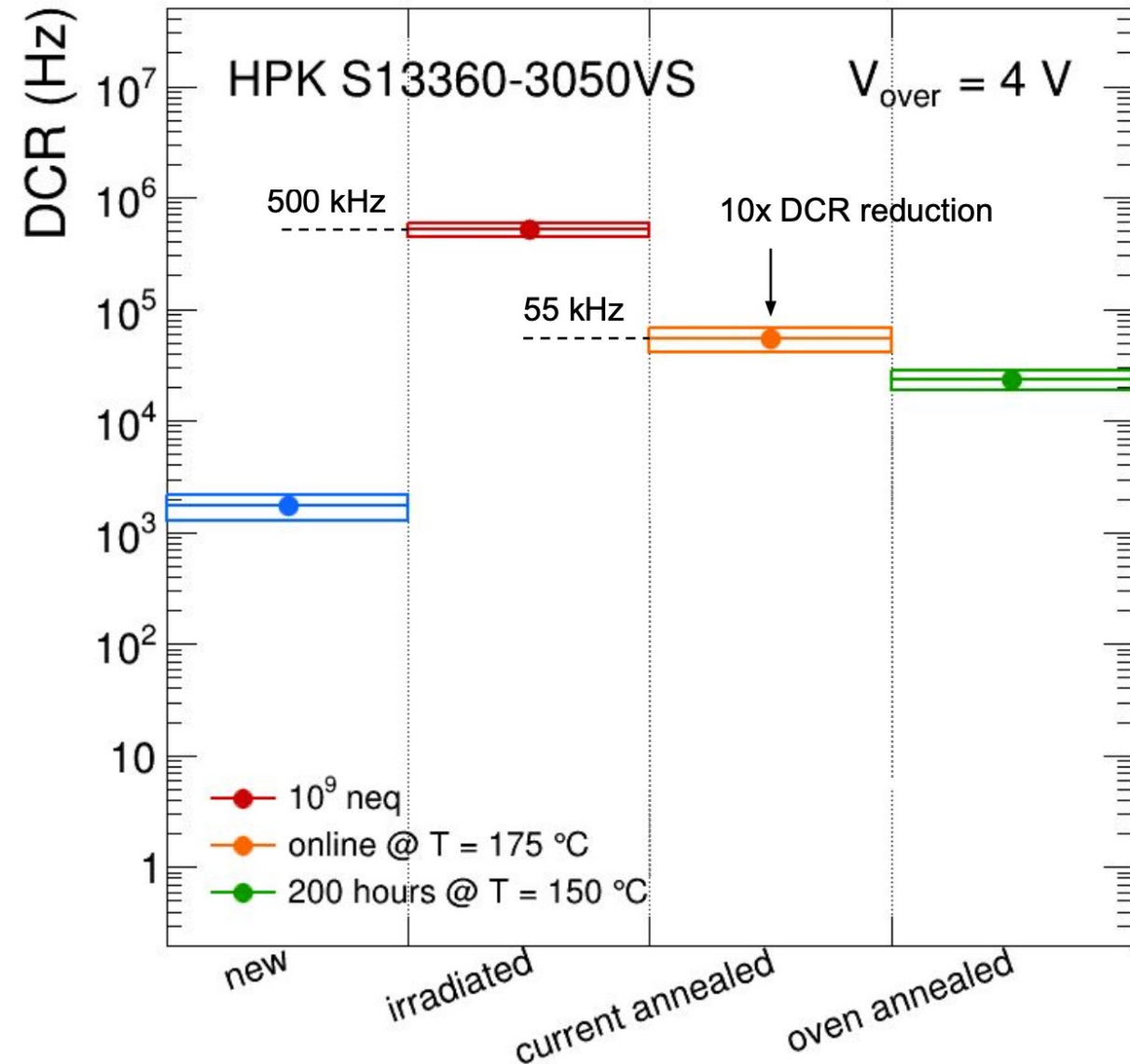
The sensors current-annealed found at 55 kHz

Residual DCR not good as in oven (15 kHz) but:

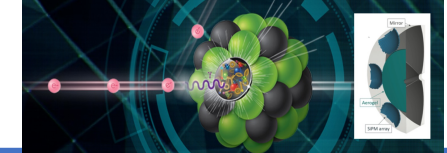
- 100 times faster!! (2.5 hours vs 200 hours!)
- can be done in-situ
- can be done more frequently

It looks very promising!

Specific R&D planned for 2023 on this item



# Radiation damage & annealing



## Radiation damage model (HPK S13360-3050 @ $V_{over} = 3\text{ V}$ )

- **reasonable assumptions**

- radiation damage is additive
- does not know and care of the past damage
- annealing heals up to a certain fraction of damage, not more than that

- **numbers**

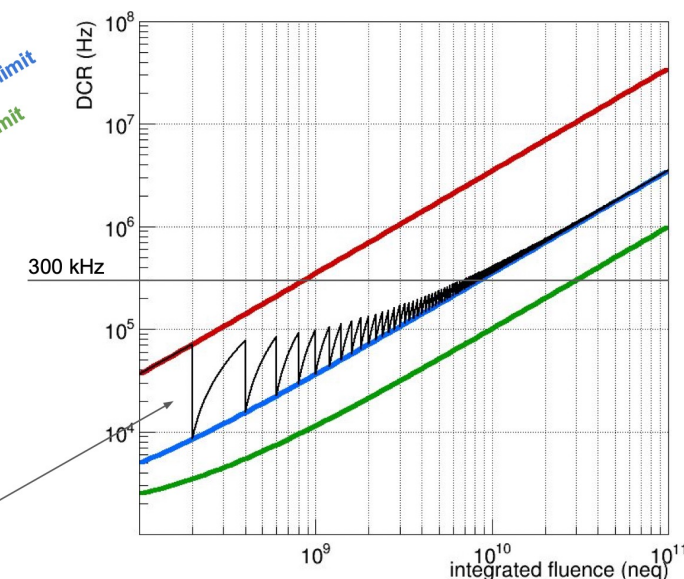
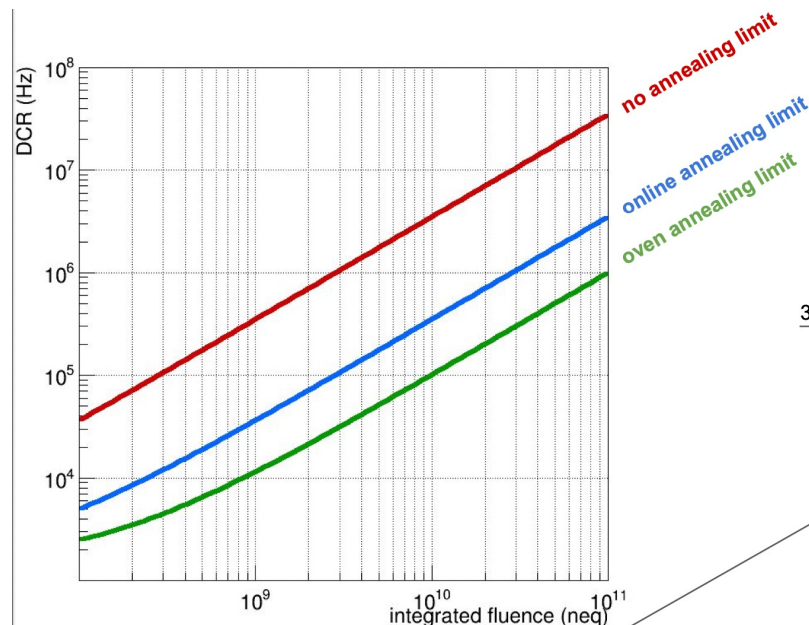
- DCR when new = 1.5 kHz
- DCR increase with radiation damage = 350 kHz /  $10^9$  neq
- DCR increase with online annealing = 35 kHz /  $10^9$  neq
- DCR residual after oven annealing = 3%

- **how it works?**

- start with DCR as new  $\rightarrow$  NEW
- add DCR with increasing radiation  $\rightarrow$  NEW + NIEL1
- heal with annealing  $\rightarrow$  NEW + x NIEL1
- add DCR with increasing radiation  $\rightarrow$  NEW + x NIEL1 + NIEL2
- heal with annealing  $\rightarrow$  NEW + x ( NIEL1 + NIEL2 )

Message:

Max “tolerable” rate per channel determines frequency of annealing



online annealing every  $2 \times 10^8$  neq (500 times)

# dRICH throughput estimates

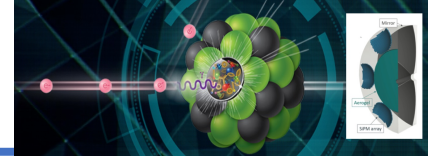


Table 2.5: Maximum data volume by detector.

from ATHENA proposal

Detector	Channels	DAQ Input (Gbps)	DAQ Output (Gbps)
B0 Si	400M	<1	<1
B0 AC-LGAD	500k	<1	<1
RP+OMD+ZDC	700k	<1	<1
FB Cal	4k	80	1
ECal	34k	5	5
HCal	39k	5.5	5.5
Imaging bECal	619M	4	4
Si Tracking	60B	5	5
Micromegas Tracking	66k	2.6	.6
GEM Tracking	28k	2.4	.5
pRWELL Tracking	50k	2.4	.5
dRICH	300k	1830	14
pRICH	225k	1380	12
DIRC	100k	11	11
TOF	332k	3	.8
Total		3334	62.9

ASSUMPTIONS in these estimates

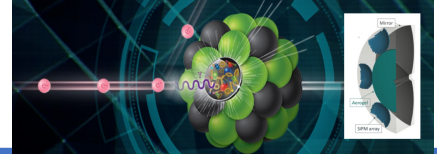
- throughput @ average 300 kHz DCR per pixel MAX before moving to annealing cycles given limitations on ALCOR and DAQ bandwidth
- factor 3 reduction due to timing selection
- throughput assumed 64 bit per hit (TOT)

## Future developments and outlook

- timing reduction could be factor 10 (shutter on ALCOR)
- cooling at  $T = 40\text{ }^{\circ}\text{C}$  would help another factor 2
- TOT might not be necessary?
- frequent electrically induced annealing
- ....

Note: 1.8 Tbps (300 kHz/pixel) is after  $> 6 \cdot 10^8 n_{eq}$  (and no annealing and under above assumptions) but we will start @ 7.3 Gbps (2 kHz/pixel)

# Some back of the envelope estimates



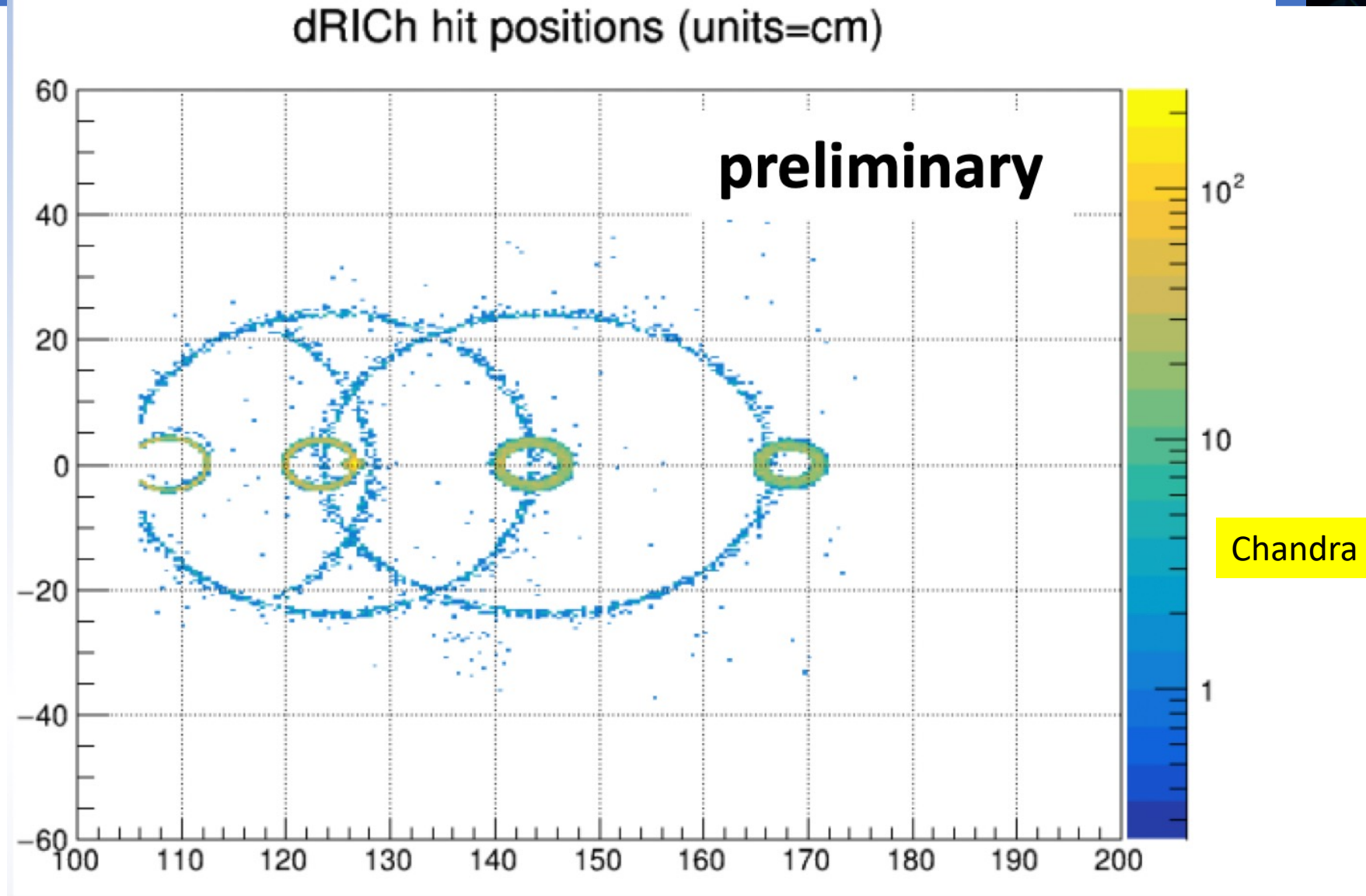
- DCR is easy to simulated: just white noise at a DCR given rate
- Simulate RICH “images” and have as external parameter  $fDCR = DCR \text{ rate} / \text{pixel}$
- Assume “shutter” (time cut) at 3 ns or 1 ns
- Assume 310k channels

fDCR (kHz)	shutter 3 ns	shutter 1 ns	Tot Hit (1 ns)	Tot Hit (sector)
3	0,9	0,3	0,93	0,155
30	9	3	9,3	1,55
300	90	30	93	15,5
5000	1500	500	1550	258,3333333
310000				

+ 20 hits from rings

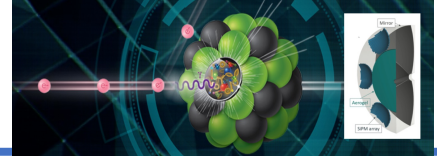
Random sample hits (from background) 1 ns or 3 ns window...  
Worst case: 5 MHz input rate

# We need to add the DCR and check!





# Requests

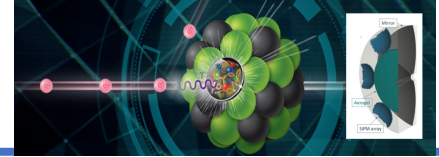


Produce images + background at increasing rate

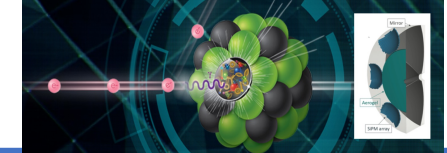
“simple file format”

INFN groups with AI algorithm starting in February very much useful “sector matrix” (+ time)

# Backup



# Throughput (I)



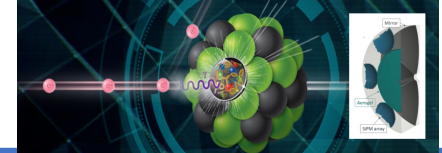
- ALCOR clock 320 MHz ma dati serializzati a frequenza DDR a gruppi di 8 canali → le parole di 32 bit sono encoded a 40 bit
- Questo porta a un limite massimo di 640 Mb/s che corrisponde a un massimo rate su 8 canali di 16 MHz → quindi siamo ora limitati a 2 MHz su singolo canale (averaged su 8)

Starting to play with numbers and known limitations:

- Below no TOT
- Note that 10 Gbps limitation might be overcome (20 Gbps seems reachable even if rad. Tol. might be problem) to be investigated
- Exploit timing reduction

Singolo canale	serializer 8 canali ALCOR column			FPGA (16 ALCOR-64). Timing reduction		Opt Link
	16 MHz	8 ch	→ ALCOR-64			
5 MHz	2 MHz	64 MB/s.	→ 512 MB/s	8 GB/s → 64 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s.	→ 76,8 MB/s	1,2 GB/s → 9,8 Gbps	1	10 Gbps
300 kHz	300 kHz	9,6 MB/s.	→ 76,8 MB/s	1,2 GB/s → 9,8 Gbps	3	3,3 Gbps

# Throughput (II)



ALCOR test pulse (in inverse polarity) can act as “inhibit” of the digitalization. This could help greatly to reduce data throughput  
Note [EIC beam bunch timing](#) presentation by Todd (Sep. 2022)

Short summary:

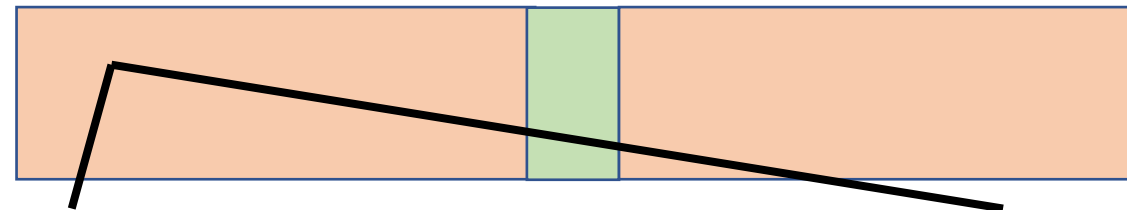
<b>EIC Orbit</b>	<b>12.78 usec</b>
<b>Bunch spacing (Nb 290)</b>	40.599 ns
<b>Bunch spacing (Nb 1160)</b>	10.150 ns
<b>Gap length</b>	1.01 usec
<b>Collision spread (bunch length)</b>	23-30 ps (ESR) 250-200 (ps) HSR

Notes:

- we will need to implement disable during gap region which is sizeable (8% data reduction “for free”)
- Bunch crossing every 10 ns! With a bunch length of 250 ps if we could select just 1 ns data reduction by a factor 10 before serializing stage in ALCOR

Critical measurement to be done in Turin:

- How react ALCOR to such “short” shutter cycles?
- What happens to the TOT measurement?
- What happens if trailing edge is ON and leading edge was OFF

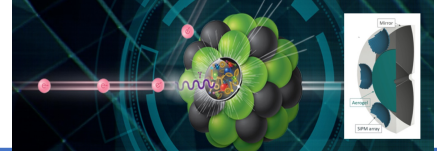


Note LHCb is thinking something very similar with [FastRich](#)

If it works then requirement on precise clock alignment / phase shift inside FPGA sending shutter to ALCORs



# Throughput (III)



		serializer						
		8 canali						
		ALCOR column						
		16 MHz						
Singolo canale			8 ch	→	ALCOR-64		FPGA (16 ALCOR-64). Timing reduction	Opt Link
5 MHz		2 MHz	64 MB/s.	→	512 MB/s	8 GB/s → 64 Gbps	1	10 Gbps
300 kHz		300 kHz	9,6 MB/s.	→	76,8 MB/s	1,2 GB/s → 9,8 Gbps	1	10 Gbps
300 kHz		300 kHz	9,6 MB/s.	→	76,8 MB/s	1,2 GB/s → 9,8 Gbps	3	3,3 Gbps
5 MHz		500 kHz	16 MB/s.	→	64 MB/s	1,0 GB/s → 8 Gbps	1/0.92	7,4 Gbps