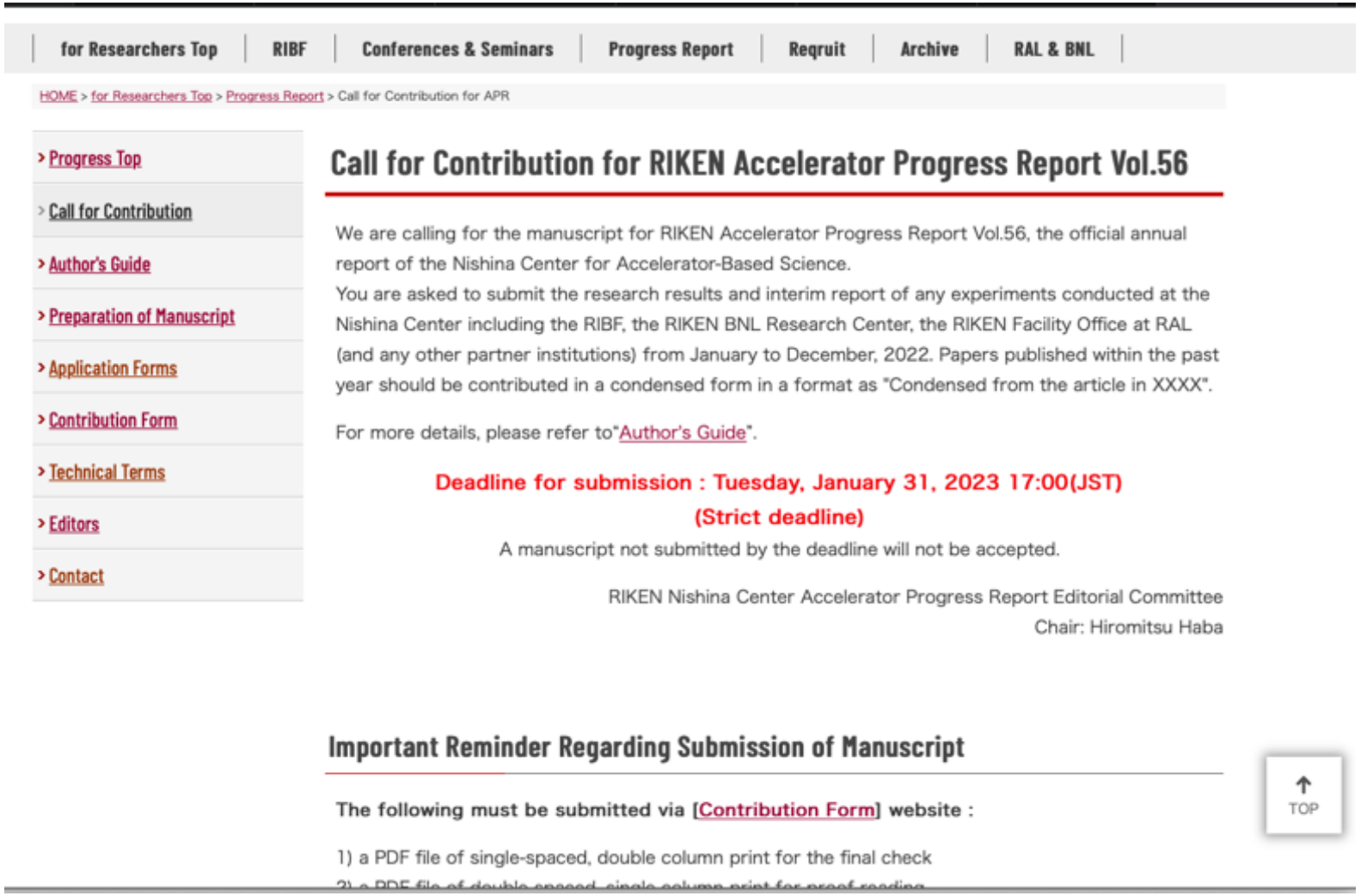
INTT Status Update

RIKEN/RBRC

Itaru Nakagawa

Call for Contribution for RIKEN APR

https://www.nishina.riken.jp/researcher/APR/call_e.html



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Call for Contribution for RIKEN Accelerator Progress Report Vol.56

We are calling for the manuscript for RIKEN Accelerator Progress Report Vol.56, the official annual report of the Nishina Center for Accelerator-Based Science.
You are asked to submit the research results and interim report of any experiments conducted at the Nishina Center including the RIBF, the RIKEN BNL Research Center, the RIKEN Facility Office at RAL (and any other partner institutions) from January to December, 2022. Papers published within the past year should be contributed in a condensed form in a format as "Condensed from the article in XXXX".

For more details, please refer to"Author's Guide".

Deadline for submission : Tuesday, January 31, 2023 17:00(JST)

(Strict deadline)

A manuscript not submitted by the deadline will not be accepted.

RIKEN Nishina Center Accelerator Progress Report Editorial Committee
Chair: Hiromitsu Haba

Important Reminder Regarding Submission of Manuscript

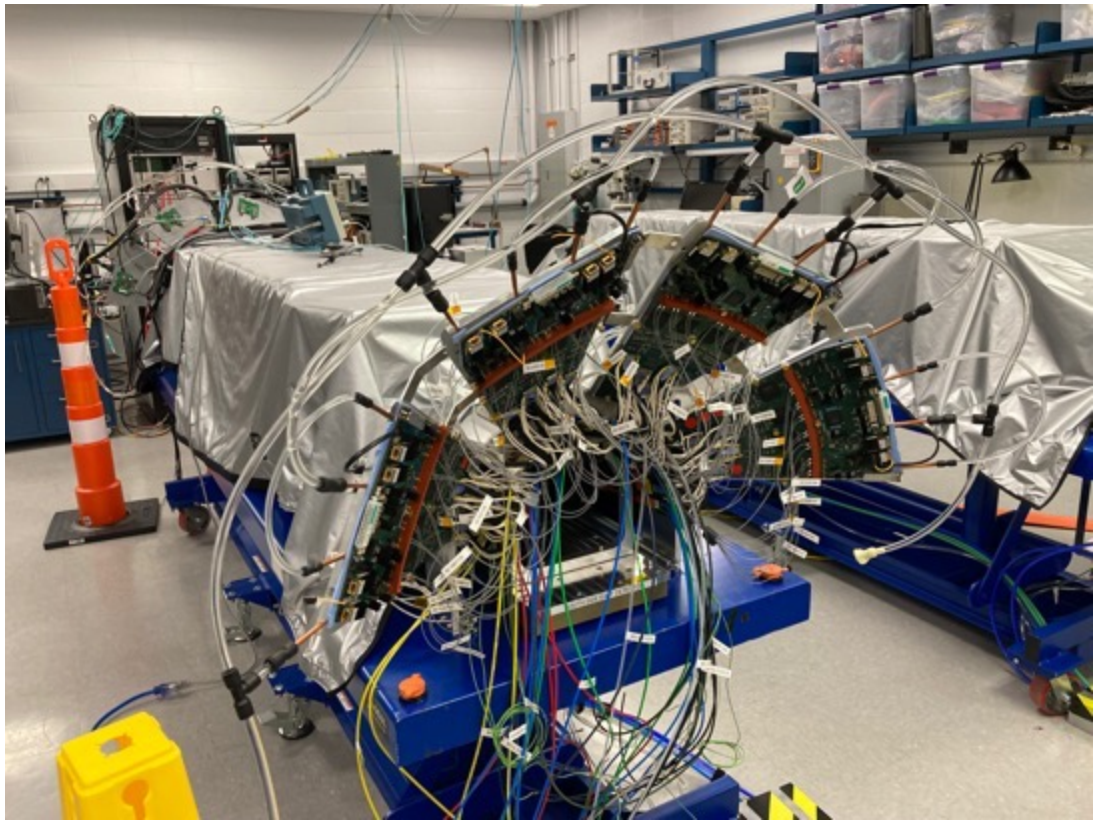
TOP

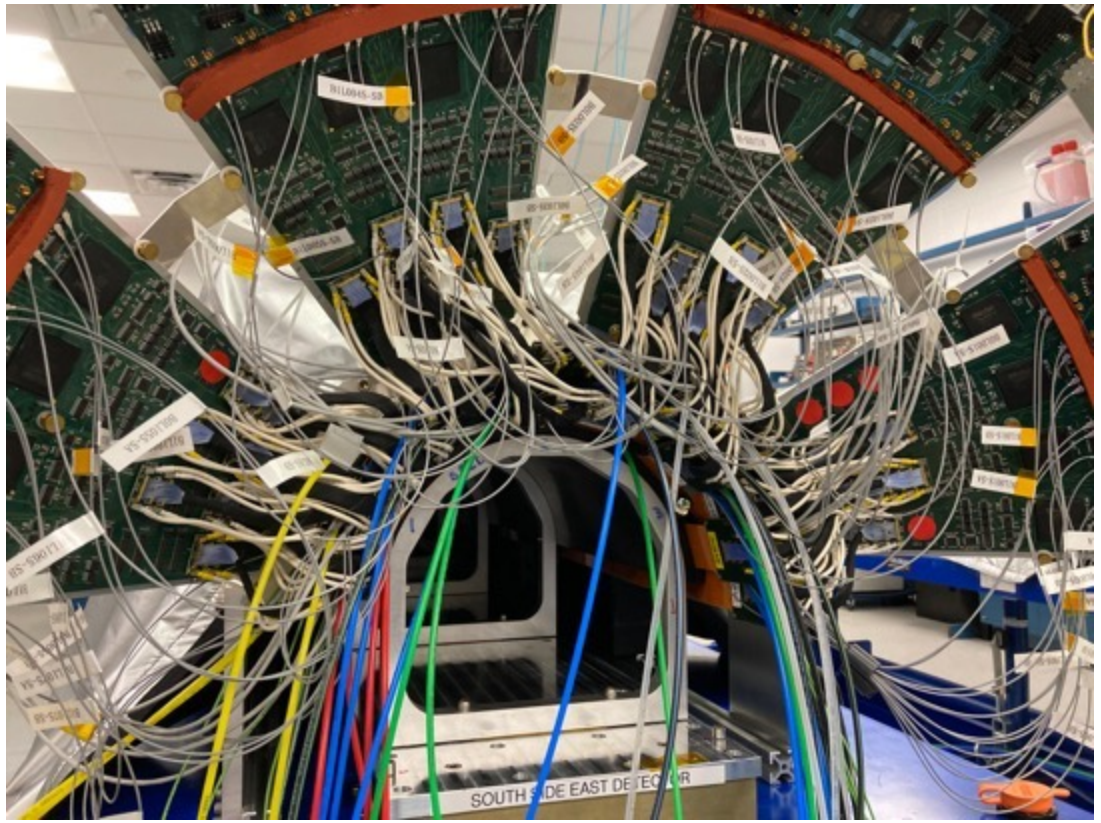
The following must be submitted via [Contribution Form] website :

1) a PDF file of single-spaced, double column print for the final check

- 1 page summary of your major work for INTT
- Deadline is January 31st.
- It is encouraged to send your draft to the INTT mailing list a week before the deadline
- Author list is to be provided from Itaru soon
- Latex style file can be found in the “Application form” page of the left menu

Barrel Testing with Felix Readout





7 ladders / ROC Simultaneous Readout using Felix has been completed successfully

Load Map of Felix Readout

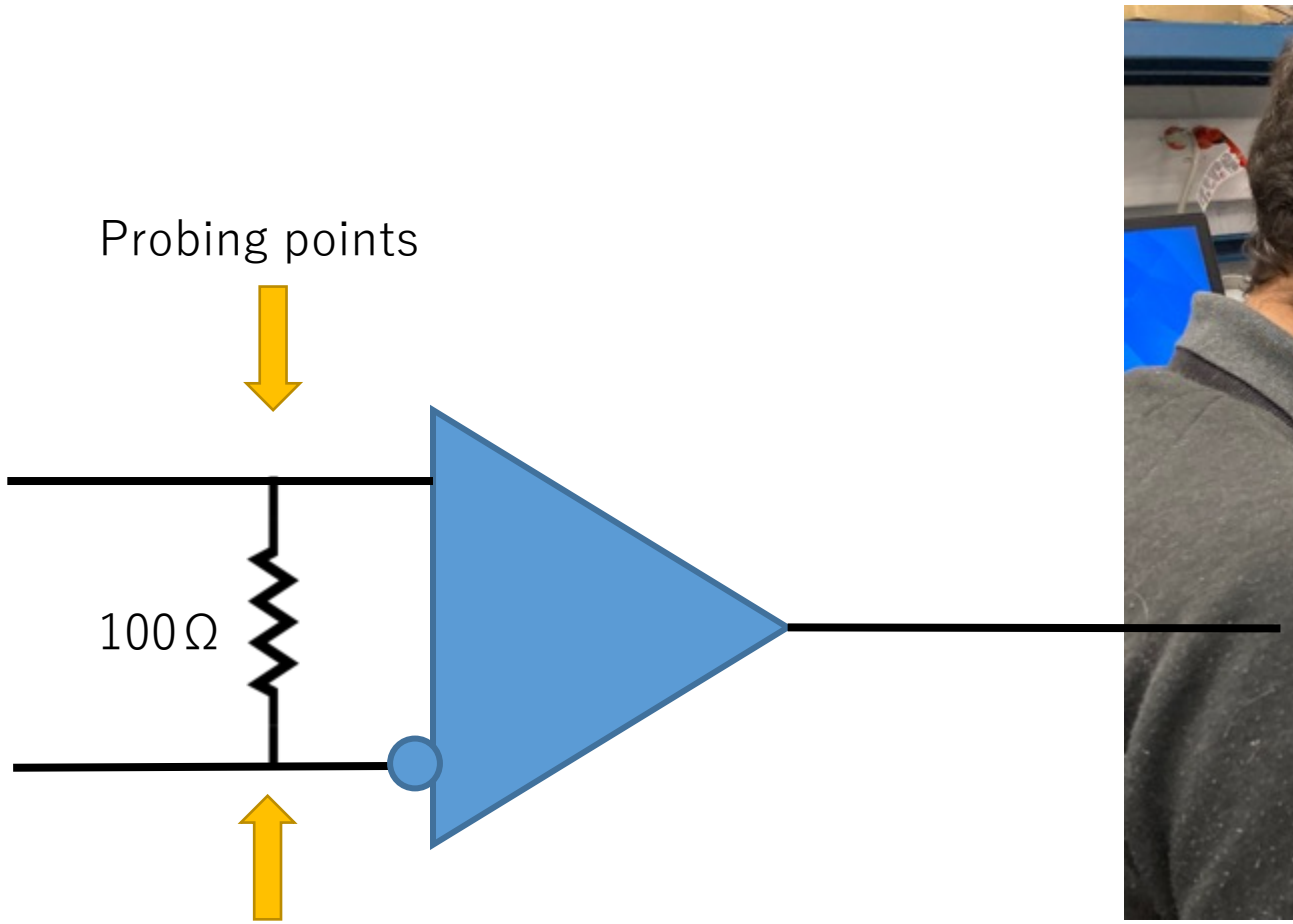
1. 7 Ladders Simultaneous Readout (done)
2. 2 ROCs with single Felix Readout (Achieved once)
3. 2 ROCs with 2 Felix Readout
4. GTM External Trigger Readout (Cosmic Trigger)
5. Integration to RCDAQ

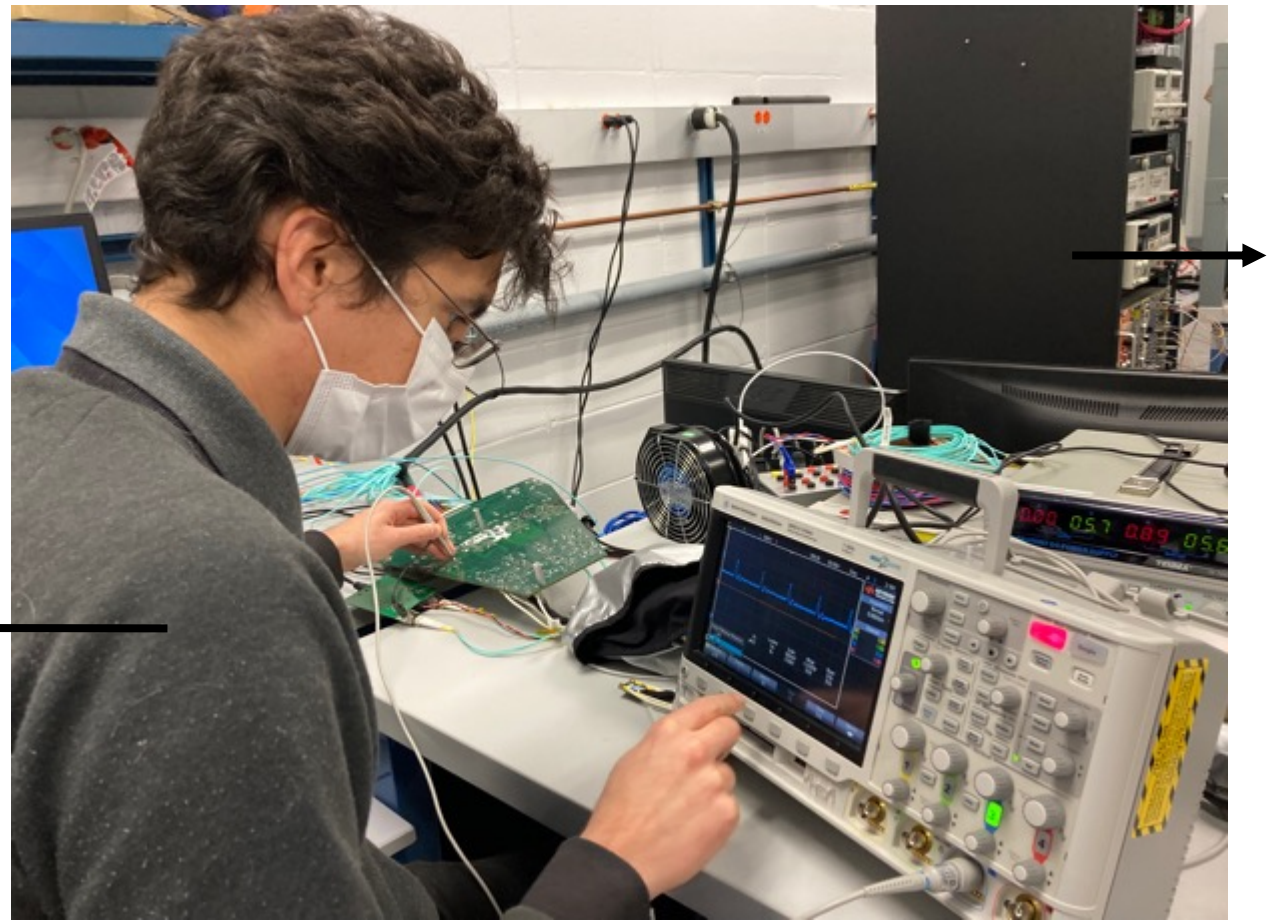
Problem in North Side Test

- Lost correlation between ADC and amplitude DAC value in the data taking.
- This problem is caused by the loosing the slow control link at the beginning of run.
- It occurs in all 4 ROCs in North side. It comes and go so far.
- Initial debugging attempt didn’t pin down the exact cause.
- Need further investigation (perhaps Raul comes back from his vacation ~ middle of January)

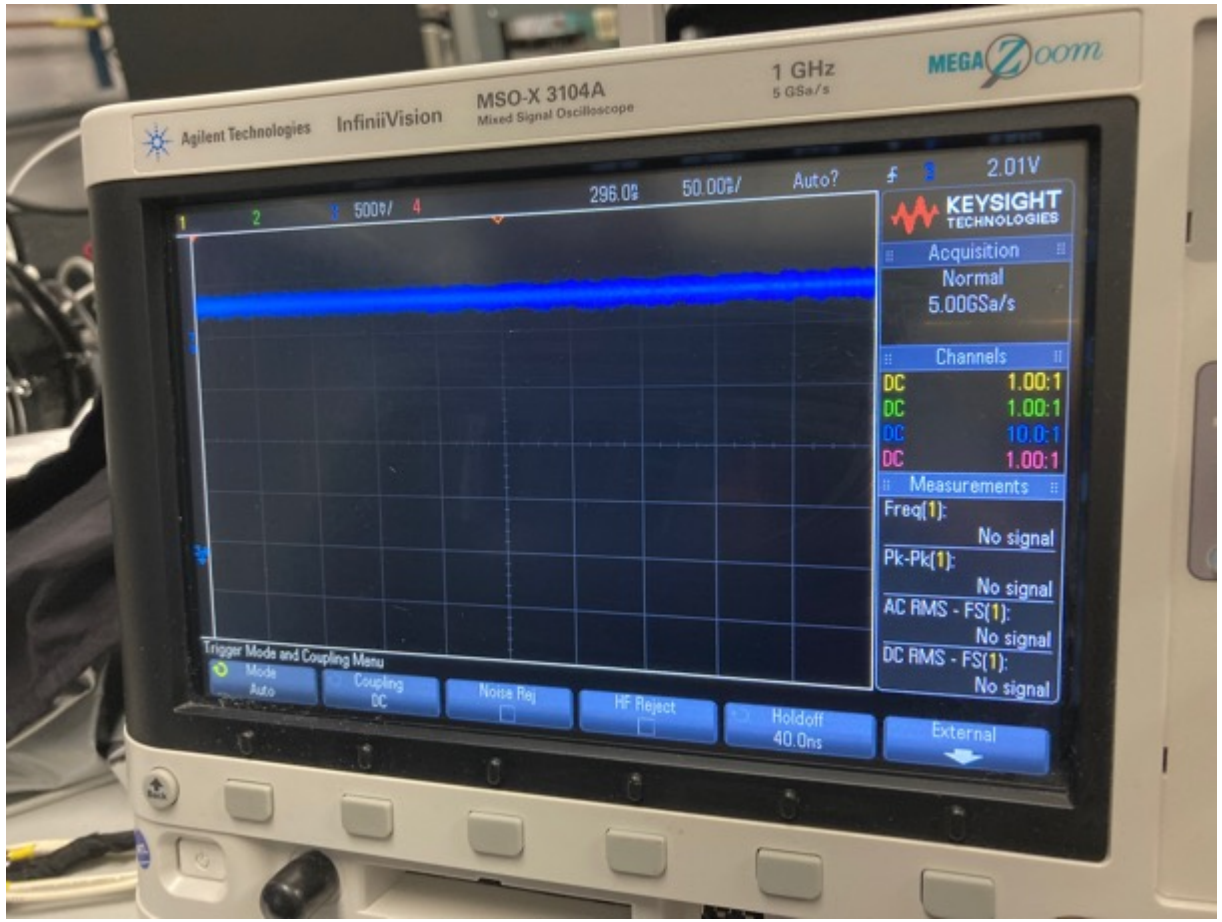
Cause of Fake Hits

Attempt to Observe Fake Hits





Observation



- Probed open ports during calibaration data taking where fake hits appears in the analysis.
- As far as we monitored with a scope, no AC components are observed. No DC level change was observed neither.
- Observed only very quiet DC component.
- It is very hard to create such a fake hits from this observation.
- A new hypothesis arised that fake hits are generated even downstream of the open ports.
- For example, misbehavior of radiation damaged TLK chips?

Partial Data Drop Issue in ROC D3 Port

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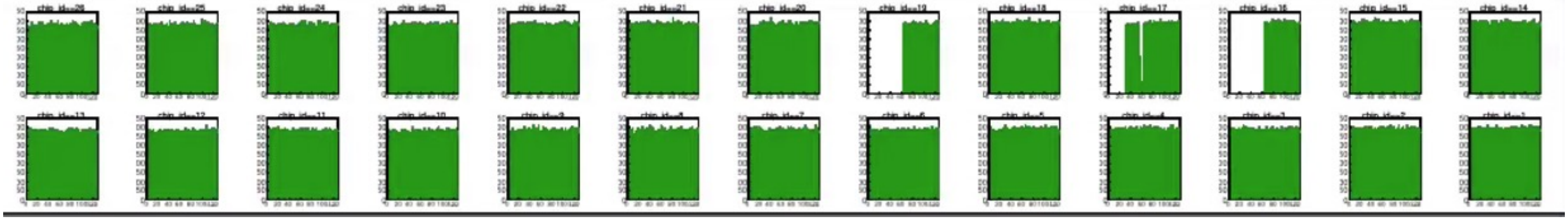
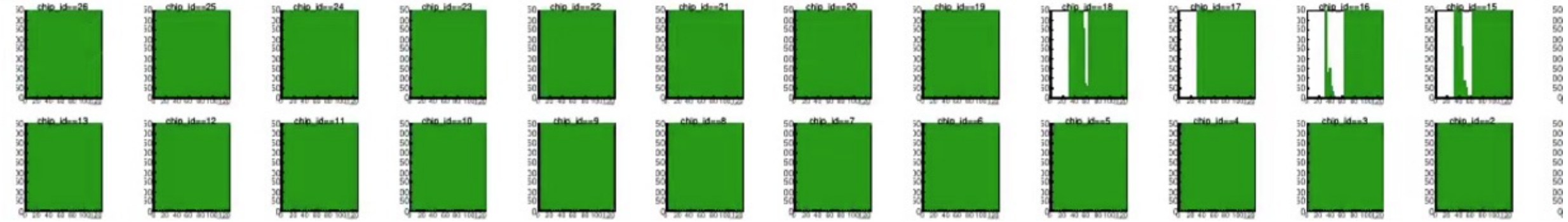
Partial Data Drop in D3 Port Issue

ROC SW5

Data: 221207_1941



Data: 221207_1741

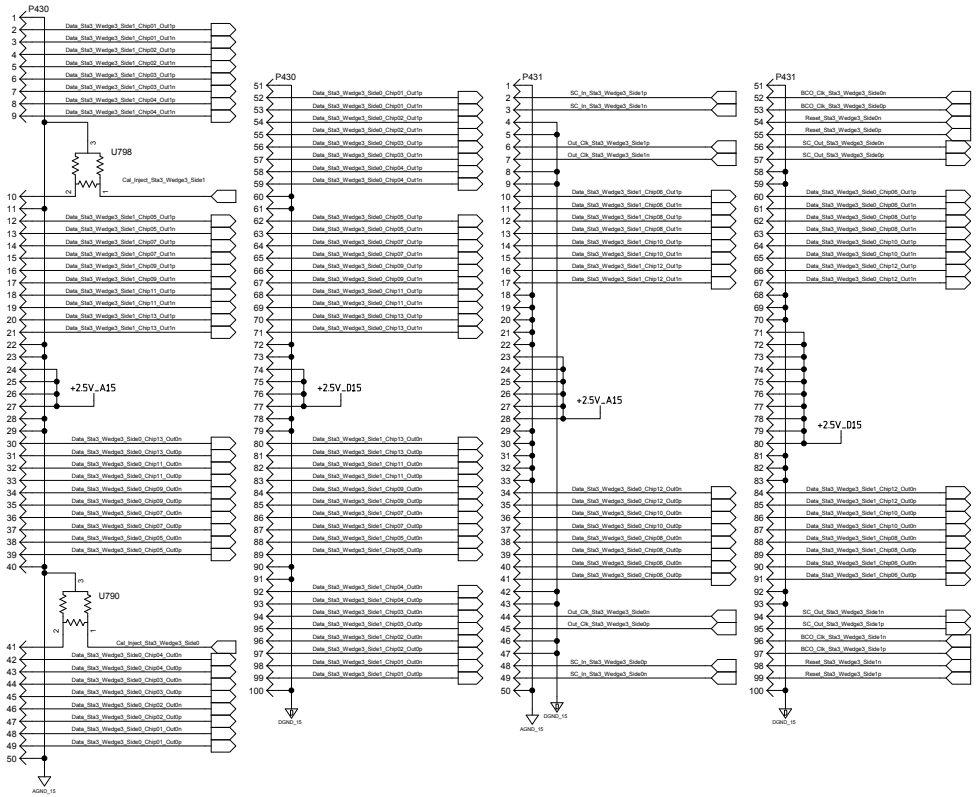


The partial data drop issue is reproduced in BNL as well with Barrel ladders (BEX+Production CC)

What can be wrong?

- The reproducibility of this problem is very good. I am afraid it is not something fragile condition causes this symptom.
- One possibility is intrinsic design difference of the D3 port with respect to other ports.
- There do exist different circuits in ROC which we learned from the past, for instance, floating GND of A1 digital regulator.

P431&P431 Ports



Station 3 Wedge 3

AS OF 07/11/2011 @ 9:33AM

REVISION LETTER	CLASS REVIEW	REVISIONS	DATE	CHANGE BY	CHECK BY	APPROVED BY
—		ORIGINAL ISSUE	—	—	—	—

LOS ALAMOS
LOS ALAMOS NATIONAL LABORATORY
LOS ALAMOS, NEW MEXICO 87545

MENTOR 2005

	NAME	SIGNATURE	DATE	GROUP
ORIGINATED				
DESIGNED				
DRAWN	S. CHACON	S. CHACON	APR 2009	AOT-IC
CHECKED	M. PROKOP	M. PROKOP	APR 2009	AOT-RFE
PROJ. ENGR.	M. PROKOP	M. PROKOP	APR 2009	AOT-RFE
APPROVED				
RELEASED				

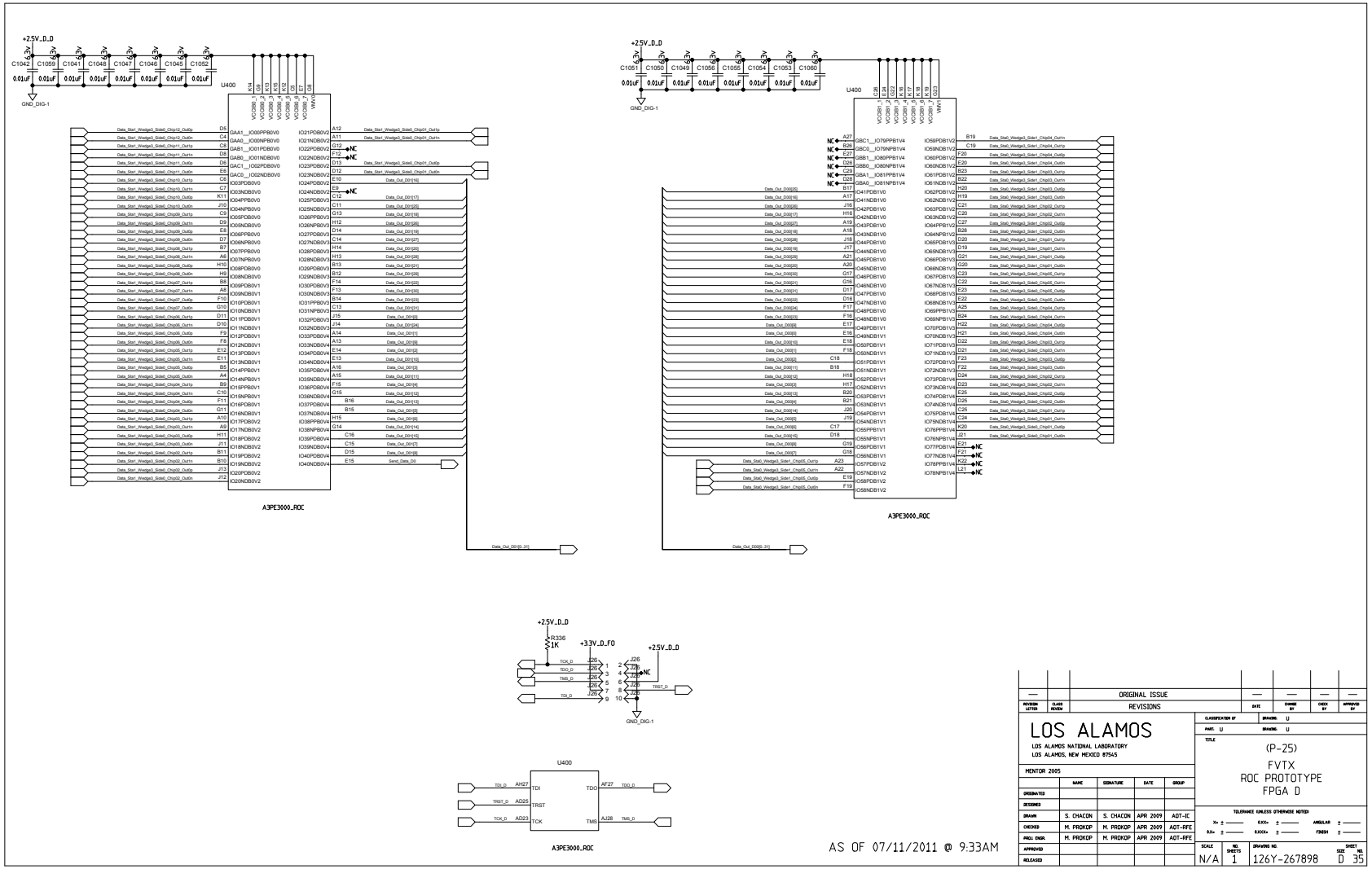
CLASSIFICATION OF: DRAWING: U
PART: U DRAWING: U

TITLE
(P-25)
FVTX
ROC PROTOTYPE
SIGNAL CONNECTORS-STATION 3

TOLERANCE (UNLESS OTHERWISE NOTED)
X± — 0.XX± — ANGULAR ±
0.X± — 0.XXX± — FINISH ±

SCALE	NO. SHEETS	DRAWING NO.	SHEET SIZE	SHEET NO.
N/A	1	126Y-267898	D	13

FPGA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C1051 C1050 C1049 C1056 C1055 C1054 C1053 C1060
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U400
A3PE3000_ROC
+3.3V_D_FO
R336
1K
J26
J27
TDI_D
TDO_D
TMS_D
TCK_D
TRST_D
AH27
AD25
AD23
AF27
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