Fermilab U.S. DEPARTMENT OF ENERGY | Office of Science

FCFD Status and Plan

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eRD112/LGAD Consortium Meeting

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Constant Fraction Discriminator ASIC (FCFD)

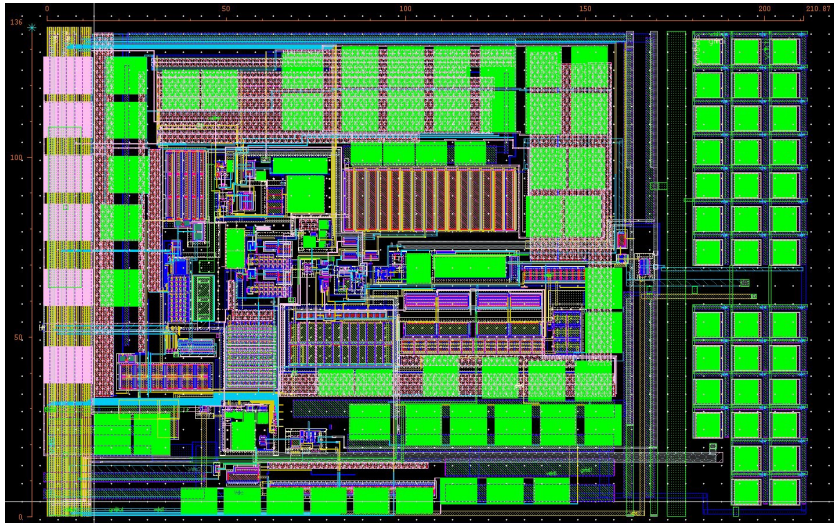
- Develop a robust fast-timing measurement technique for LGADs
  - Easy to use and stable: no corrections, or calibrations and threshold adjustments
- The first (FCFDv0) version was designed, produced and tested with DC-LGAD sensors
  - Excellent performance demonstrated with charge injection, laser and beta source
- The next version (FCFDv1) is being optimized with EIC sensor specifications
  - In close collaboration with the EIC detector experts and AC-LGAD developers
- CFD approach achieves better performance, especially for low S/N systems, such as LGADs **(NIM A 940 (2019), pp 119-124)**

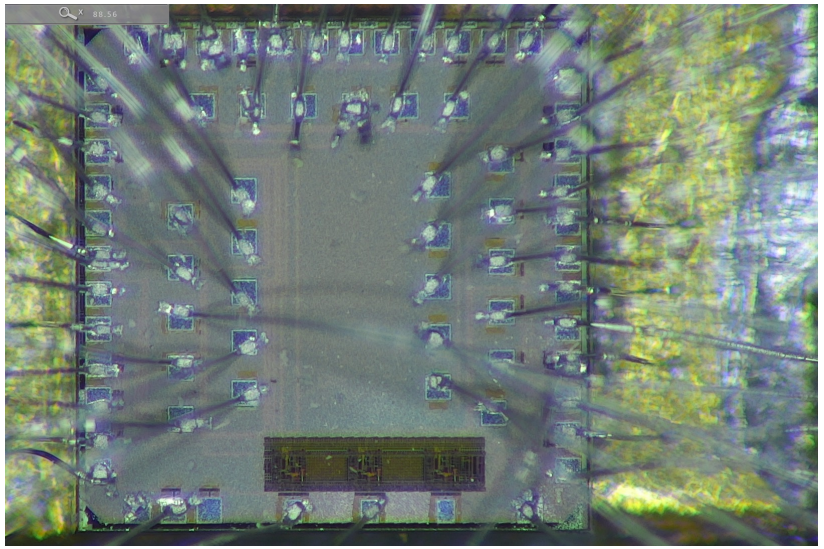
Advantages of CFD approach

- The difference was studied in detail in **NIM 940 (2019)**
  - At low signal amplitudes, CFD algorithm outperforms LE
  - CFD algorithm offers significant reduction in noise, as demonstrated in TOFHIR ASIC for CMS barrel timing detector
    - Improvement in the time resolution by x3.5 in TOFHIR
  - CFD-based readout is much simpler in operation and maintenance
    - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc…
  - Power consumption for analog front-end LE and CFD comparable
    - Consumption for the digital parts is expected to be low, completed blocks exist

FCFDv0

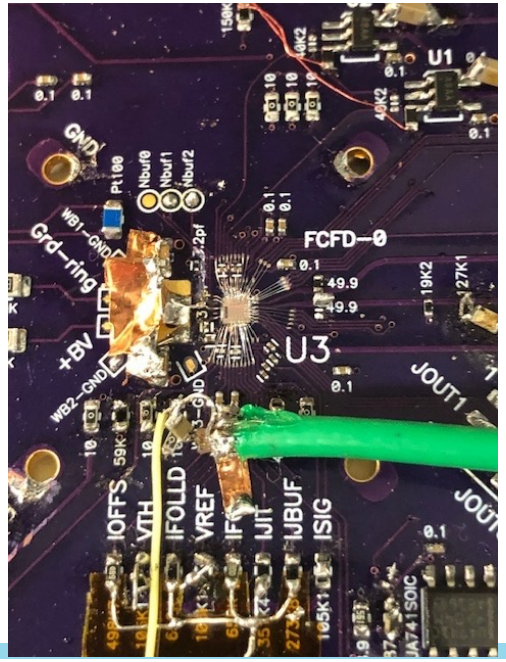
- First version of the chip to test and study the approach
  - Only analog output to measure the performance of the CFD approach
  - Measurements first performed using the internal charge injection circuit

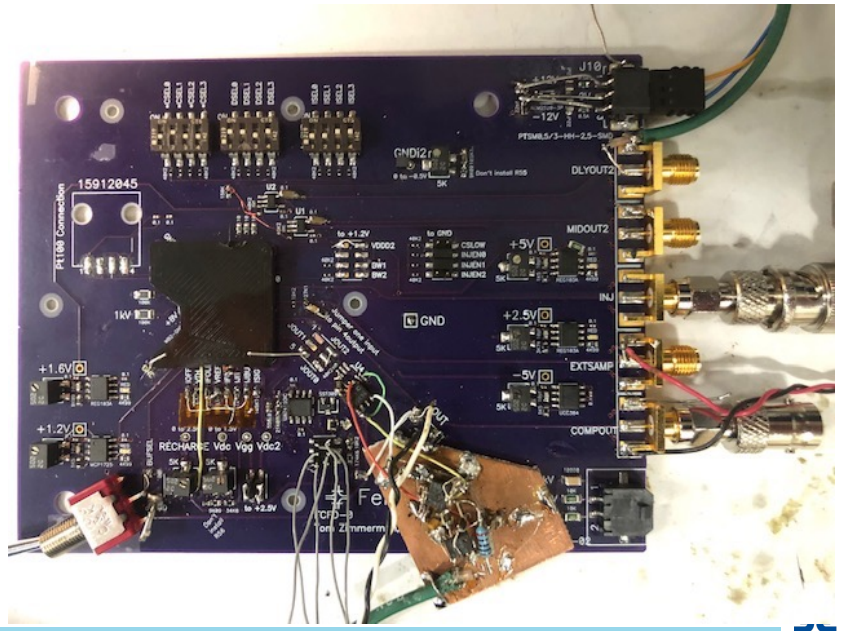




Testing with LGAD signals

- Characterization of FCFDv0 with beta source and test beam
  - Designed dedicated board for measurements with LGADs
  - On-board regulators for charge injection, switch ON/OFF analog buffers
  - SMA-output of the comparator and analog buffer
- Wirebond LGAD sensor of CMS-size pixels (1.3x1.3 mm^2)





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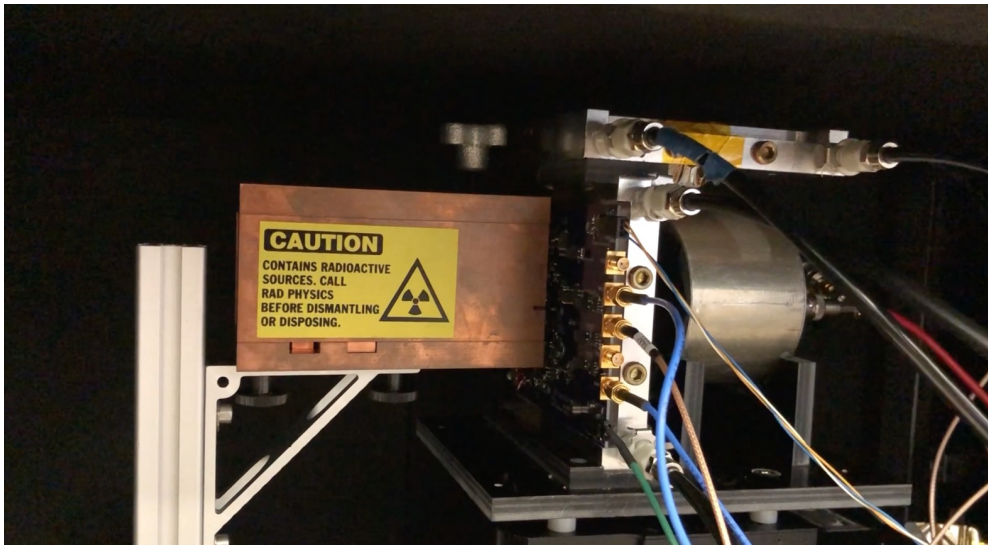
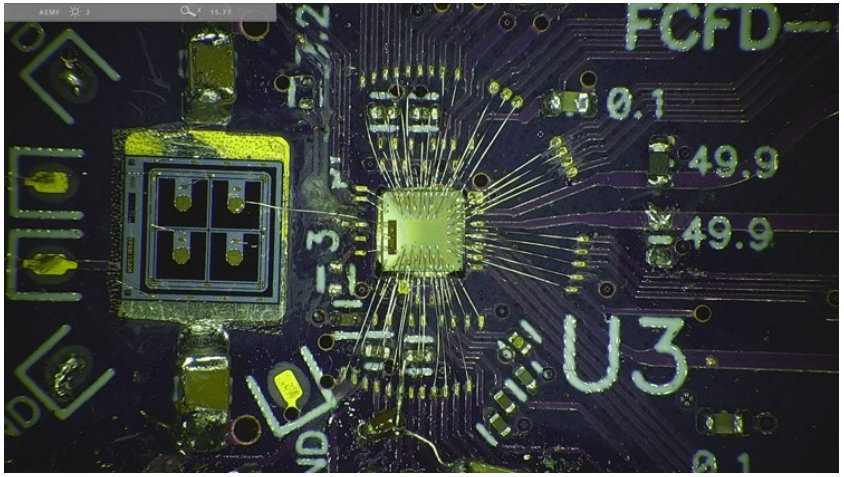
Beta-testing setup

- Board with sensor mounted inside environmental chamber in SiDet
- Tests have been performed with laser and beta-source,
  - Will be tested in beams during this week



Board mounted with β-source



FCFD0 chip mounted to LGAD

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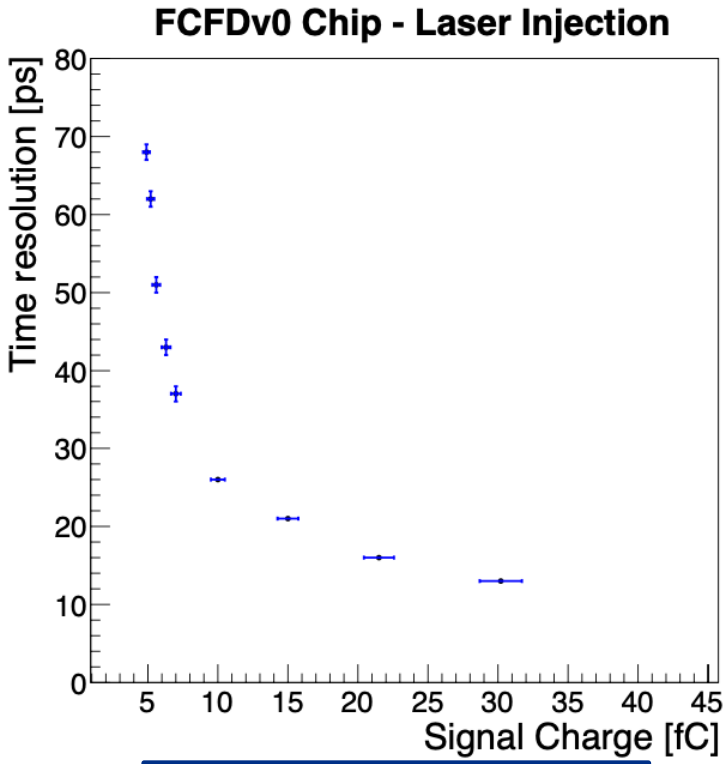
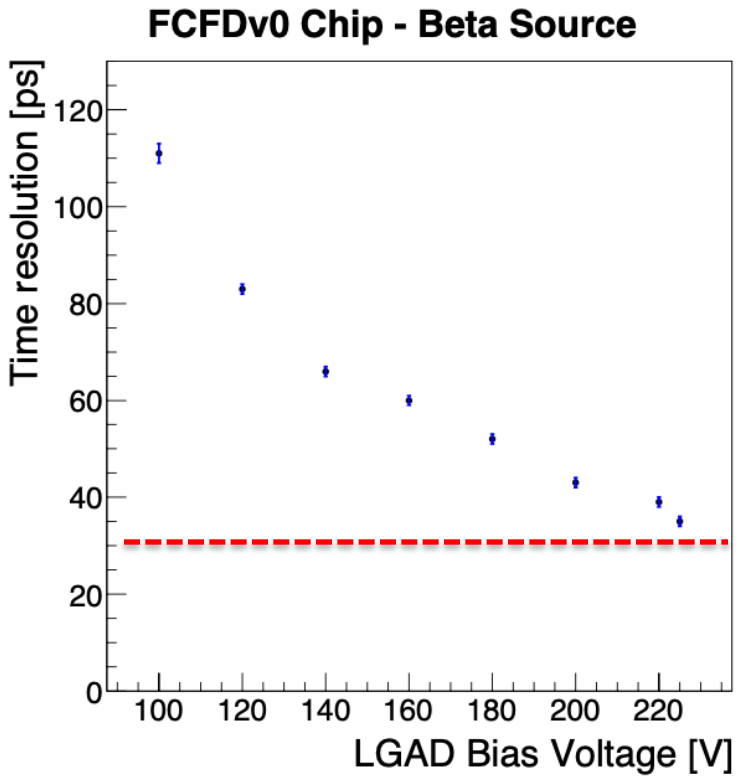
Timing ASIC with CFD

- Measurements with laser and beta-source confirm the excellent expected time resolution



Time resolution with 1.3x1.3 mm^2 LGAD sensor



Time resolution with 1.3x1.3 mm^2 LGAD sensor

Development plans for 2023

- Develop the next version targeting EIC AC-LGADs
  - Focus on AC-LGAD readout which needs both amplitude and timing information from each channel
  - Extended dynamic range for readout of smaller signals from AC-LGAD
  - Multichannel chip for AC-LGAD strip detector, 10 channels
  - Analog readout, and the ADC one one of the channels
- Preliminary specs from our test-beam studies of AC-LGADs
  - AC-LGADs with 500 µm pitch and 1.0 cm length of strips
  - Details have been presented in previous eRD112 meetings
- Will also develop the readout board to wire-bond to AC-LGAD sensors
  - To be used for measurements with laser, source and beams

Timeline and milestones in 2023

- Finish the design in Spring 2023
  - Contacted CERN IMEC representative to start schedule submission
- Receive back from TSMC: Summer 2023
  - After the chip is submitted, design and submit the readout board for testing the ASIC coupled with AC-LGAD strip sensors
- Testing of FCFDv1
  - Initial bench testing with charge injection: late Summer 2023
  - Testing with beta-source and laser: Fall 2023
  - Test-beam once Fermilab Test Beam comes online: Fall-Winter 2023

Developments in 2024 and 2025

- After the successful demonstration of the system readout with a 10-channel system during FY23
  - In 2024 focus on the full chip: full-size FCFDv2
    - If the sensor geometry is not finalized yet, we could target a scaled-down version to demonstrate the rest of the system.
    - Complete system including the digital readout that would interface with the EIC experimental DAQ
- The final, mixed-signal ASIC will be produced and tested during FY25, and its performance will be characterized using a single-layer AC-LGAD demonstrator at FTBF.