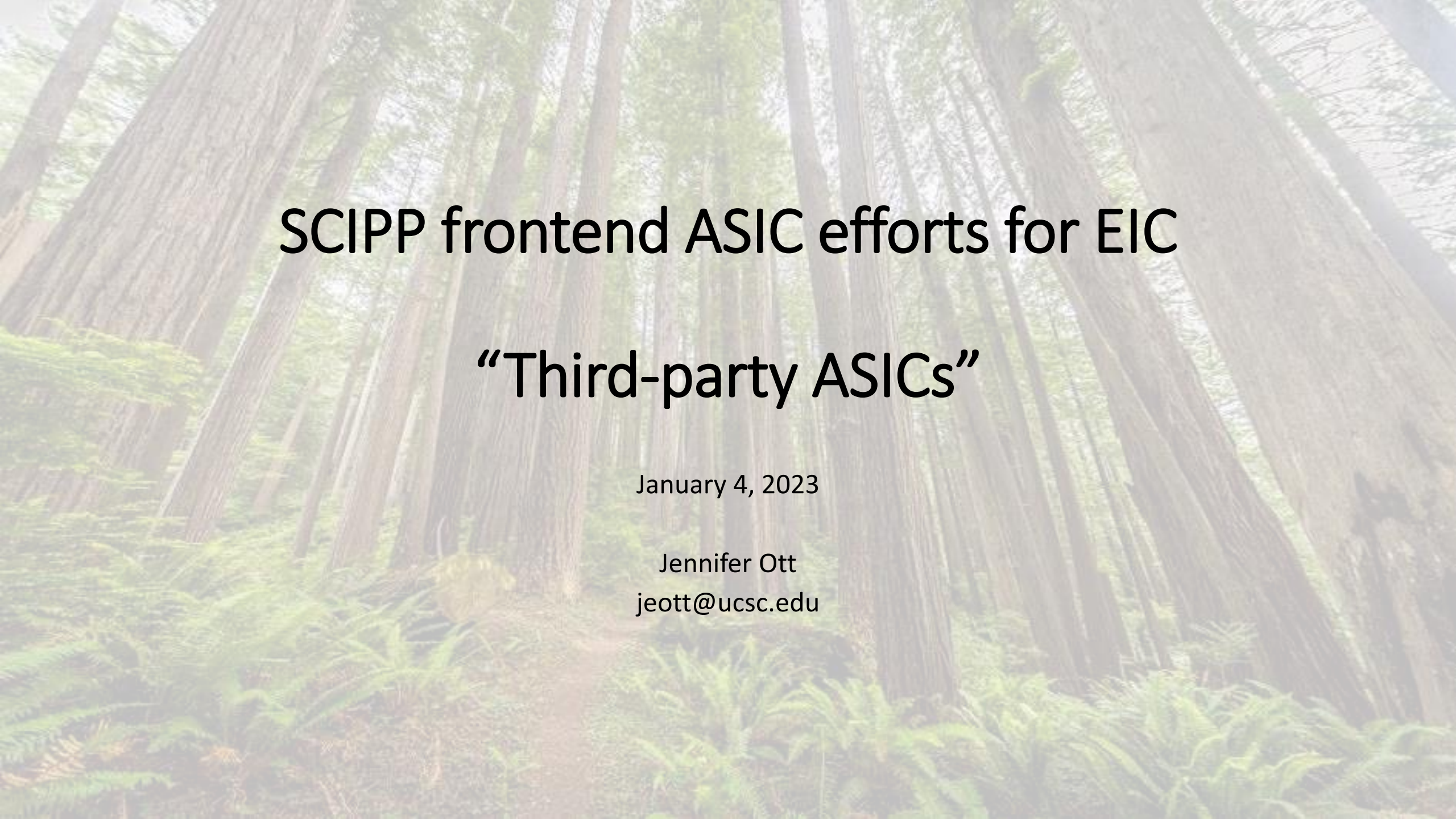

SCIPP frontend ASIC efforts for EIC

“Third-party ASICs”

January 4, 2023

Jennifer Ott
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Team at SCIPP

- Simone Mazza (staff scientist)
- Jennifer Ott (postdoc)
- Matthew Gignac (asst. faculty)
- Bruce Schumm (faculty)
- K.-W. Taylor Shin (electronic engineer / senior specialist)
- Max Wilder (electronic specialist)
- Noah Nagel (junior specialist)
- Undergraduate students
- *Abe Seiden (faculty emeritus)*
- *Hartmut Sadrozinski (adj. faculty emeritus)*

SCIPP activities overview

"In collaboration with two small electronics firms, SCIPP is currently a driving force in the development of two complementary approaches to LGAD readout. These include the CMOS-based HPSoC precision-timing "system on chip" development (Nalu Scientific) and the SiGe-based low-power ASROC front-end development (Anadyne, Inc.), both described above. We plan to continue our collaborative work with these two companies. For the case of HPSoC, characterization data accumulated for the initial five-channel prototype has allowed Nalu to begin, under our continued guidance, the refinement of the front-end design to meet the emerging goals of the EIC Detector effort. Support from this source, coupled with that expected from other sources, should allow the HPSoC collaboration to produce and characterize a second, more optimized prototype with a 10 Gs/s back-end digitizer. For the case of the ASROC effort, the FY23 will be expected to produce and characterize the first prototype of a 16-channel SiGe-based front-end amplifier ASIC geared towards the specific design goals of EIC LGAD sensors. SCIPP will also continue to collaborate with INFN Torino for the characterization of the FAST family of chips of which a new version is expected soon."

From the eRD112/eRD109 FY2023 proposal

4.2.3 SCIPP

Workforce at SCIPP on EPIC: 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, 8 undergrad students. Given the involvement of SCIPP both in the sensor and ASIC development a support in both. The total budget amount requested by SCIPP is 100 k$ split evenly between the two efforts, Tab. 19 contains the breakdown of the budget allocation at SCIPP.

Resource	Task	FTE (%)	Budget (k$)
Electronic Design Specialist	Service board design and layou	7.5	12.4
Electro-Mechanical Engineer	Board Assembly	5	11.8
Assistant specialist	Board loading and lab msmt	5	5.5
Materials and Supplies	ASIC service boards	-	3.3
Total	-	-	**33**

Table 19: eRD109 SCIPP budget request for FY23 on frontend ASIC R&D. All entries in thousands of dollars.

Only referring to frontend ASIC-related section – work on sensors comes in addition

SCIPP activities overview

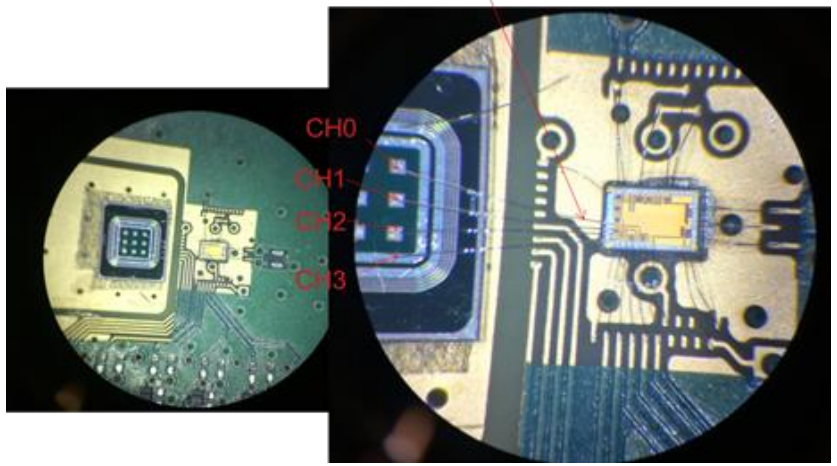
- Guidance on ASIC requirements for companies, active communication and collaboration on chip design
- Design and assembly of service and readout boards
- Characterization of ASICs
- Bonding of ASICs to relevant sensors, testing of sensor-ASIC system with signals from laser, alpha, beta particles

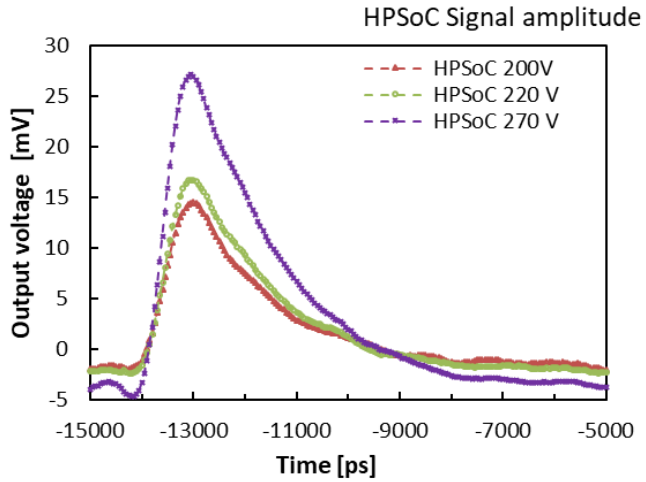
➢ $ 33k in EIC eRD funds: envisioned project distribution over FY2023 as shown below, details for each frontend ASIC in the following slides

ASIC	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
Nalu												
ASROC												
FAST3												

HP-SoC / HD-SoC (Nalu Scientific LLC)

- 65 nm CMOS, aimed at waveform digitization
- First 4-ch prototype developed, fabricated and tested through SBIR Phase-1 funding
- Emphasis on characterization of first-stage transimpedance amplifier with LGAD sensors



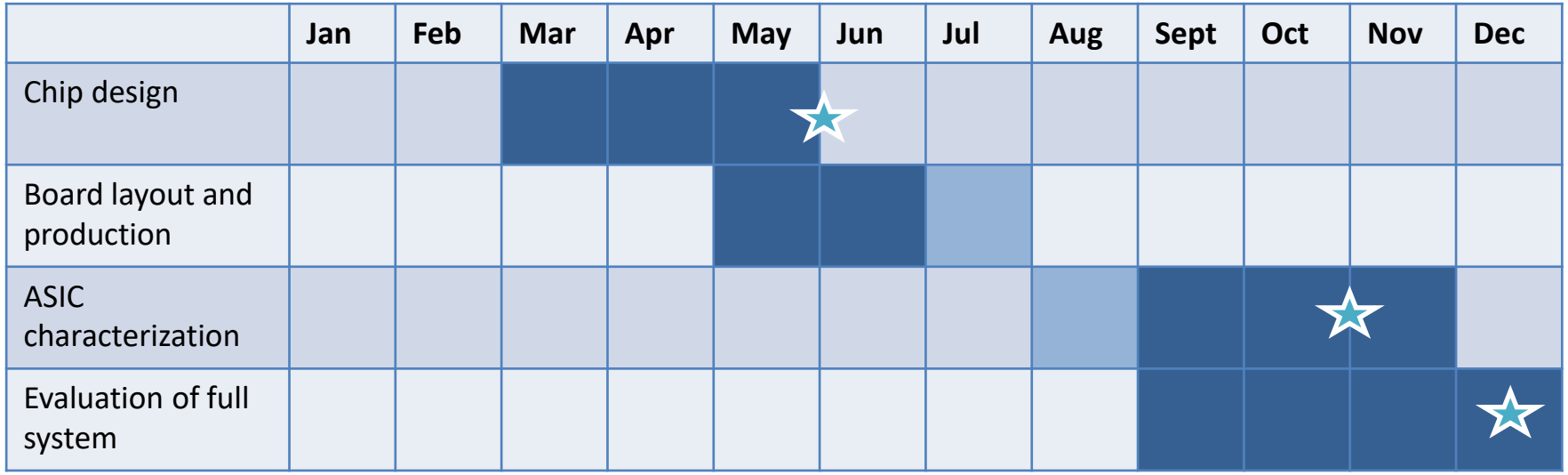


TWEPP 2022: https://indico.cern.ch/event/1127562/contributions/4904727/

https://arxiv.org/abs/2210.09555v2

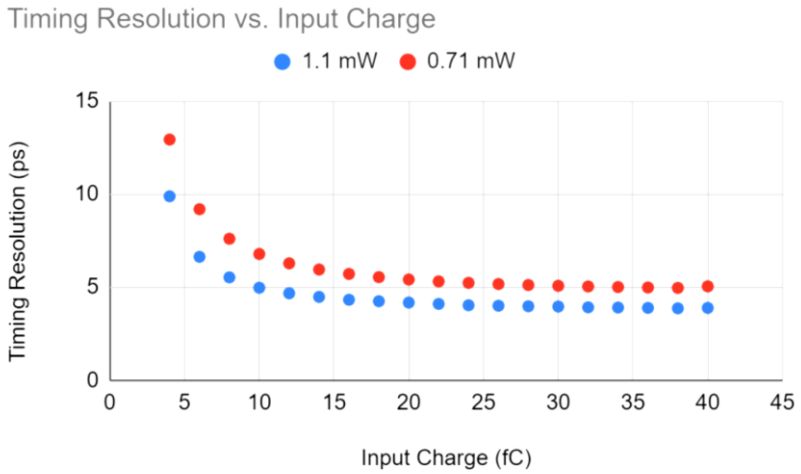
HP-SoC / HD-SoC (Nalu Scientific LLC)

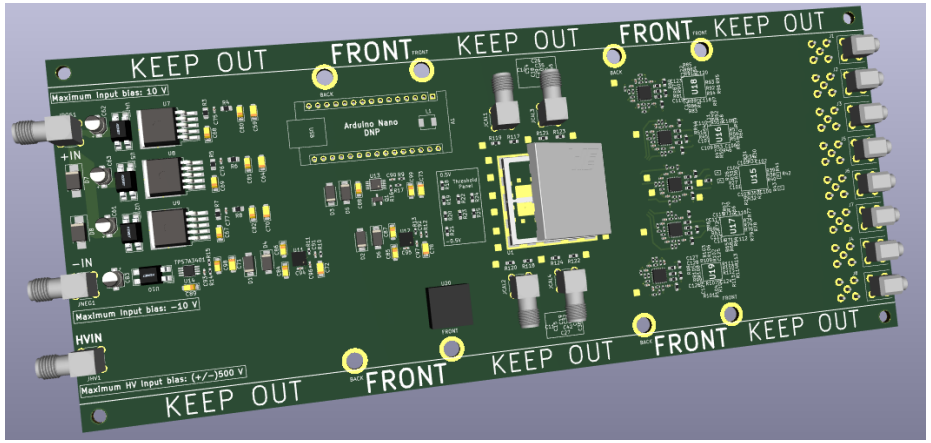
- Prototype 2: improved first amplification stage, waveform digitization at 10 GS/s, independent operability of multiple channels
- Partly funded by JLab EIC funding (primarily design and production costs of Nalu)
- SCIPP:
  - $ **Electronic engineer, specialist(s)**
  - $ Production of readout PCB
- Milestones:
  - Submission of HP-SoC prototype 2 chip
  - Characterization of TIA stage and signal properties on channel level
  - Full waveform digitization, on 4 channels



ASROC (Anadyne Inc)

- 16-ch SiGe BiCMOS analog (discriminator) chip, developed under SBIR Phase-1 funding
- Focus on low power consumption (0.7-1.1 mW/channel) and noise
- ROC design finalized, tapeout: Dec 2022





TWEPP2021:https://indico.cern.ch/event/1019078/contributions/4444426/

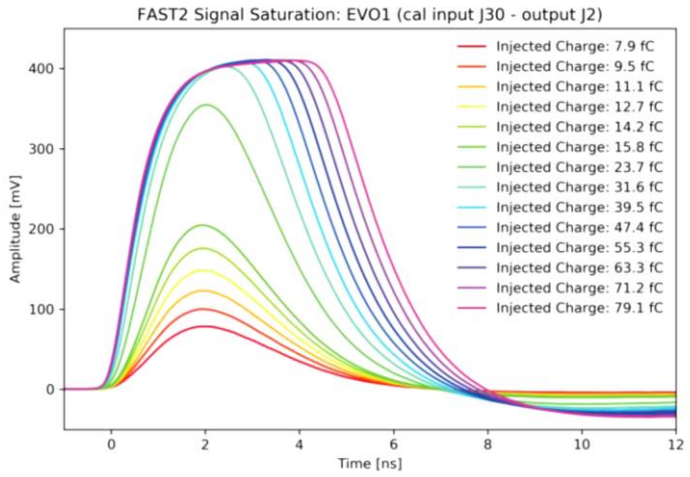
ASROC (Anadyne Inc)

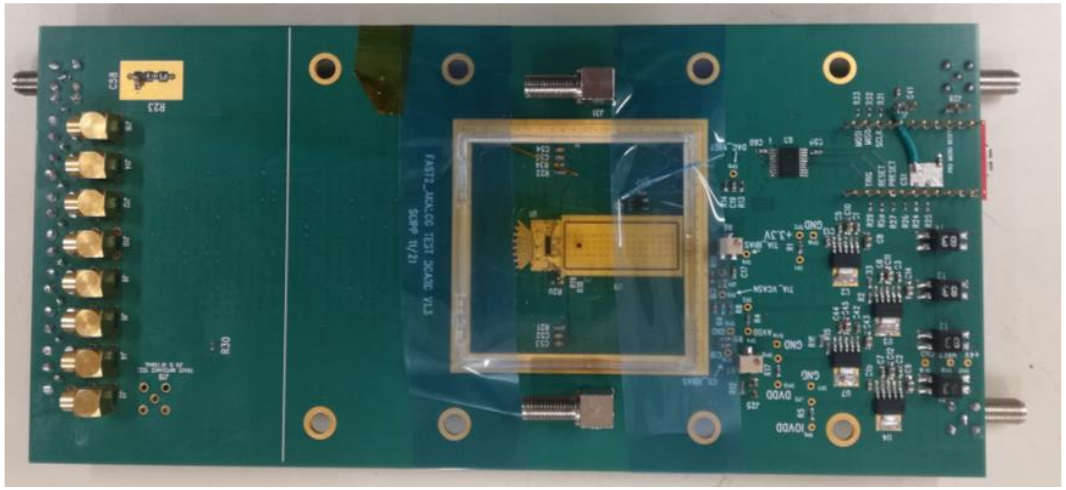
- ROC design finalized, tapeout: Dec 2022
- Development of readout board ongoing, estimated finish Feb 2023
- SCIPP:
  - $ **Electronic engineer, specialist(s)**
  - $ **Production of readout PCB**
- Milestones:
  - Complete first electrical tests with ASROC
  - Evaluation of ASIC in both power modes, with multiple channels bonded to sensor and read out

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
Board layout and production												
Initial ASIC testing							☆					
Full ASIC characterization								☆				

FAST (INFN Torino)

- Good contacts with University and INFN Torino through fast sensors R&D
- FAST ASIC family: 110 nm CMOS, 16-(20)-ch discriminator & TDC
- Programmable high- and low-gain stages; longer rise and fall time
- FAST and FAST2 analog chips have been tested at SCIPP with different signal polarities and injected charge
- Custom readout board developed for FAST2





E.J. Olave et al (FAST): https://www.openaccessrepository.it/record/74450#.Y7WoDRXMJPZ
A. Martinez Rojas et al (FAST2): https://ieeexplore.ieee.org/document/9875441

FAST3 (INFN Torino)

- New designs for input bias cell, analog output buffer, pulse width regulator; several test versions (analog and digital) produced
- SCIPP:
- Custom readout board developed for FAST2: can be used with no or minimal adaptations for next generation – FAST3
  - $ (Modification) Production of readout boards
  - $ **Junior specialist or student(s)**
- Milestones:
  - Testing of FAST3, comparison of performance to FAST2 and other ASICs

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
Board layout and production												
Testing												
Results evaluation					☆							

Summary of costs / budget, distribution

- PCB production and population: 3.3 k$
- 7.5 % / 5 % FTE electronic engineer / senior specialist
- 5 % FTE junior specialist

- FAST and corresponding readout board is the most mature technology: can rely more on students and junior specialist
- ASROC and HP-SoC require electronic engineer for board design; testing will be lead by staff scientist and postdoc