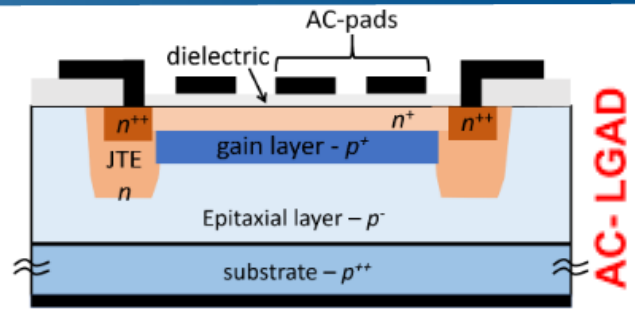
Front-End ASICs to read-out AC-LGAD sensors: status and plan

Dominique Marchand (IJCLab, Orsay, France)

on behalf of teams involved in ASIC development and characterization for ePIC detectors

OUTLINE

Objective: **ASIC design and characterization**
dedicated to the read-out of **AC-LGAD**
(Low-Gain Avalanche Diode) silicon sensors



4D reconstruction (timing & position)

Central **T**racking & **T**iming **L**ayer (Barrel TOF): AC-LGAD **strips** (reduced number of # to lower power)
(Far)-Forward detectors (TOF & Roman Pots): **pixelated** AC-LGAD (0.5 x 0.5 mm^2)

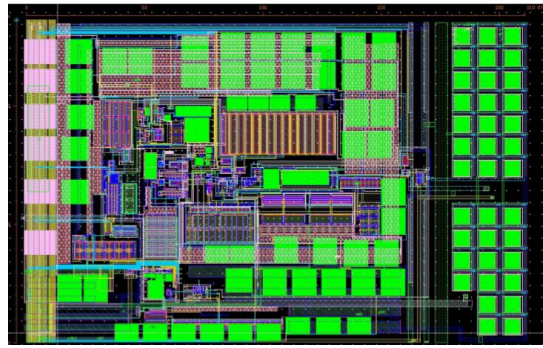
- **FCFD (FermiLab) ⇨ AC-LGAD strips**
- **Univ. of California Santa Cruz / SCIPP: HP-SoC, ASROC, FAST**
- **EICROC (French collaboration + BNL)**
- **Summary**

FCFD: Forward Constant Fraction Discriminator

From Artur Apresyan (FermiLab)

Goals:

- Develop a robust fast-timing measurement technique for fast detector
- 30 ps time resolution or better
- easy to use & stable: no corrections, no calibration or threshold adjustement
- very low dead time after a hit (< 25 ns)
- complete testatbility with simple bench-top equipment



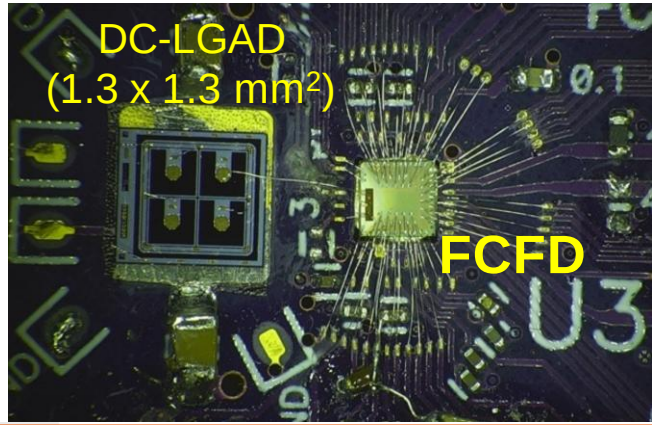
✸« A simulation model of front-end electronics for high precision timing measurements with LGAD », C. Peña *et al.,* NIM A 940 (2019) 119.

⇔ Comparison Leading edge // Constant Fraction Discriminators

FCFDv0 (TSMC 65 nm CMOS technology)

1 single channel, **only analog blocks** to test CFD approach

- Chip performance characterization with internal charge injection circuit
  Jitter: ~30 ps (5 fC); < 10 ps (30 fC)
- + DC-LGAD (CMS-size pixel:1.3 x 1.3 mm^2) 1 # wire-bonded
  IR Laser, Beta source ⇨ confirmation of excellent time resolution:
- ~30 ps (LGAD Bias voltage 220 V, Beta source)
- *measurements in beams will follow*



FCFD: FY23 plan

From Artur Apresyan

FCFDv1 (TSMC 65 nm CMOS technology)

10 channels, **only analog blocks** to test CFD approach

- Chip performance characterization with internal charge injection circuit
  Jitter: ~30 ps (5 fC); < 10 ps (30 fC)
- + DC-LGAD (CMS-size pixel:1.3 x 1.3 mm^2) 1 # wire-bonded
  IR Laser, Beta source ⇨ confirmation of excellent time resolution:
- ~30 ps (LGAD Bias voltage 220 V, Beta source)
- *measurements in beams will follow*

A. Apresyan presentations at eRD112 meetings:

https://indico.bnl.gov/event/17999/ (01/04/23)

https://indico.bnl.gov/event/17084/ (09/14/22)

UCSC/SCIPP effort: 3rd party ASIC characterization

Lead institution	Name	Tech	Output	n channels	Funding
INFN Torino	FAST	110 nm CMOS	TDC	20	INFN
NALU Sci.	HPSoC	65 nm CMOS	Waveform	5 ($\geq$ 81 final)	DoE SBIR
Anadyne Inc.	ASROC	SiGe BiCMOS	Discrim.	16	DoE SBIR

Name	Specific goal	Status
FAST	Large cap TDC	Testing, new version soon
HPSoC	Max timing precision, digital back-end	Testing
ASROC	Max timing precision, low power	Simulations finalized, Layout board

From Jennifer Ott (UCSC/SCIPP)

Presentation at the eRD112 Jan. 4th '23 meeting: https://indico.bnl.gov/event/17999/

SCIPP effort: FY23 plan

EICROC effort

2021-2022 funding

Objective: Development of an **ASIC prototype**
EICROC0
able to readout a new generation of silicon sensors:
AC-LGAD
(Low-Gain Avalanche Diode)
for the **Electron Ion Collider** (EIC) **Roman Pots**

Organization for Micro-Electronics desiGn and Applications, Ecole Polytechnique, Palaiseau

CEA Saclay/Irfu/
Département d'Electronique des Détecteurs et d'Informatique pour la Physique (DEDIP)

eRD112 AC-LGAD: weekly meetings

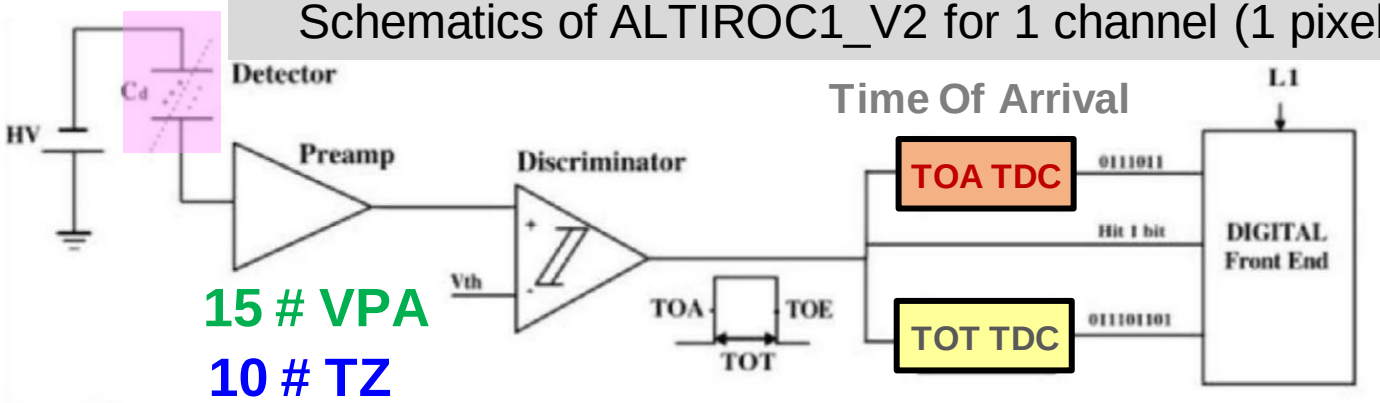
ATLAS/HGTD (High Granularity Timing Detector): ALTIROC ASIC

ALTIROC: **A**TLAS **L**GAD **T**iming **I**ntegrated **R**ead **O**ut **C**hip
[technology **CMOS 130 nm** (TSMC)]

designed and characterized by OMEGA and IJCLab

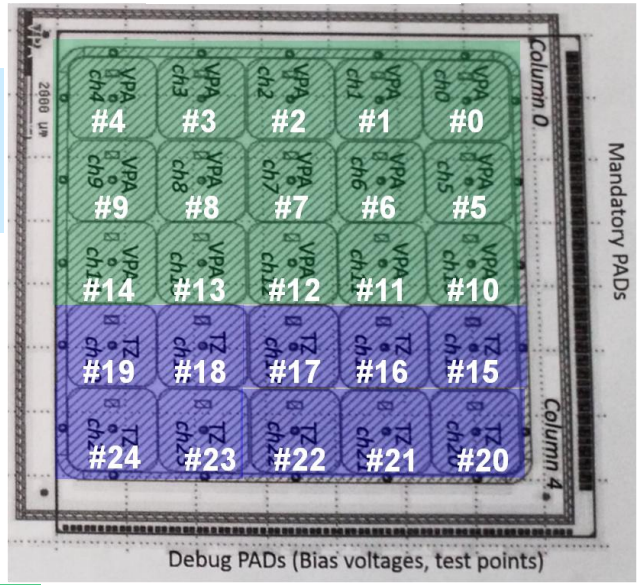
ALTIROC0/1: Existing ASICs designed to read DC-LGAD (1.3 x 1.3 mm2)
Achieved goal ~30 ps time resolution
ALTIROC3 (full size: 225 channels)

Schematics of ALTIROC1_V2 for 1 channel (1 pixel)



(TDC: Time-to-Digital Converter)

ALTIROC1_V2 channel mapping
(25 channels)



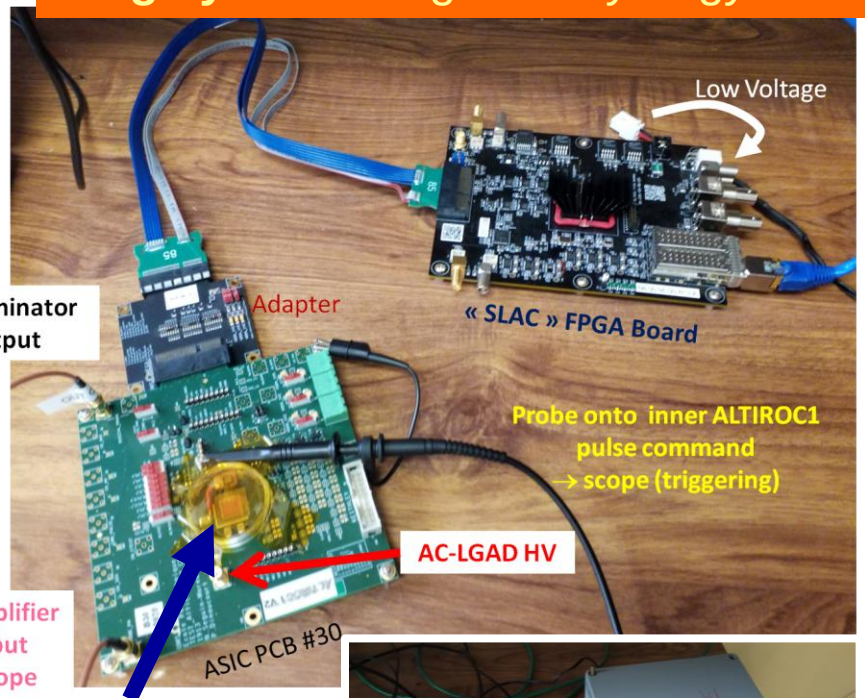
\# **Voltage PreAmplifier (VPA)**

\# **TransImpedance PreAmplifier (TZ)**

"Performance of the Front ASIC for picosecond precision time measurements with LGAD sensors", C. Agapopoulou, C. La Taille, L. Serin *et al.*, JINST, 2020, 15 (07), pp.P07007.

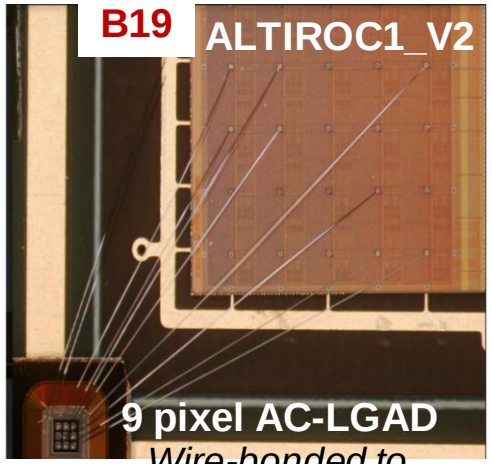
ATLAS/HGTD test bench: ALTIROC1 + AC-LGAD (3x3 pixels)

Largely benefitting from synergy with ATLAS/HGTD IJCLab team: expertise and testbench setup



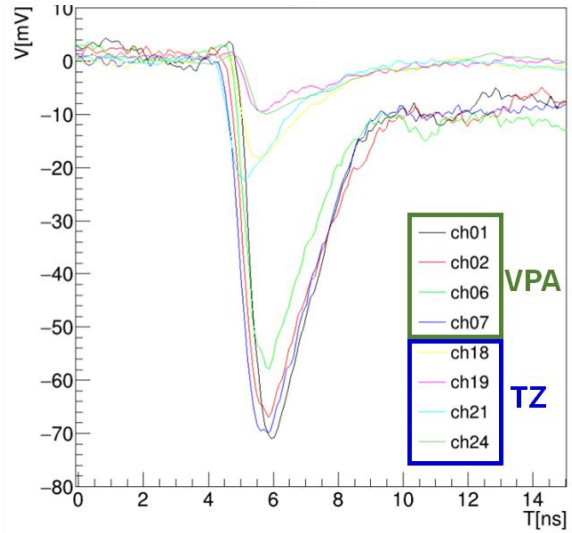
AC-LGAD prototype wire-bonded to ALTIROC1_V2 by **BNL team**

Sept. ’21 - Jan. ‘22



Wire-bonded to ALTIROC1 by BNL

HV: -160V (I ~68nA), DAC Pulser ~ 8 fC



- Corrected LSB (Least Significant Bit) for each TDC channel is ~30 ps
- The average jitter for each channel is ~15-20 ps
- Connected TDC channel performances uniform
- Study of PA amplitudes versus injected charge
- Lowest detectable charge 2.5 fC

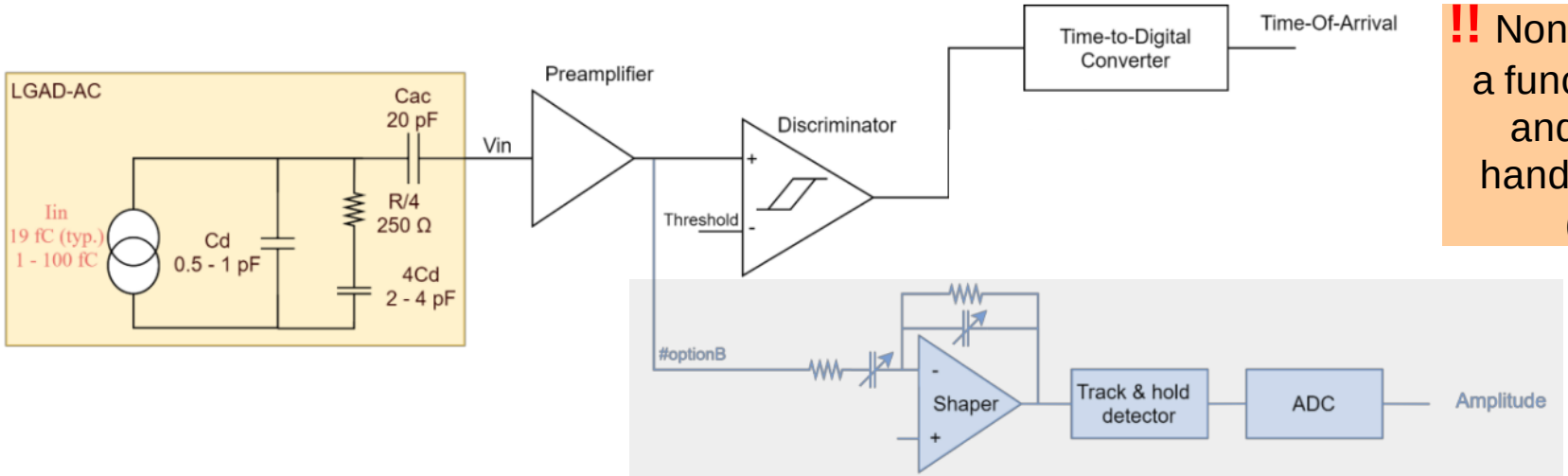
EICROC0 design: 16 channels (4x4)

Requirements:
- pixel size **0.5 x 0.5 mm²** (HGTD 1.3x1.3 mm²)
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- **sensitivity to low charge (2 fC)**

Charge sharing studies (simulation + β source)

EICROC0 design:
- TZ Preamplifiers from ALTIROC (ATLAS/HGTD, OMEGA)
- TDC from HGCROC (CMS/HGCal, CEA/Irfu/DEDIP)
- 8 bit ADC for time-walk correction (AGH Krakow, adapted from HGCROC)

Schematic for 1 channel (1 pixel)



!! Non-linear behavior of **TOT** as a function of deposited charge and low discri threshold to handle small energy deposits (neighboring pixels)

Time-walk correction:
amplitudes
of **central hit pixel**
+ neighboring pixels required

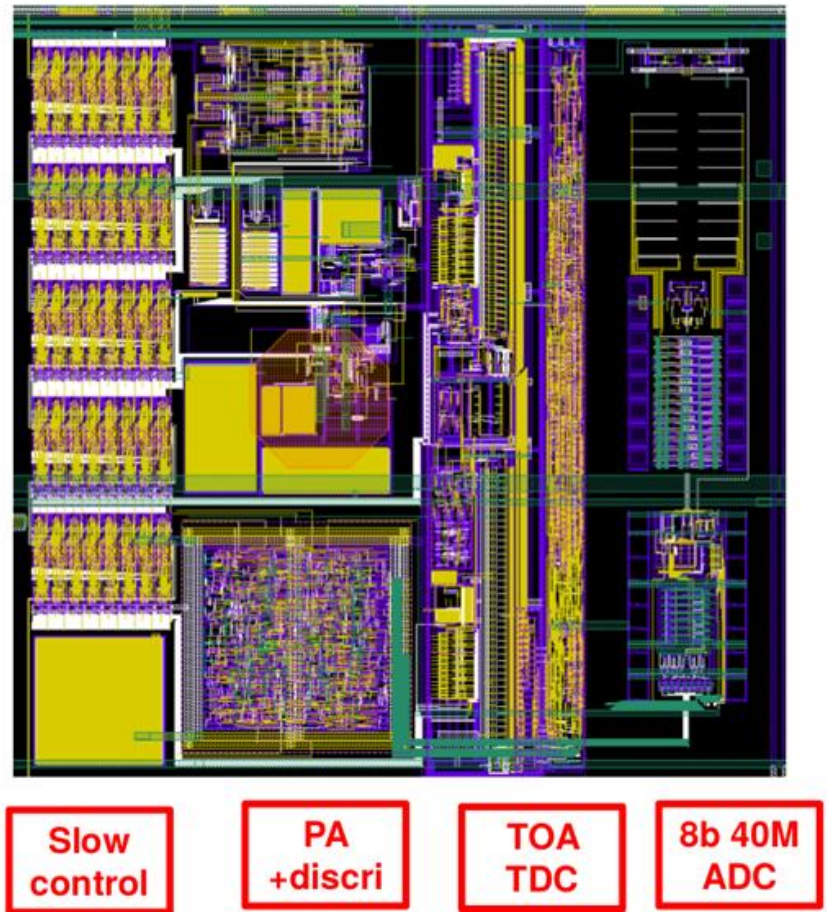
ADC: next EICROC iteration will include a lower power consumption ADC (~1 mW/channel) designed at **IJCLab**

EICROC0: 1 pad (500 x 500 µm²) overview

- High speed TZ PA and discriminator (from ALTIROC)
- I²C slow control (from CMS HGCROC)
- 8 bits 40 MHz ADC (adapted from HGCROC 10 bits ADC M. Idzik *et al.*, AGH Krakow)
- Digital readout FIFO (depth 8, 200 ns)
- 10 bits **TDC** (TOA) designed by **CEA Irfu/DEDIP**:
  HGCROC TDC (1 mm x 120 µm):
  - spatially adapted to fit in a pixel of 0.5 x 0.5 mm²
  - optimization in terms of dynamic range and resolution (10 ps rms) as well as power consumption
  - common block for calibration of all TDC channels

✸ <u>5 slow control bytes/pixel:</u>
- 6 bits local threshold
- 6 bits ADC pedestal
- 16 TDC calibration bits
- Various on/off and probes

EICROC0 layout (1 pad = 1 channel)

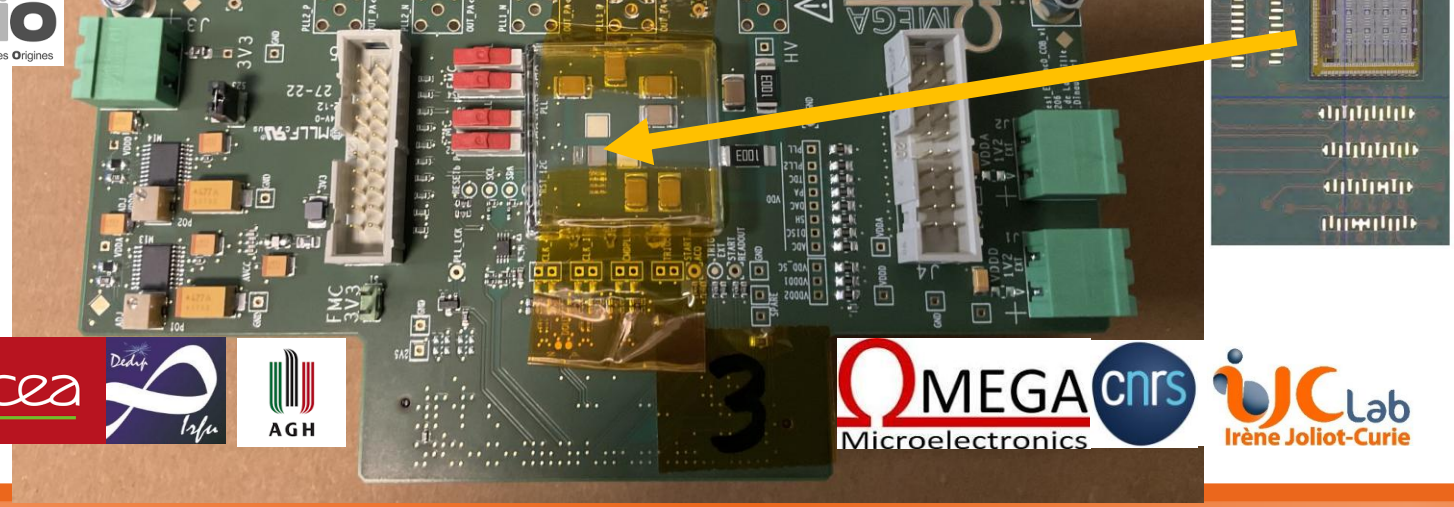


EICROC0: EIC 4x4 AC-LGAD readout test chip

- Submitted through a Multi Project Wafer (130 nm CMOS technology) in March ’22
  Delivered end of July ‘22
- **Test board** (PCB) designed by OMEGA, 10 pieces **delivered end of July ‘22**
  - test board cabling by IJCLab
- **Wire-bonding of EICROC0 to test boards** by BNL collaborators
- Delivery of 3 test boards to IJCLab in **Oct. ‘22**

- **Interface board** (Xilinx ZC 706): firmware / software developments (A. Ba & B.Y. Ky, IJCLab)

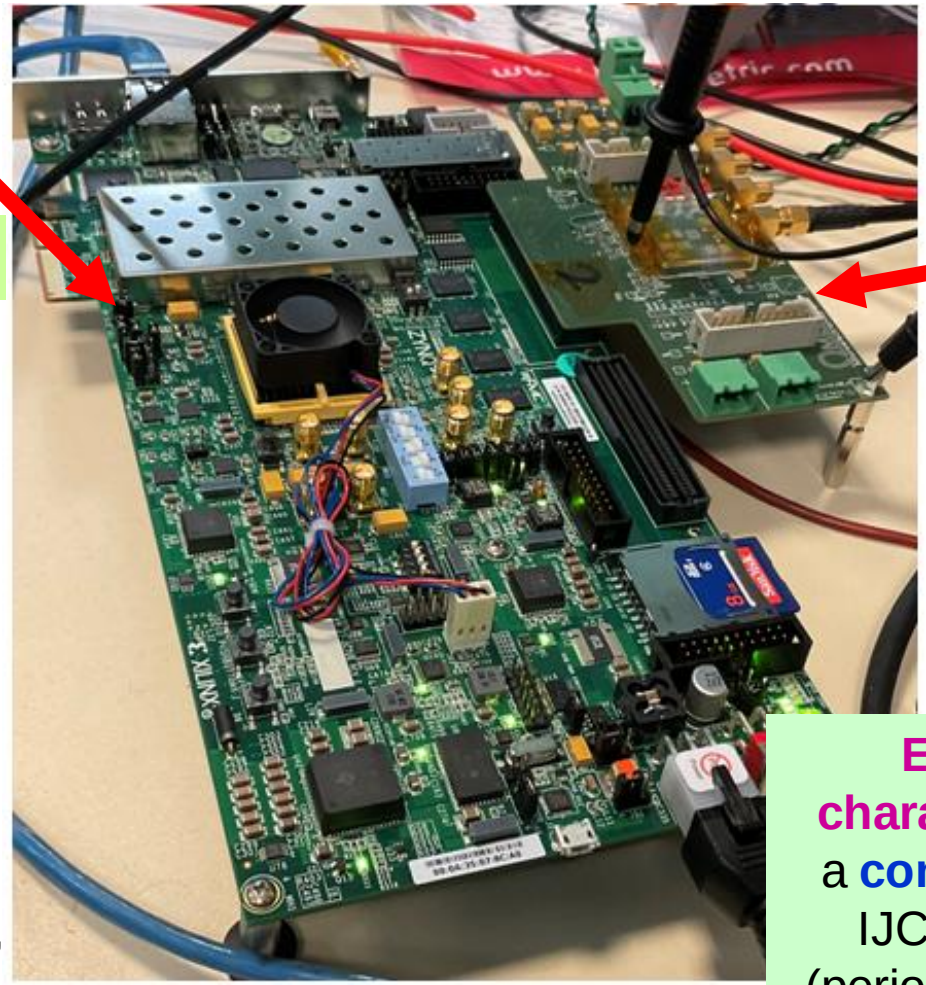
EICROC0
Test board



EICROC0 Test Bench at IJCLab

- installed in an electronic test room (IJCLab)

Interface board (Xilinx ZC 706)



EICROC0 Test board

Test bench finalization under progress

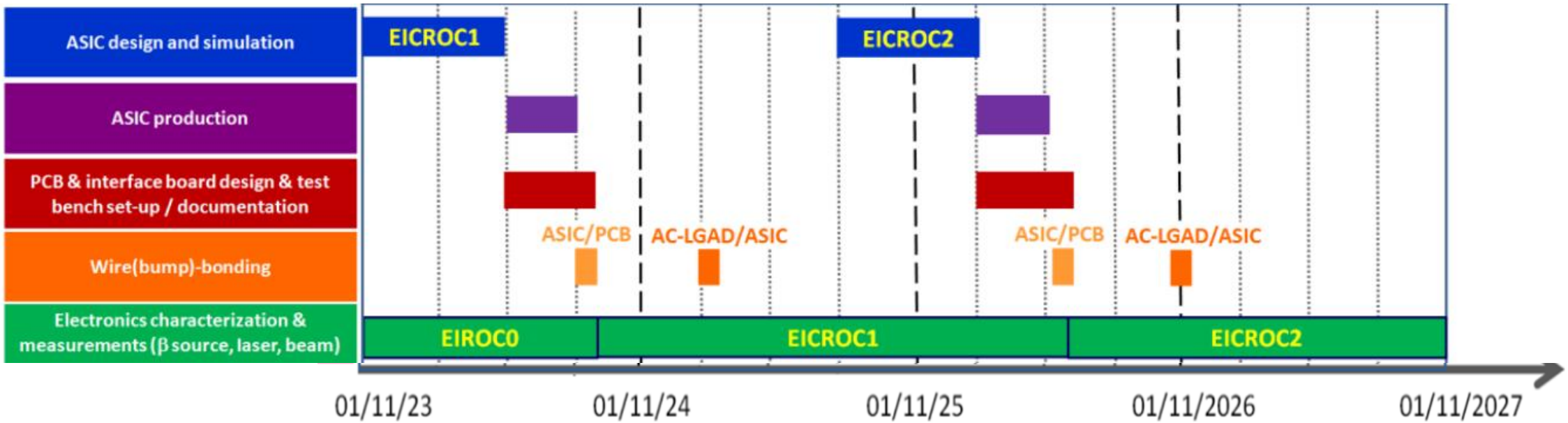
- ✓ I²C communication
- ✓ Data stream written/read
  decoding still under investigation
- ✓ EICROC0 DC levels
- ✓ Discri threshold exploration
- ✸ EICROC0 command pulse signal issue under investigation

Next step:

EICROC0 channel by channel electronic response characterization (PA, **TDC**, ADC, LSB & jitter evaluation, cross talk)

EICROC0 characterization: a **common effort** IJCLab & BNL (periodic meetings)

EICROC FY23 and beyond



- **EICROC1:** 8 (or 16) × 4 channels prototype (floor planning), **low power ADC** + **EIC clock**
- **EICROC2 full size: 32x32 channels (engineering run)**

✸ EICROC0 command pulse signal issue ⇨ time shift

⇨ **EICROC0_v1:** 4 × 4 channels prototype + **low power ADC**

ASIC + AC-LGAD characterization: IR laser test bench (IJCLab)

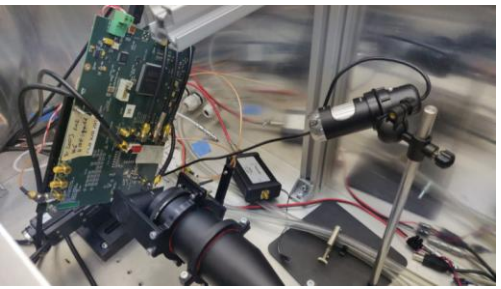
Dedicated infrared test bench setup at IJCLab:

Largely benefiting from synergies among IJCLab departments and from BNL expertise

✓ Purchase of all the required material:
- IR laser λ=1050 nm, optical fibers + splitter
- optical alignment elements: mirrors, lenses, visible/IR camera, power meter, safety equipment

Characterization of the response of ALTIROC1_V2 + AC-LGAD sensor (3x3 pixels) → signal sharing, time and space

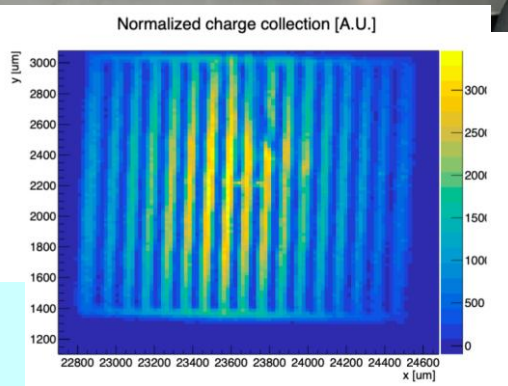
⇨ Comparison with (AC-LGAD + ALTIROC0_V2B) by BNL



arXiv:2209.07329; JINST **17** P11028 (Nov. '22)

Scanning-Transient Current Technique (TCT) using IR laser

Colour indicates integral charge of the signal peak from the ALTIROC analog output



AC-LGAD strips

Brookhaven National Laboratory

Summary

- Characterization of the system (AC-LGAD + ALTIROC1_V2) exploiting ATLAS/HGTD test bench (electronics response signal to an injected charge)
- Evaluation of the charge sharing ratio among neighboring pads / pixels:
  - measurements based on ALTIROC1 injected charge
  - measurements with a beta source
- Development of a full simulation to evaluate spatial resolution from signal sharing including digitalization in the context of a 8/10 bits ADC
  - ADC with 8 bits sufficient to achieve 20 µm spatial resolution.

Studies presented at the EIC User Group Early Career Workshop 2022, July 24-25 (CFNS Stony Brook University, USA), "Simulation and instrumentation for the Roman Pot in the future Electron-Ion Collider", Pu-Kaï Wang (PhD, IJClab)

- Design/layout of EICROC0 : submission within a MPW in March '22 (delivered July '22)
- Test board designed, manufactured (10 pieces) and cabled
- EICROC0 wire-bonded onto test boards by BNL collaborators, available at IJCLab: Oct. '22
- EICROC0 electronic test bench being finalized
- IR laser test bench close to be operational

Back-Up

Electron Ion Collider (EIC)

Unique oppotunity to access/probe/image/quantify/qualify
the **gluonic, valence and sea quark content** of hadrons (low x)

- Dynamic of quark - gluon confinement
- Nucleon detailed comprehensive 3D-tomography
- Missing gluon contribution to nucleon spin and mass

And many more!

Expression of Interest supported by French theorists and experimentalists

~ 2034
Brookhaven National Laboratory

electrons (10 - 18 GeV, **~70 %** polar.)
□ **protons** (275 GeV, **~70%** polar.)
or
□ **ions** (light - deuterium - to heavy - Au, Pb, U)

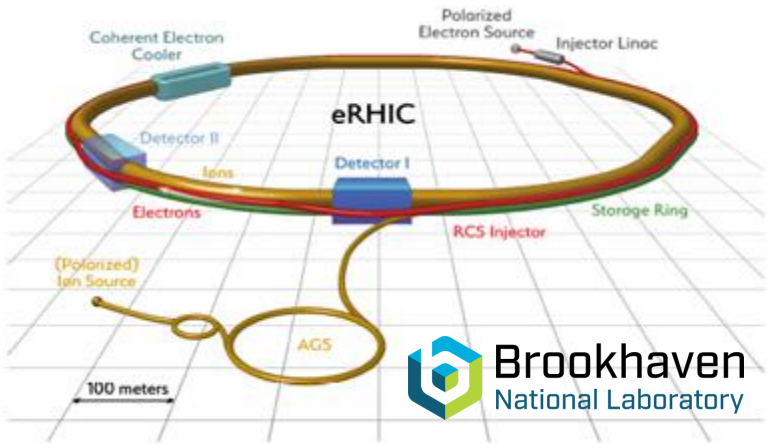
Complementarity Jlab, LHC

- ✶ Variable center-of-mass energies:
  20 - 100 GeV [140 GeV]
- ✶ High collision $\mathcal{L}$ **$10^{33\text{-}34}$** $cm^{-2}\ s^{-1}$
- ✶ **1 (2) interaction point(s)**

Our main interest:
Exclusive Reactions
(*e.g.* Deep Virtual Compton Scattering, DVCS)

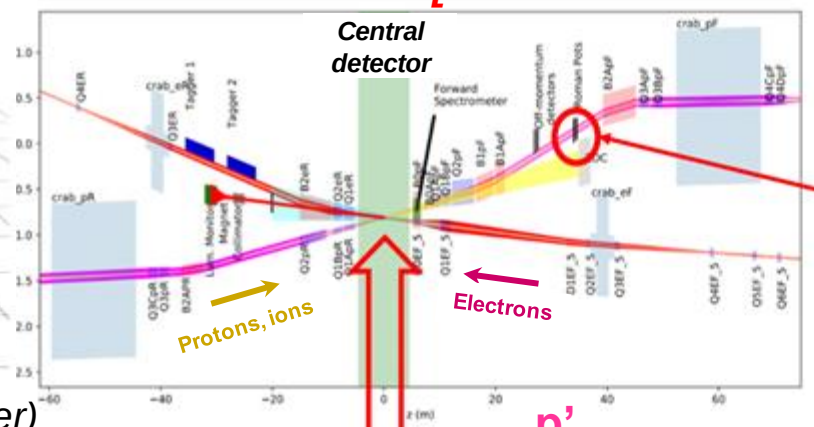
2103.05419 (March 2021)
Nucl. Phys. A 1026 (2022) 122447

electron Proton Ion Collider (ePIC) experiment: Roman Pots



Based on RHIC (Relativistic Heavy Ion Collider)

[Far-forward detectors]

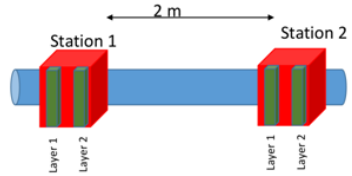


protons / ions

Momentum & Timing

Roman Pots **located ~30-40 m from IP**

2 stations of 2 layers each

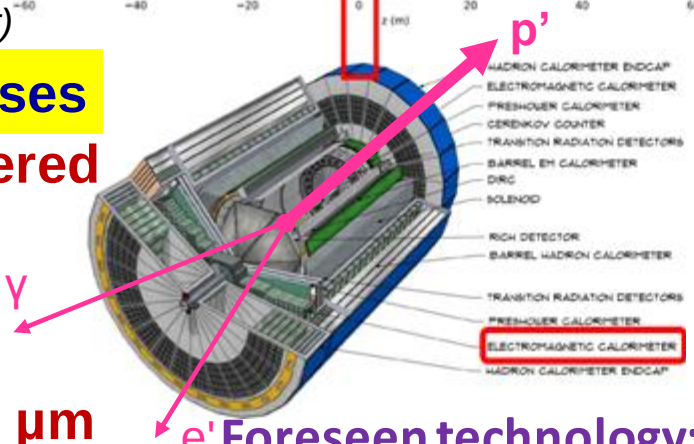


Exclusive & diffractive processes

Requirements on **forward scattered particles detection**:

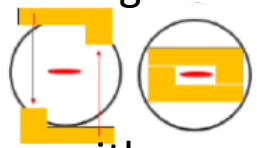
- at very small angle **< 5 mrad**
- time resolution **~30 ps**
- spatial resolution better than **50 µm**

to achieve a P_T resolution better than **10 MeV/c**



Roman Pots:

- Detector system surrounding the beam axis (a few mm)
- Placed in vacuum
- Holding silicon detectors with associated front-end electronics



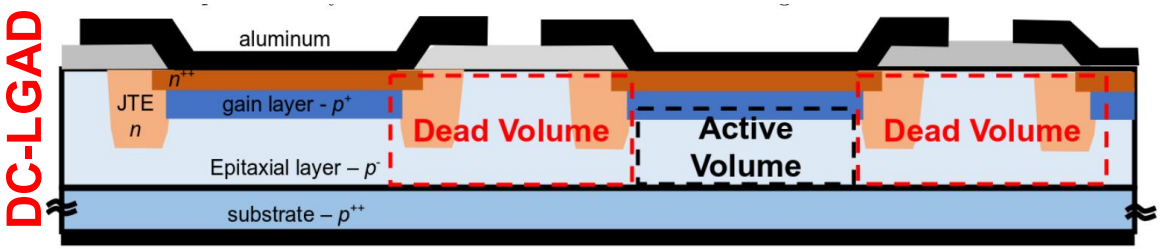
Foreseen technology: new generation of pixellated LGAD

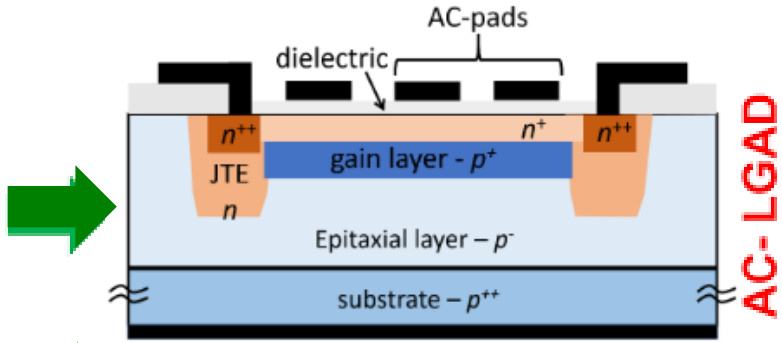
➡ **AC-LGAD**

associating good timing AND tracking capabilities

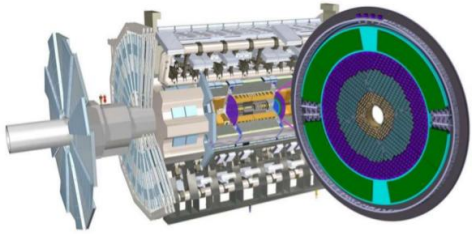
Low Gain Avalanche Diode (LGAD)

- Silicon sensors fabricated in a thin (≈50 µm) high resistive p-type substrate
- Charge gain (up to 100) to achieve very high timing resolution (20-30 ps)
- The size of the pads must be larger than the substrate thickness to achieve a uniform amplification
  → limitation for fine pixelation (< 1 x 1 mm²)





1D (timing) → **4D** reconstruction (timing & position)



ATLAS EXPERIMENT

Upgrade phase II **High Granularity Timing Detector (HGTD)**

- ➢ AC-LGAD sensors include metal electrodes placed over a thin insulating at a fine pitch, signals are induced capacitively.
- ➢ Insensitive area (edges) could be minimized
- ➢ Charge sharing → barycenter computation

- ➢ Based on pixellated **DC**-LGAD 4 x 2 cm²
- ➢ Pixel size: 1.3 x 1.3 mm²

"Fabrication and performance of AC-coupled LGADs", G. Giacomini *et al.*, JINST 14 (2019) 09, P09004,ArXiv: 1906.11542

BROOKHAVEN NATIONAL LABORATORY

The EICROC/AC-LGAD Team

- Abdourahmane Ba
- Beng Yun Ky
- Carlos Munoz Camacho
- Dominique Marchand
- Emmanuel Rauly
- Jean-Jacques Dormard
- Laurent Serin
- Ana-Sofia Torrento
- Pu-Kaï Wang

- Florent Bouyjou
- Eric Delagnes

- Christophe de la Taille
- Nathalie Seguin-Moreau
- Maxime Morenas
- Pierrick Dinaucourt

Thank you

- Alessandro Tricoli
- Gabriele Giacomini
- Gabriele D'Amen
- Enrico Rossi
- Wei Li
- Shanmuganathan Prashanth

- Weekly IJCLab meetings
- Monthly IJCLab - Irfu - OMEGA meetings
- Monthly BNL- IJCLab - Irfu - OMEGA meetings
- Weekly EIC LGAD meetings

Fruitful tight collaboration between all involved partners

The design of the first optimized ASIC (EICROC0) dedicated to AC-LGAD sensor readout funded by P2IO positioned the French community in the forefront of this promising new technology with multiple applications in particle physics and beyond.
Visible role within the EIC international community.

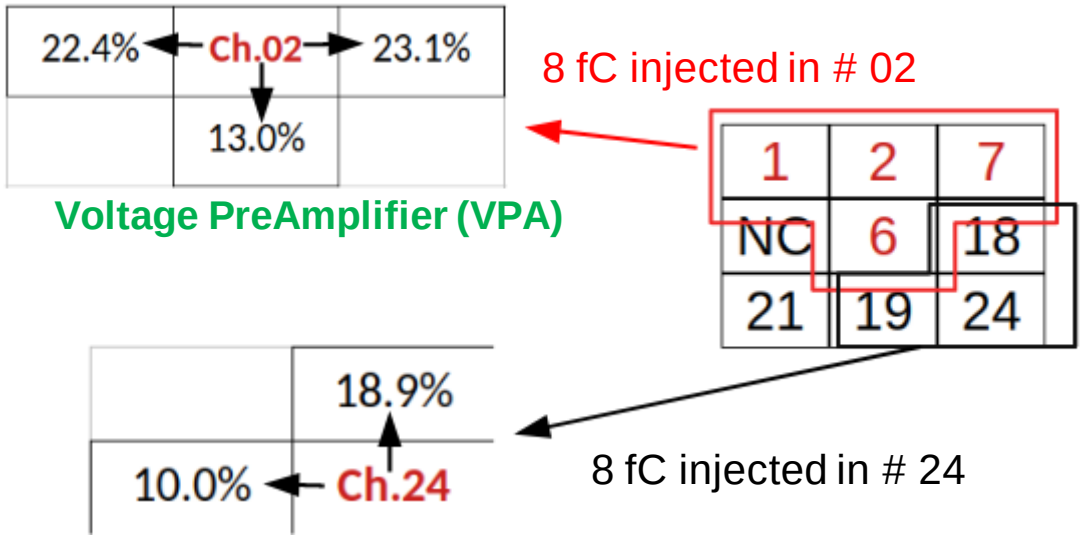
IN2P3 Scientific Council (27/10/22): *for information* « EIC Project: scientific challenges and project presentation », Carlos Muñoz Camacho (IJCLab)

- contribution to EIC AC-LGAD R&D consortium: FY2022 report & FY2023 proposal
- R&T project proposal submitted in Oct. 2022 (duration 3 years, 20 k€ / year)
- **?** 2023 ANR: submission of a pre-proposal (PRC: IJCLab, CEA Irfu/DEDIP, OMEGA, *BNL*): « CD_4D-TrACE » [Chip Design for 4D-Tracking with AC-LGAD for EIC], 4 years design of EICROC full size (32 x 32 pixels)

Studies of charge sharing: measurements

Objective: evaluation of charge sharing among adjacent pads / pixels

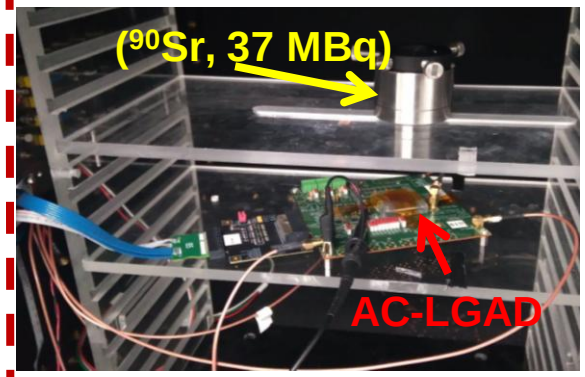
➢ Through charge injection (8 fC)



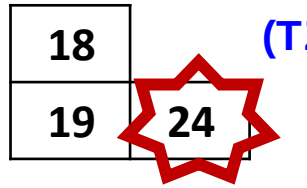
Charge sharing among neighboring pads (cross talk):
~ 15%

➢ Exposing AC-LGAD to a beta source

At IJCLab Semi-conductor and instrumentation technological platform (PSI)



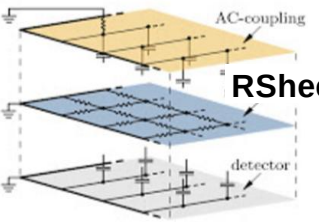
- AC-LGAD HV = -170 V
- Beta source ~5 cm above
- Whole system in black box



Charge sharing among neighboring pixels (# 18 & 19):
~30% w.r.t. # 24 (highest amplitude)
includes cross talk between pads and suffers from *ALTIROC1* TDC (TOT) discriminator signal distortion (earlier observed by ATLAS/HGTD team)

Studies of charge sharing: simulation and measurements

Synergy IJCLab ATLAS/HGTD , JLab/EIC and OMEGA teams



Objective: evaluation of achievable spatial resolution taking into account charge sharing between neighboring pads/pixels including smearing (Landau) +1-4 mV noise and considering **N**-bit ADC (**N**=4-12), P-K Wang

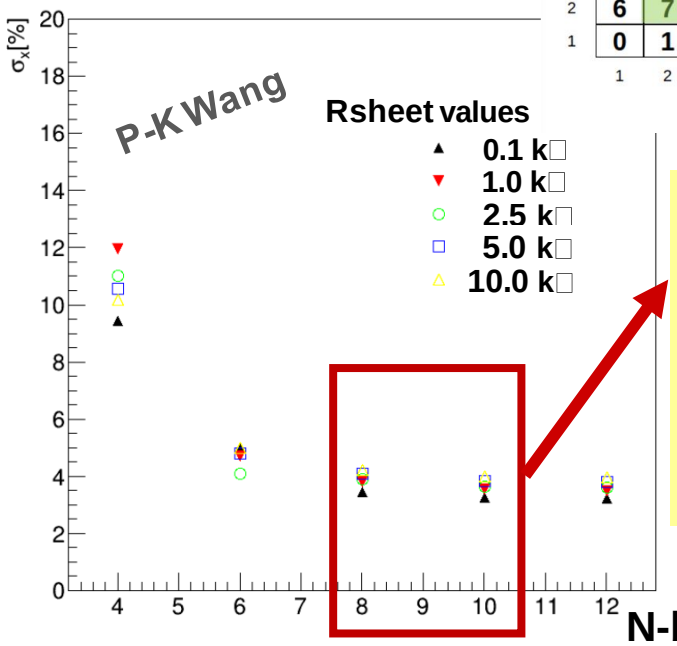
➢ Electronics Model (M. Morenas, OMEGA): 5x6 pads, TZ, several Rsheet values considered

5	24	25	26	27	28	29
4	18	19	20	21	22	23
3	12	13	14	15	16	17
2	6	7	8	9	10	11
1	0	1	2	3	4	5
	1	2	3	4	5	6

x pos

Inject E(19fC) between ch.14 & 15

2D-Representation, P-K Wang (IJCLab)



8 and 10-bits ADC

σ_x ~ 4% (pixel width=0.5 mm)

σ ~20 µm