Silicon Tracker R&D (eRD111, eRD113, generic)

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California EIC Consortium Collaboration Meeting

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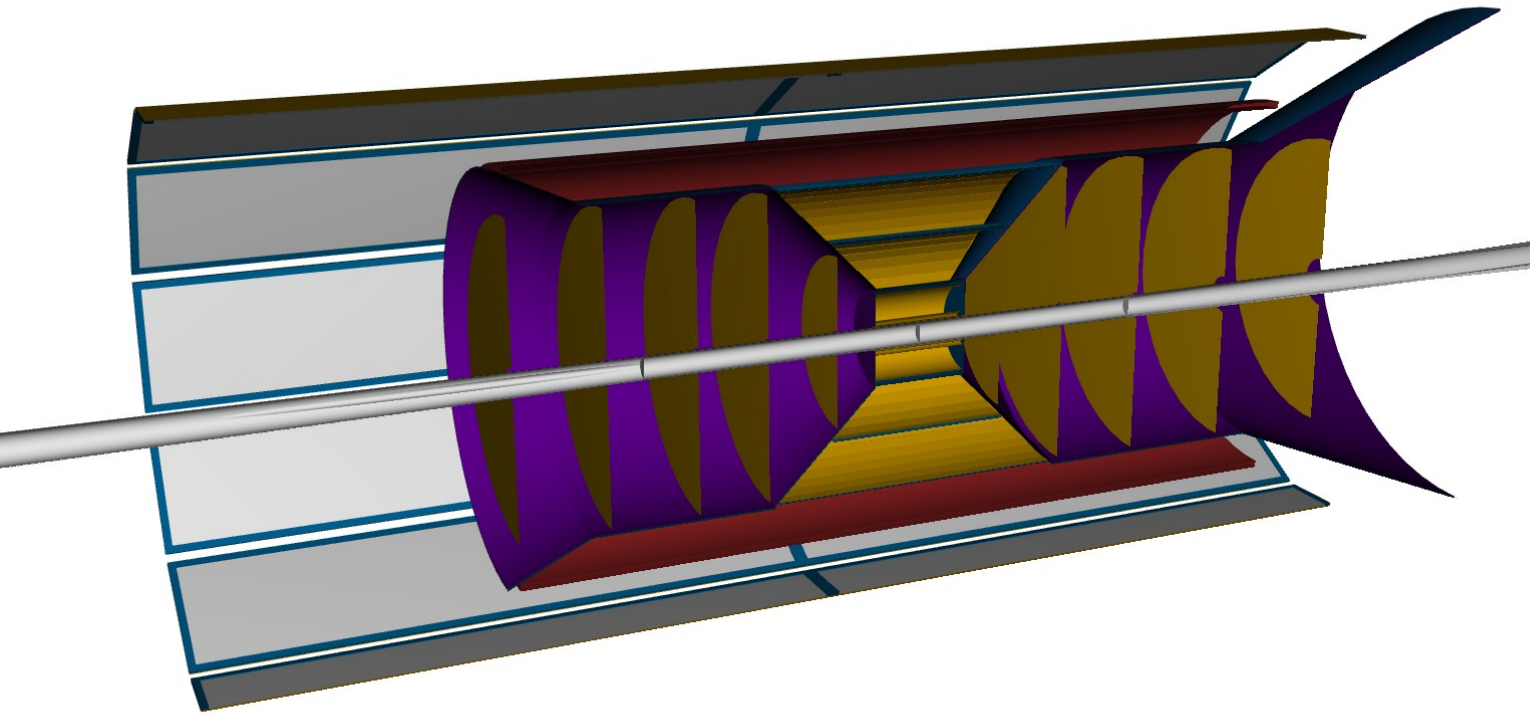
Silicon Tracker R&D @ LBNL

- EIC Silicon Consortium
  - Goal to develop & construct full tracking & vertexing detector for EIC based on **65 nm MAPS**
- EIC project R&D (targeted to detector 1, ePIC)
  - **eRD111**
    - **Silicon tracker, no sensors**
  - **eRD113**
    - **Sensor development & characterization**
- EIC generic R&D (risk mitigation, upgrades/optimizations)
  - Embedded silicon
  - Aluminum flex cable

Current status

- ePIC SVT layout developed for the first simulation campaign
  - **5** barrel layers, **5** disks per side



BARREL	r [mm]	l [mm]	X/X0 %
Layer 0	36	270	0.05
Layer 1	48	270	0.05
Layer 2	120	270	0.05
Layer 3	270	540	0.25
Layer 4	420	840	0.55

DISKS	+z [mm]	-z [mm]	X/X0 %
Disk 1	250	-250	0.24
Disk 2	450	-450	0.24
Disk 3	700	-650	0.24
Disk 4	1000	-900	0.24
Disk 5	1350	-1150	0.24

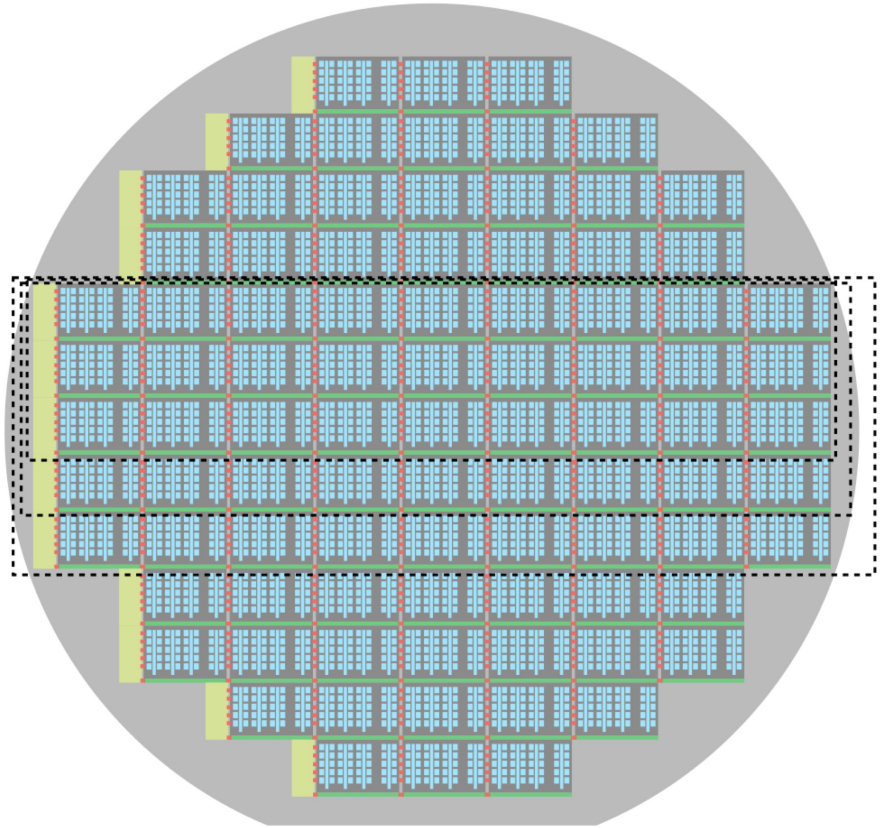
Goal: Minimize material, maximize acceptance

65 nm MAPS

- ALICE ITS3 MLR1: 2021+
  - 65 nm process verified
- ALICE ITS3 ER1: submission end of 2022
  - Stitching verification & first yield information

Big unknown!

- Open questions:
  - What changes need to be made if yield is low?
  - Power distribution over the stitched sensor



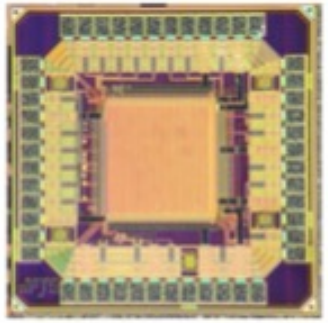
eRD113: Sensor development/characterization

- **Sensor development** – RAL, BNL, LBNL: at CERN for 6 months
- **Sensor characterization** – INFN, UK, LBNL, ORNL, LANL
- Establish work & contribution with ALICE ITS3 team on wafer-scale sensor design
- Characterization of ITS3 **MLR1** & **ER1**
- Make plans for **Large Area Sensor (LAS)**
  - Understand changing stitching plans, evaluate specific functionalities for EIC sensors
- Collaborate with eRD111 & 104

Contact person: Grzegorz Deptuch

MLR1 Characterization - DPTS

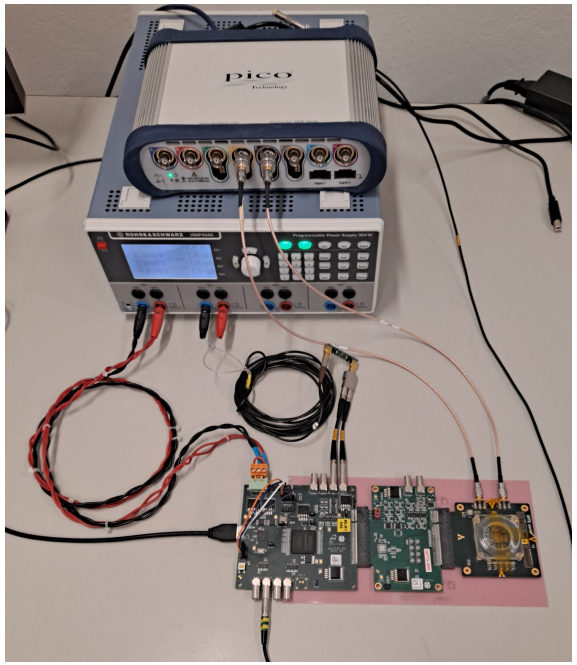
DPTS



Digital Pixel Test Structure

- 32 x 32 matrix, pitch: 15 µm
- Digital time-encoded pixel position

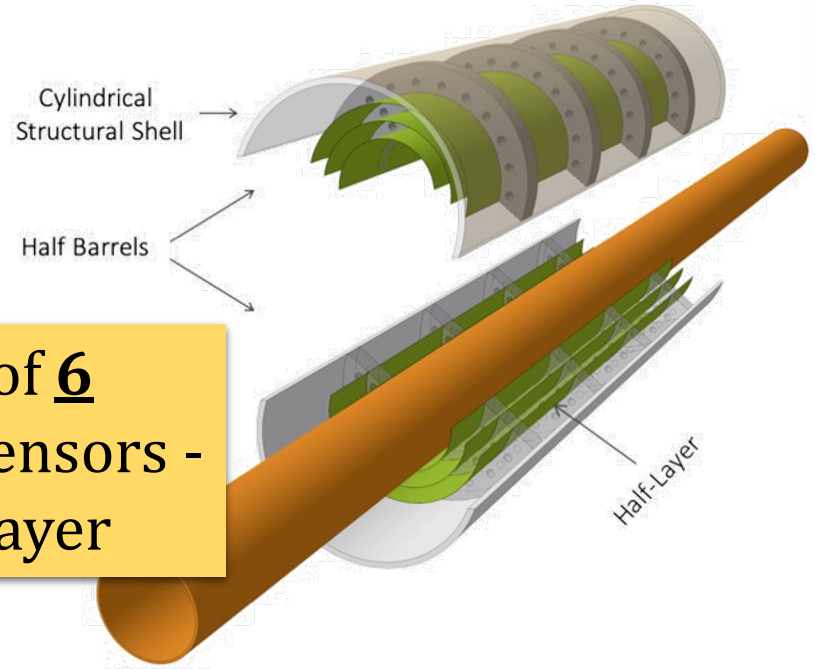
Test in-pixel discrimination and asynchronous digital readout
Instrumental for readout of future chips



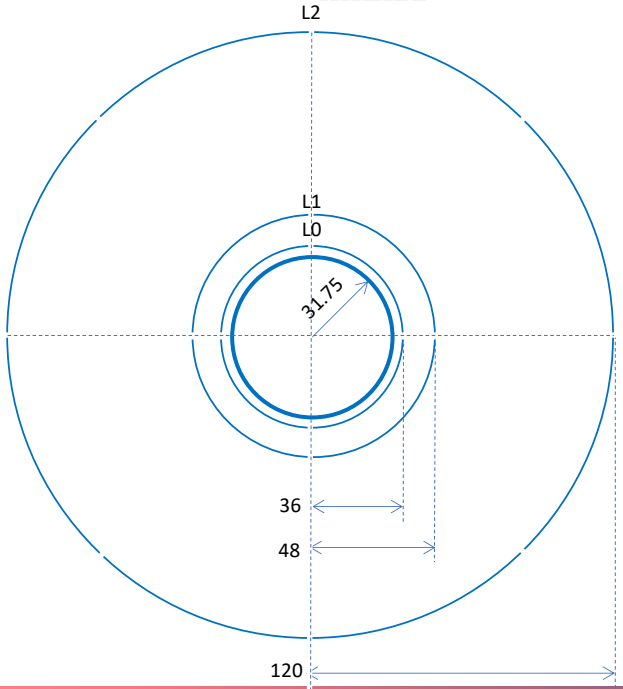
- Test bench setup in progress
  - Have local participation experience in bench & beam tests @ CERN & Trieste
- Task list available from ALICE ITS3
- Plans for beam tests at the 88”
  - Radiation testing?
  - ALPIDE telescope from LANL?

From ALICE ITS3 to EIC

- ITS3 sensor reticle size will be optimized for ALICE radii
- **EIC radii larger** → geometry needs to be adapted
- Some mechanical challenges still to be thought out
  - Lose some of the structural support from curvature
  - What is the stress/strain on silicon?



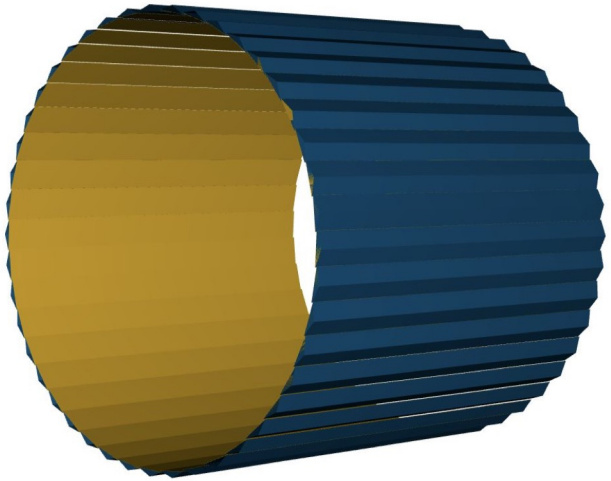
Total of **6** stitched sensors - 2 per layer

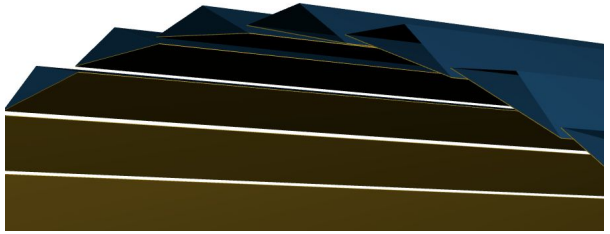


Option for ePIC layers 0-2

Total of **16** stitched sensors
Layers 0, 1: 4
Layer 2: 8

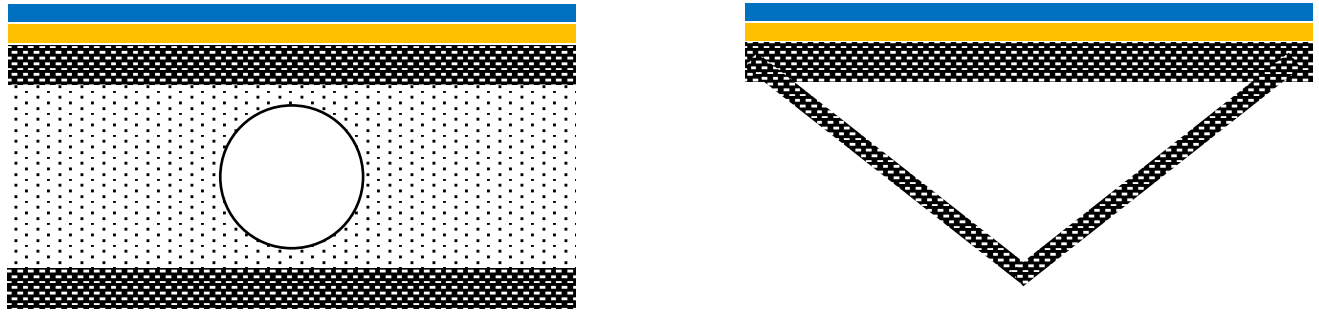
Staves & discs





- Material budget an issue for tracking
  - Longer lengths mean more material (power, support)

Potential stave & disc cross sections

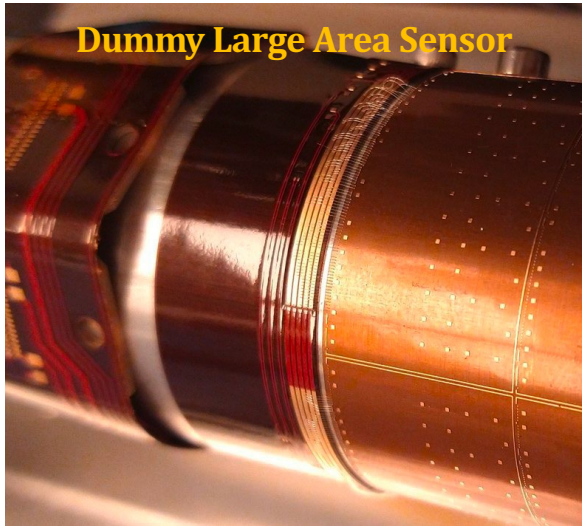


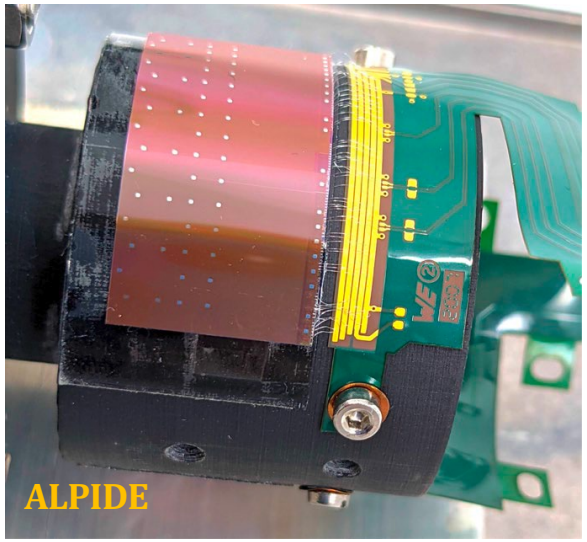
Not to scale

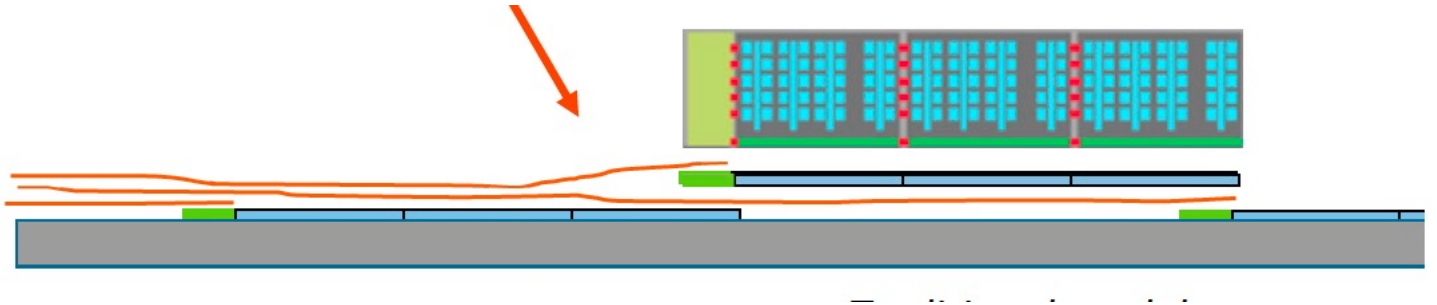
- FPC/power (aluminum)
- Silicon
- Carbon fiber
- Carbon foam

eRD111: Silicon tracking (no sensors)

- Modules (shown) – INFN, UK
- **Barrel & discs – LBNL, UK, LANL**
- **Mechanics, infrastructure, cooling – LBNL, LANL**



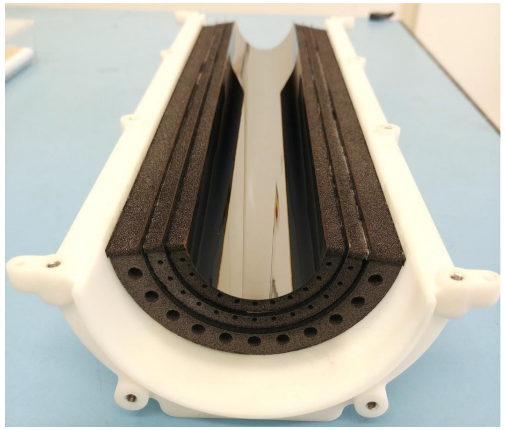


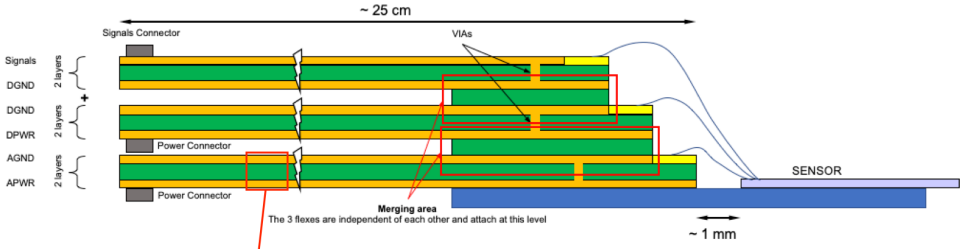


Traditional module: support+FPC+sensor

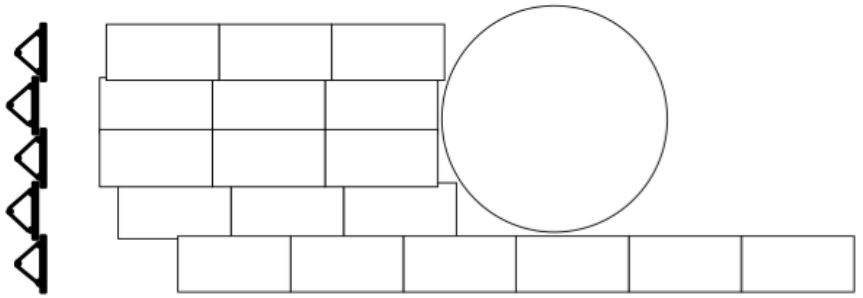
Contact person: Nicole Apadula

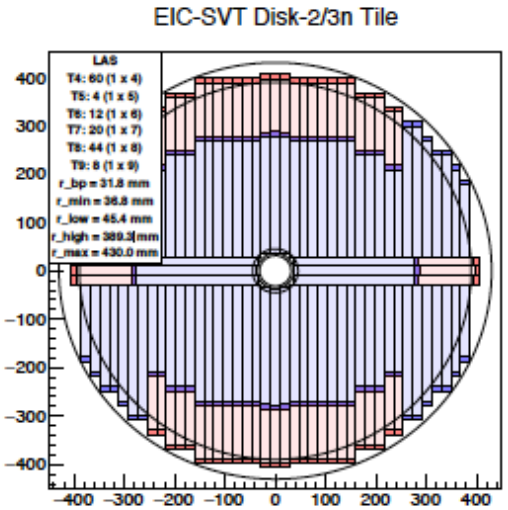
Barrel & discs





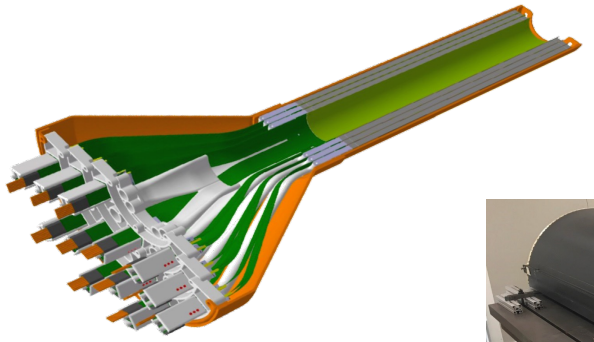
- **Vertex layers**
  - **Conceptual design**, including possible new support structures
  - **Prototype pieces**: carbon foam longerons/rings, carbon fiber support for wire bonding near periphery
- **Stave & discs**
  - **Conceptual design** – seriously consider stave-like disc design
  - **Prototype pieces** & (possible) mechanical & thermal tests

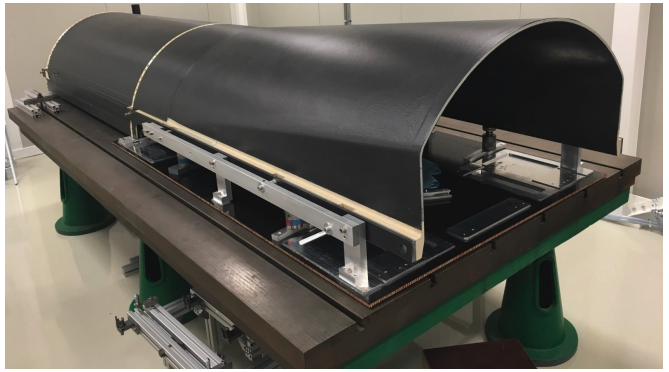


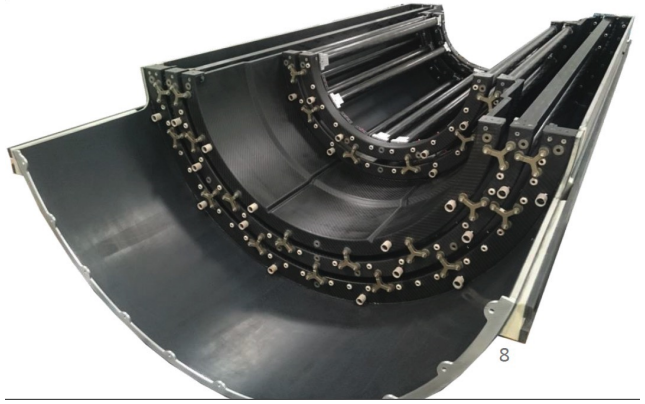


Mechanics, infrastructure, cooling

- Updated **CAD model** of tracker
- Analysis of cooling options
  - **Build on FY22 work for air**
    - **More information in talks from Beatrice & Mathias**
  - Vertex cooling options
  - Beam pipe bake out
  - Add liquid cooling options
    - Particularly important for periphery (900 – 4000 mW/cm^2)
- **Conceptual designs** for detector support structures
  - Prototype pieces with (possible) mechanical & thermal tests







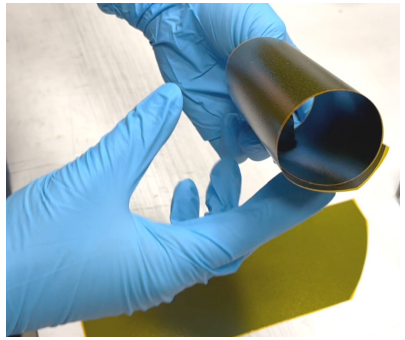
Generic R&D: embedded silicon

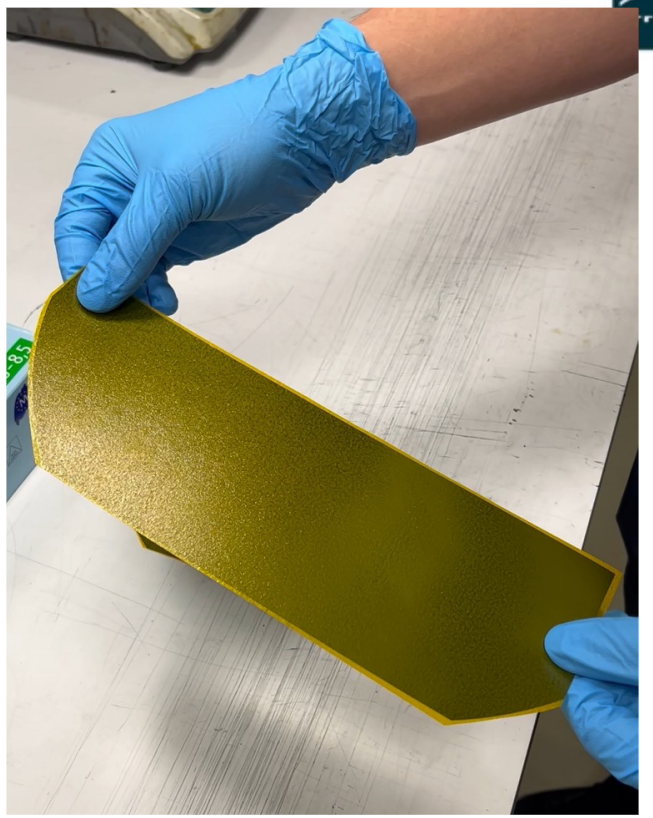
Motivation

- Alleviate deformation expected from carbon foam longerons
- Reduce mechanical strain to the bare silicon
- Sagitta/Outer layers: Planar staves → larger, more cylindrical barrel structures
- Overcome possible weakness in power distribution network in 65 nm process

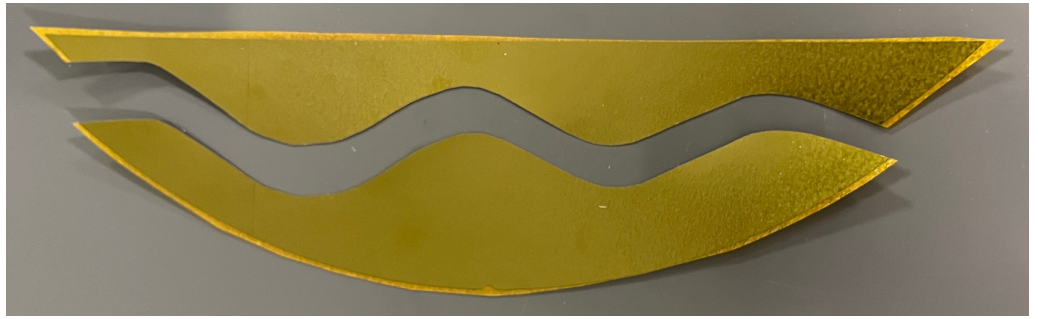
Risk reduction for detector 1, options for detector 2

Silicon lamination



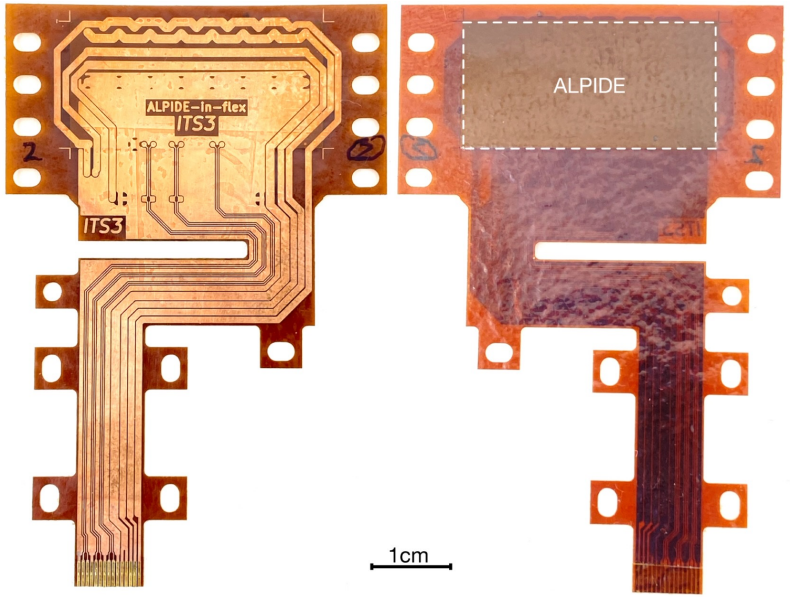


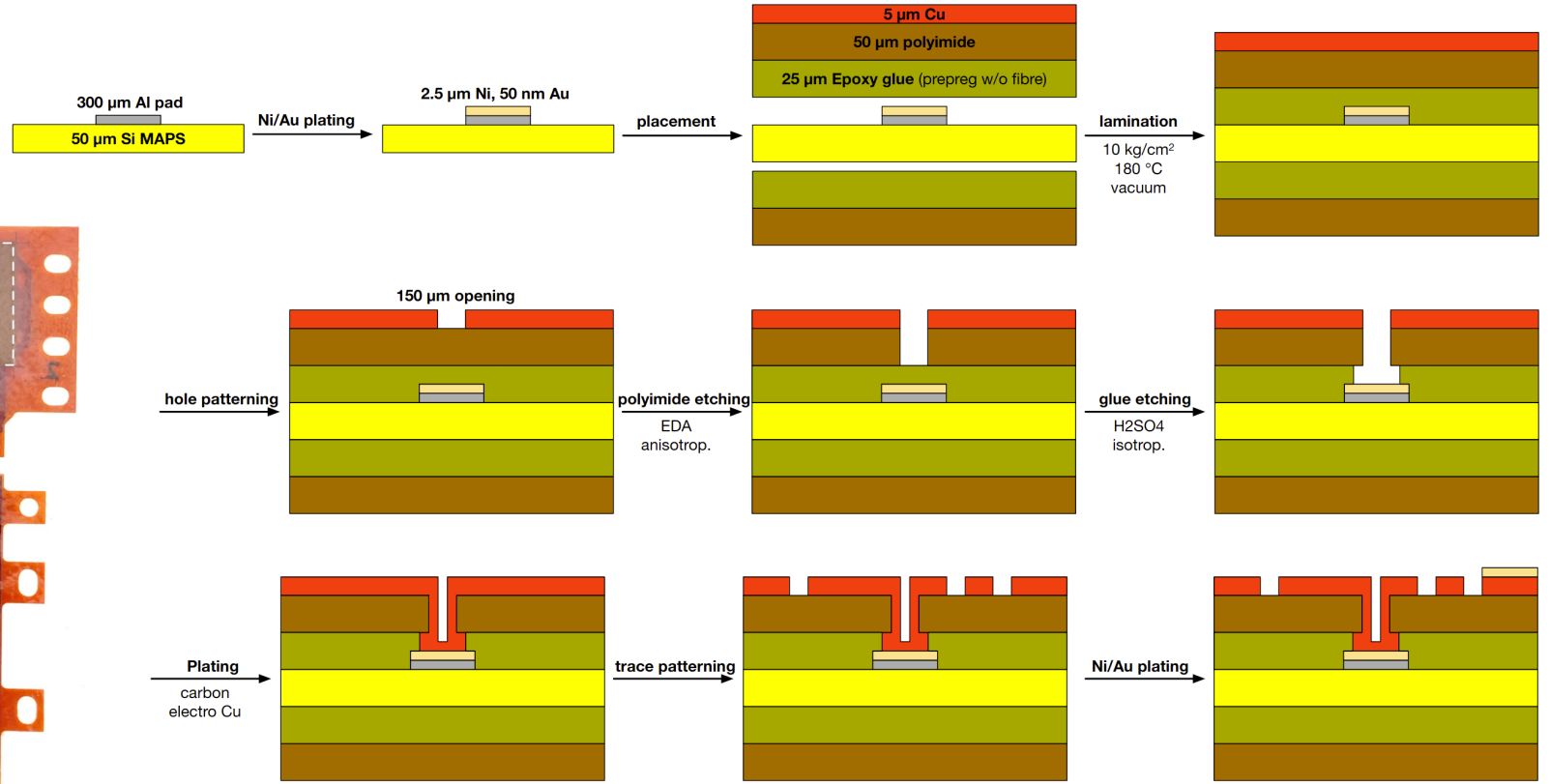
- ORNL on-site facility will produce embedded silicon pieces (**single reticle** & **larger area**)
- LBNL will use pieces for **thermal & mechanical tests**
- Similar process ongoing at CERN



Improved mechanical resistance with low material: 0.1% X/X_0 silicon + kapton

“MAPS foil”





https://doi.org/10.1016/j.nima.2022.167673

- Kapton foil lamination process developed for thinned MAPS
- Demonstrated successfully on single ALPIDE sensors (ITS2)

Aluminium Flex PCB (cable)

Radiation length:

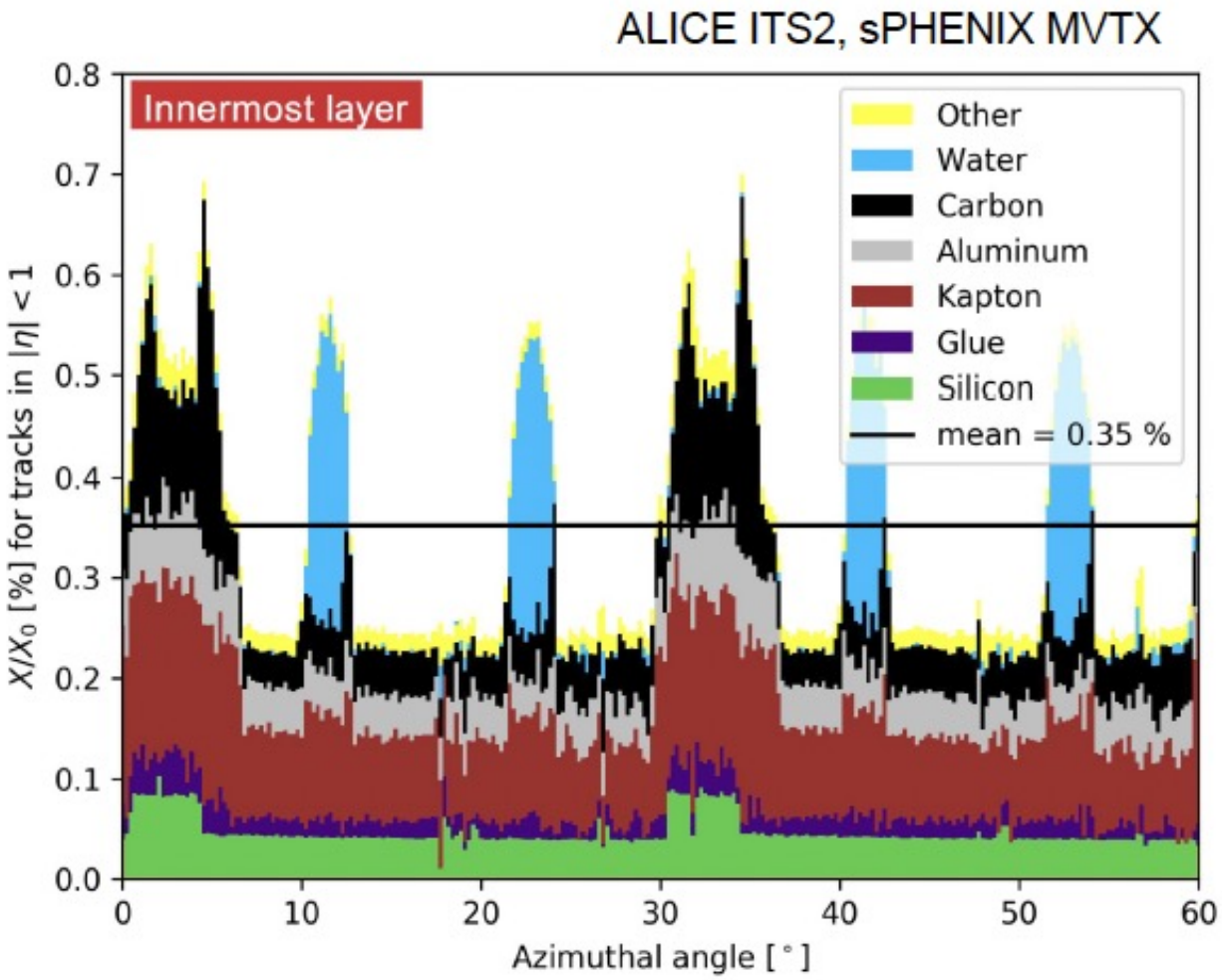
$X_{0\ Cu} \sim 1.4cm$
$X_{0\ Al} \sim 8.9cm$
} factor 6

CERN

Kharkiv Institute

Explore companies:

- Hughes Circuit Inc. (CA)
- Qflex Inc. (CA)
- Omni Circuit Boards Ltd. (BC, Canada)



From Yuan Mei's Generic R&D presentation

Summary

- R&D for the silicon tracker is underway
  - Work expected to pick up significantly in FY23
- Focus is on keeping material budget low & buildability
- @LBNL
  - **Barrel & disc** designs & prototypes, **Mechanical support & infrastructure** designs & prototypes, **Cooling** studies → focused on air, **Embedded silicon**, **Aluminum flex**
- Welcome input & collaboration
  - Lot's of work still needed to make this successful!