Summary of the RDO/Timing Subgroup Mtg on Jan 23

- present: Jo, Marius, Pietro, William, Tonko
- fixed word size of 120 bits; use 8b10b decoding ⇒ 12 bytes available
- words are strobed with the EIC clock (~100 MHz) ⇒ link rate 12 Gbs
- first byte of the word is always the K28.0 comma symbol
  - used for bit & byte alignment → indicates byte 0
  - and used to align the recovered clock to the rising edge of the sent clock
- we plan to implement the clock recovery including clock feedback to FELIX PLLs (ala TClink)
- 88 bits are free for the user to use
- 5 special control words (as 8b10b “K” or “comma” words)
  - **LINK_IDLE** – issued when there’s no data to send
    - also necessary during link establishment
  - **LINK_IDLE_BUSY** – same as above but also indicates the sender is BUSY and data to the sender should be throttled – provides a data backpressure mechanism
  - **FRAME_START** – start of data packet/frame
  - **FRAME_END** – end of data packet/frame
  - **FPGA_RECONFIGURE** – FPGA should reconfigure (added this after the Mtg; only sent *to* the RDO)

- the link will have 3 states
  - LINK_ESTABLISHMENT: at power up, during the link establishment & synchronization
  - CONFIGURATION (entered automatically after LINK_ESTABLISHMENT)
    - FELIX user (e.g. code on the DAQ PC) “owns” the downlink
    - user is free to send free-form data to the RDO
      - e.g. configuration data for the ASICs etc
  - RUNNING
    - the GTU “owns” the downlink and only special pre-defined 1-word strobes are sent deterministically to the RDO directly from the GTU
    - e.g. TIMEFRAME, TRIGGER/PULSER, STATE_CHANGE etc.
- bulk data is organized into frames of some maximal size (~ MBs)
  - **start-of-frame comma**
  - *data…*
  - **end-of-frame comma**
    - *NOTE that this has nothing to do with the length of the streaming “timeframe” but is part of the low level framing protocol to be able to adjust the various buffer sizes in the destination e.g. memory blocks in the DAQ PC*
- Marius will attempt to implement this protocol and clock recovery on Xilinx devkits he already owns

Miscellaneous

- we plan to use SFP28 transceivers on the RDO
  - [Pietro] his experience is that some manufacturers are more radiation tolerant than others ⇒ he will investigate further
- Forward Error Correction (“FEC”) ala lpGBT
  - we don’t think it is necessary due to our much gentler radiation environment compared to LHC
  - OTOH we will look into it and see what can be implemented to correct only 1 or 2 bit flips or at least detect bit flips via a checksum algorithm [Tonko]
  - NOTE: if implemented it will decrease the available word size from 88 to e.g. 80 or so…