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Reminder: ALPIDE Principle of Operation



Continuous Mode: long "strobes" (~5-20µs), followed by short inter-strobe periods (100 ns) for readout





ALPIDE Readout Block Diagram







CAK RIDGE

4



CAK RIDGE

5

Stitched backbone busses and fast serial outputs





~28 cm



6





Remark on timing

Projections for timing resolution

Targeting figures similar to ALPIDE

Continuous mode readout Integration period: 5 / 10 / 20 us Frame rate: 200 / 100 / 50 kHz

Low power constrains response speed MOSS pulse duration 40 us @ 1 ke MOSS time walk ~3.3 us Reviewing timing specs for next design

Discriminator time window

(MOSS, nominal bias for low power)



Discriminator time window



A few private remarks from one of the ITS-3 chip designers

- Overall readout scheme considered for ITS-3 similar to ALPIDE
 - Global strobe signal, in-pixel latching logic, transfer of hits using topological priority encoder
 - In-pixel memory not yet defined
 - Looking into latching the discriminated hit using rising edge of discriminator in coincidence with strobe assertion
- Strobe programmability will be 1us -> 100 us, duration from O(200ns) to the period
- Considering time-walk and readout scheme, best achievable timing resolution O(3us) for ITS-3
- No sophisticated clustering or other processing, likely only similar to ALPIDE combining neighboring pixels in readout
- Don't see a path to significantly improved timing resolution in ITS3 vs ALPIDE without relaxing power constraints, area constraints, and granularity
 - Intrinsic pixel sensor timing resolution OK, but collection, maintaining, and transmission at far distances not possible to reach anywhere near 100ns for very large arrays of small pixels; seen as a system design problem
 - Doubtful to achieve a gain of 1-2 orders of magnitude in timing without orders of magnitude more power and a good fraction of non-sensitive areas on the chips





EPIC Vertex and Sagitta Layers

Note: these are active lengths; they do not include the periphery

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L0, L1 and L2 lengths are single sensors that are 270 mm long (9 reticles)

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L3 length can be achieved using two sensors 270 mm long (9 reticles), or three sensors 180 mm long (6 reticles) Choice of two or three sensors may be decided by sensor yield

L4 length can be achieved using four sensors 210 mm long (7 reticles)

EIC SC general meeting | ePIC SVT layout | 07 Nov 2022



Disk Tiling

• More details on the disks tiling study and methods in the backup and here <u>https://indico.bnl.gov/event/17073/</u>

r_bp = beam pipe radius
r_min = r_bp + 5 mm
r_max = outer disk radius
r_low = smallest radius with full
acceptance
r_high = largest radius with full acceptance

TX: YY $(1 \times X) \rightarrow$ on the disk there are YY Tiles made of one stitched row of X reticules.

Example: T5: 12 (1x5) \rightarrow on the disk there are 12 tiles made of one stitched row of 5 reticules (i.e. 18.85 mm x 150 mm).

EIC-SVT Disk-1 Tile





ePIC MAPS Detector

Barrel					Se	nsor											
Layer Index	radius (mm)	z (mm)		Area (mm^2)	reticles in width	reticles in length	# of sensors in r-phi	# of sensors in z						# pixels	# sensors	Mechanical	# Readout Links
0	36	270		61,074	3	9	4	1						271,440,000	4	bent ITS3	96
1	48	270		81,432	4	9	4	1						361,920,000	4	bent ITS3	128
2	120	270		203,580	5	9	8	1						904,800,000	8	bent ITS3	320
3	268.4	540		1,017,900	1	9	100	2						4,524,000,000	200	stave	1600
4	418.5	840		2,470,104	1	7	156	4						10,978,240,000	624	stave	624
				LAS	T1	T2	T3	T4	T5	T6	T7	T8	T9				
				# of reticles	1	2	3	4	5	6	7	8	9				
e-endcap																	
Disk index	z (mm)	inner r (mm)	oute	r r (mm)													
1	-250	36.76	230	133,458	4	4	4	8	12	20	0	0	0	593,146,667	52	stave	52
2	-450	36.76	430	506,688	0	0	0	60	4	12	20	44	8	2,251,946,667	148	stave	148
3	-650	36.76	430	506,688	0	0	0	60	4	12	20	44	8	2,251,946,667	148	stave	148
4	-900	40.0614	430	507,819	0	0	0	62	4	16	18	42	8	2,256,973,333	150	stave	150
5	-1150	46.3529	430	505,557	0	0	0	64	2	16	20	40	8	2,246,920,000	150	stave	150
h-endcap Disk index																	
1	250	36.76	190	133,458	4	4	4	8	12	20	0	0	0	593,146,667	52	stave	52
2	450	36.76	430	506,688	0	0	0	60	4	12	20	44	8	2,251,946,667	148	stave	148
3	700	38.52	430	505,557	0	0	0	62	2	12	20	44	8	2,246,920,000	148	stave	148
4	1000	53.43	430	503,295	0	0	0	64	4	14	20	42	6	2,236,866,667	150	stave	150
5	1350	70.14	530	506,688	0	0	0	62	4	14	24	38	8	2,251,946,667	150	stave	150
TOTAL				8,149,986										36,222,160,000	2136		4064

Pixel Size: 15µm Reticle Size: 18.85 x 30 mm² ~2.5 GPixel



Readout Thoughts

N. Schmidt's Simulations:

Detector	Average # hits in min. bias pythia6 (10x100 GeV)	Average # hits in High Q2 pythia6 (18x275 GeV)
Full barrel (3 vertex + 2 sagitta)	9.3	30.7
Full forward (5 disks)	16.8	36.3
Full backward (4 disks)	6.4	2.2
Barrel layers (0/1/2/3/4)	2.4 / 1.7 / 1.4 / 1.9 / 1.8	7.2 / 5.8 / 4.9 / 6.6 / 6.2

- Adding these numbers, the total number of hits (vertex, sagitta, forward/backward disks) would have around 70 hits. Latest
 results from DPTS show about 1.2 pixels firing per hit, but no study has yet been done how that changes with incident angle. This
 would result in about 85 pixels with data. Let's assume the background is about the same size, i.e., a total number of 170 pixels
 per event. How much should we assume for the angle effect?
- An assumed collision rate of **500 kHz** would then result in a "Physics" pixel rate of **85 Mega-pixels per second**.
- From recent DPTS fake hit rate results, it seems that the current MLR1 prototype sensors have a noise rate of about 10⁻² pixel⁻¹ sec⁻¹ (corresponding to 10⁻⁷ pixel⁻¹ event⁻¹ for ALPIDE). For a total number of 36 B pixels in ePIC, this would result in a total of 310 Mega-pixels per second fired just from noise.
- Adding "Physics" and "Noise" together we need to read out ~400 Mpixels/sec. So far there are no thoughts yet on the data format out of an ITS-3 sensor, it will probably look very similar to the format from ALPIDE, i.e., region headers followed by double column addresses, followed by (clustered) matrix addresses of hit pixels. Let's assume for simplicity 64 bits per pixel. This results in a total data rate of 25.6 Gbps, not very much compared to a fiber rate of similar capability for the new Phase-2 FELIX fiber links. Whatever Readout Unit would be developed for ePIC MAPS would mainly be concerned with aggregation of multiple copper links, removing empty frames, and transmission over 10 or 25 Gbps fiber links.

... next slide ...



Readout Thoughts (continued)

- The range of transmission in ITS2 from the staves to the Readout Units is about 8m at 1.2 Gbps. Studies by M. Rossevij with the Samtec firefly cables used in ITS-2 show that transmission at that speed already needs proper pre-emphasis and equalization, and that the BER eye closes fully at ~3Gbps. For 5 Gbps transmission lines it seems that an active repeater is needed at ~1m from the edge of the flex. In case of ITS3 these would be in the service cone, i.e., not in the active region of the ALICE detector. Where would we be able to place such repeaters in ePIC?
- For ITS-3 the line drivers will likely not be configurable for speed, since the layers in ITS-3 are very close and thus need the same rate capabilities, but some configurability (be it the line rate or how many are actually activated and used) might be envisaged (according to Gianluca), still to be determined in the future.
- Where would we be able to place the above-mentioned Readout Boards? How far would that be from the edge of the flex cables from the sensors?
- A possible means of reduction of the required links out of the MAPS barrel region would be to use a rad-hard FPGA board to multiplex copper links for up and downstream into one or more fibers (combined into a fiber bundle like an MTP assembly) close to the flex circuit of the sensor. Possible candidates for FPGA and fiber converters were identified in earlier work in eRD104:
 Microsemi PolarFire FPGA, and Samtec optical FireFly. Rad-tolerance might require use of the VTRx+ fiber assembly from the lpGBT development (possible use of the lpGBT ASIC as well?) instead of Samtec optical FireFly. Questions: Would it perhaps be possible to incorporate such circuitry into the flex circuit of the sensor? If not, where would such a PCB be possible to place (close to the flex)?
- In ITS we were able to accommodate up to 28 copper links per Readout Unit. For ePIC this aggregation would depend on the number of transceivers available on the FPGA chosen for the RDO board. A (cheap) candidate is the Xilinx Artix UltraScale+
 FPGA family (~\$250 for the XCAU10P) which has up to twelve 12.5 Gbps transceivers. Assuming 10 links for copper, and 1 link for fiber, this would mean one would need ~400 RDO boards (corresponding to 400 12.5 Gbps fibers). Each FELIX will likely have up to 48 fiber links. The whole MAPS detector would then need 10 FELIX boards.

