

3/2/2023 ePIC DAQ WG Agenda

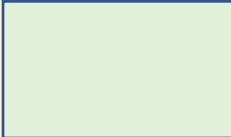
1. Announcements & ongoing task status
2. Collaboration and workgroup re-organization discussion
(John Lajoie)
3. At the stage where we need to defined the P6 costing and schedule at a detailed level to begin P6 tracking. Want to walk through the components and connections to ensure all elements are present.

Announcements & ongoing task status

1. Timing and synchronization
 - Ready to purchase development boards:
 - This will be handled from jlab by Dave Abbot, with funds split between jlab DAQ group development and EPIC DAQ project development funds
 - Dave needs an updated list of boards and vendors to make this purchase
2. FELIX purchase (1 or 2 boards)
 - The purchase mechanism process is started and likely to continue for a while
 - The purchase is not connected to getting the board from Hao, need to follow up on this
3. DAQ software/computing subgroup met on 2/17 to discuss priorities
 - Plan to set combined meeting between DAQ subgroup and Software subgroup “soon”
4. Additional Participation
 - Taku Gunji (University of Tokyo), Ralf Seidl (RIKEN), Yuji Goto (RIKEN) have expressed interest
 - Meetings last week and this week with DAQ conveners & software conveners
 - EIC Asia Workshop Mar 16th-18th, I will give overview DAQ talk (over zoom)
 - India
 - Deepak Samual has some available students for near term work, if we can specify it!
 - In general, Bedanga has asked us to help define tangible contribution for Indian groups for use in their proposal
5. GDI – digitization model discussion (2/13)
 - Digitization cartoon added to DAQ Wiki
 - Parameters updated in google sheet (and being filled in)
https://docs.google.com/spreadsheets/d/1s8oXj36Sqlh7TJeHFH89gQ_ayU1_SVEpWQNkx6sETKs/edit#gid=0
6. Cables worksheet was discussed last week, are there to-do items here?


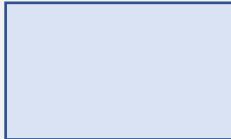



Component Walkthrough...

EPIC Electronics / DAQ



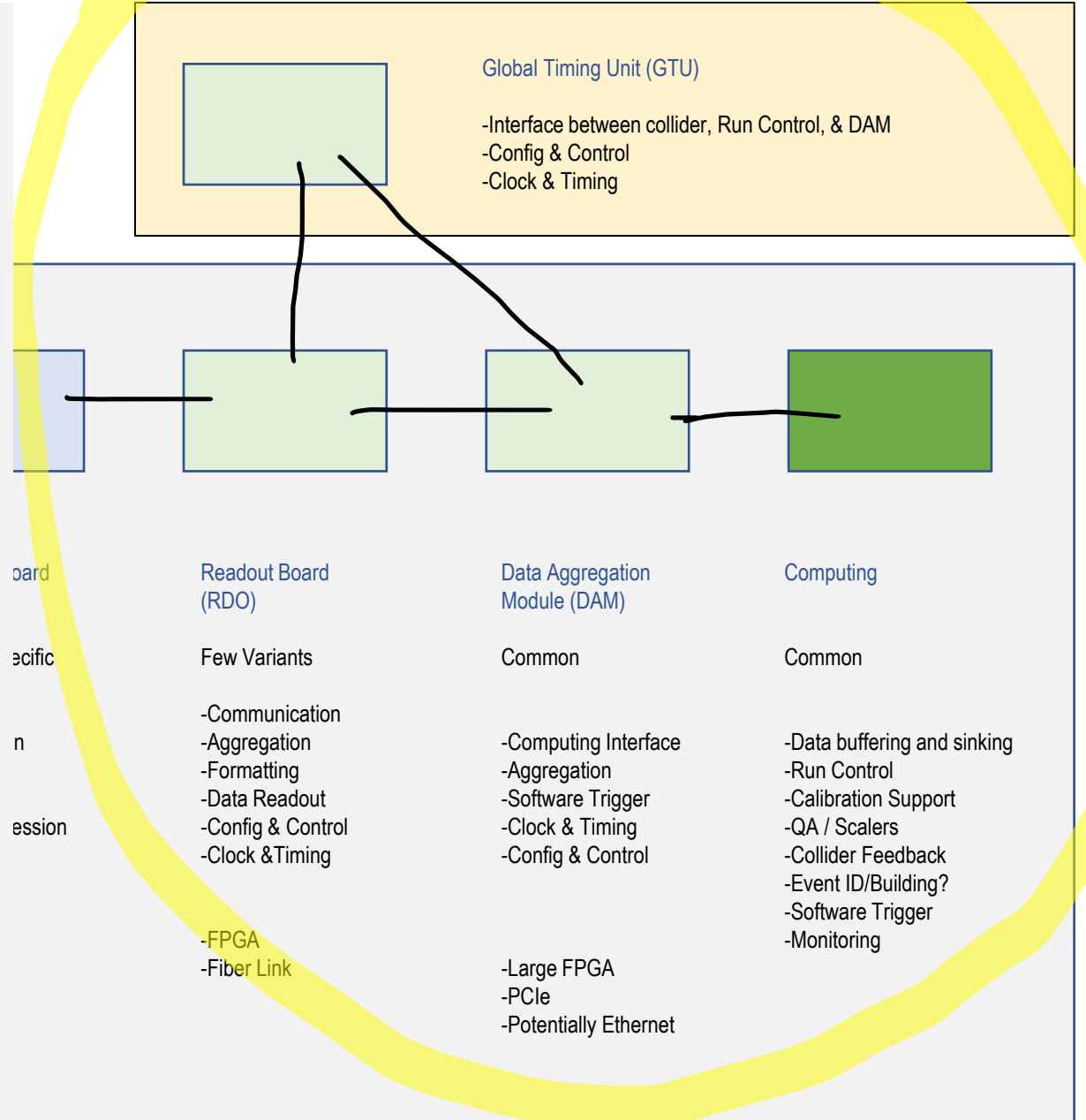
Global Timing Unit (GTU)

- Interface between collider, Run Control, & DAM
- Config & Control
- Clock & Timing

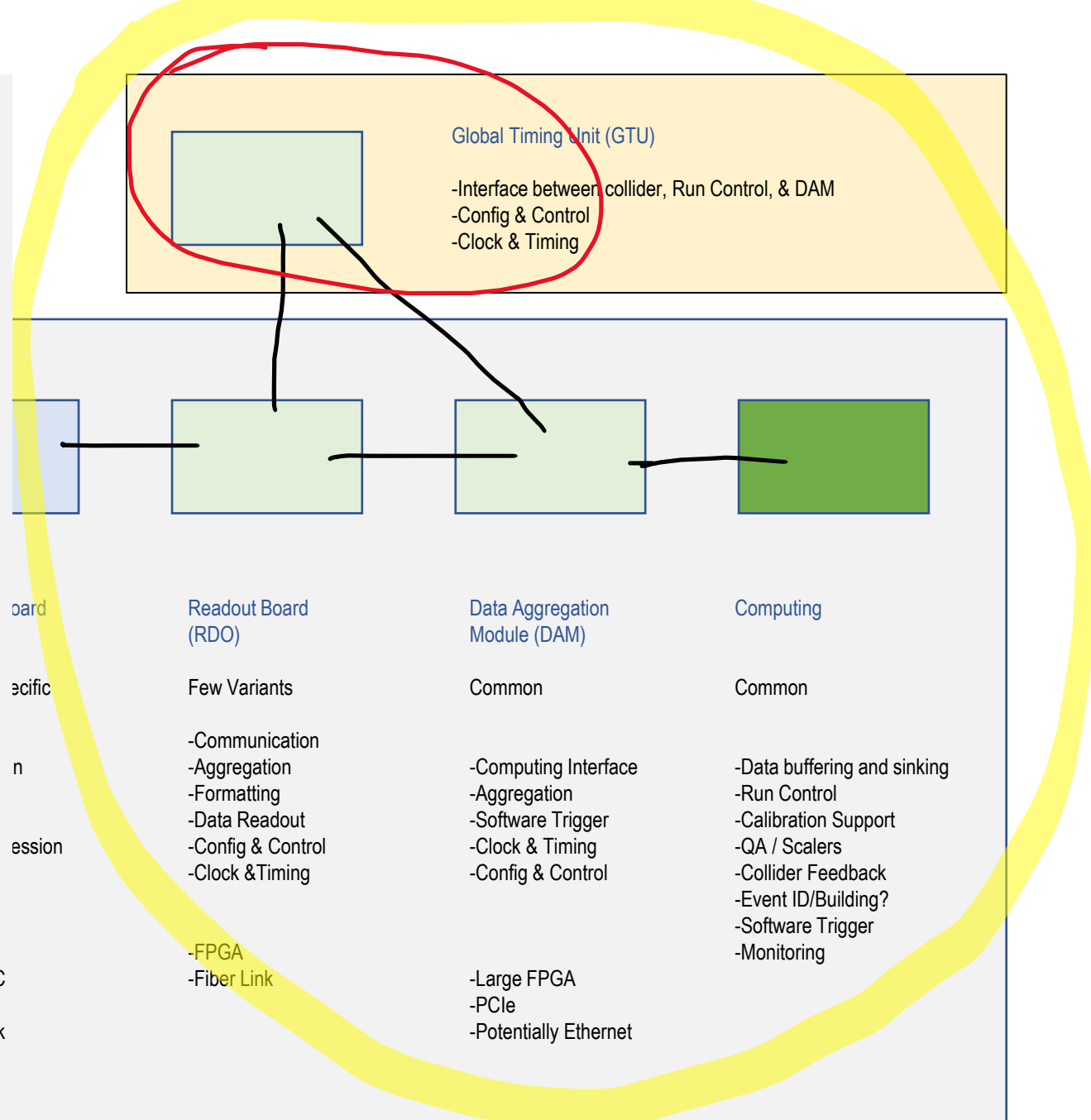
						
Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Sharing	Detector Specific	Detector Specific	Detector Specific	Few Variants	Common	Common
Function	-Multi-Channel Sensor	-HV/Bias distribution -HV divider -Interconnect routing	-Amplification -Shaping -Digitization -Zero Suppression	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Clock & Timing -Config & Control	-Data buffering and sinking -Run Control -Calibration Support -QA / Scalers -Collider Feedback -Event ID/Building? -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Potentially Ethernet	

System walkthrough

Discuss definition of and connections between these components:



GTU connections

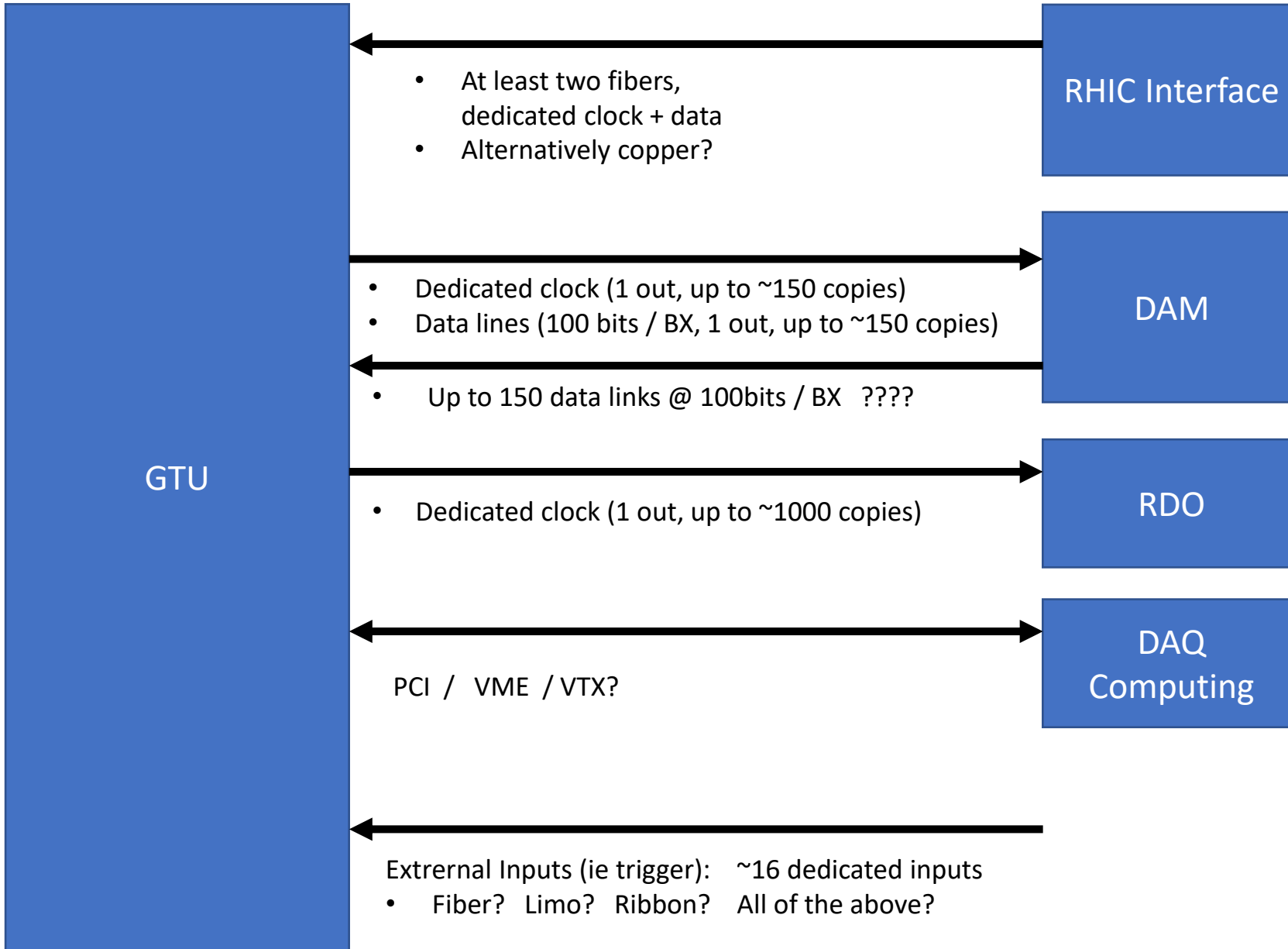


Attributes

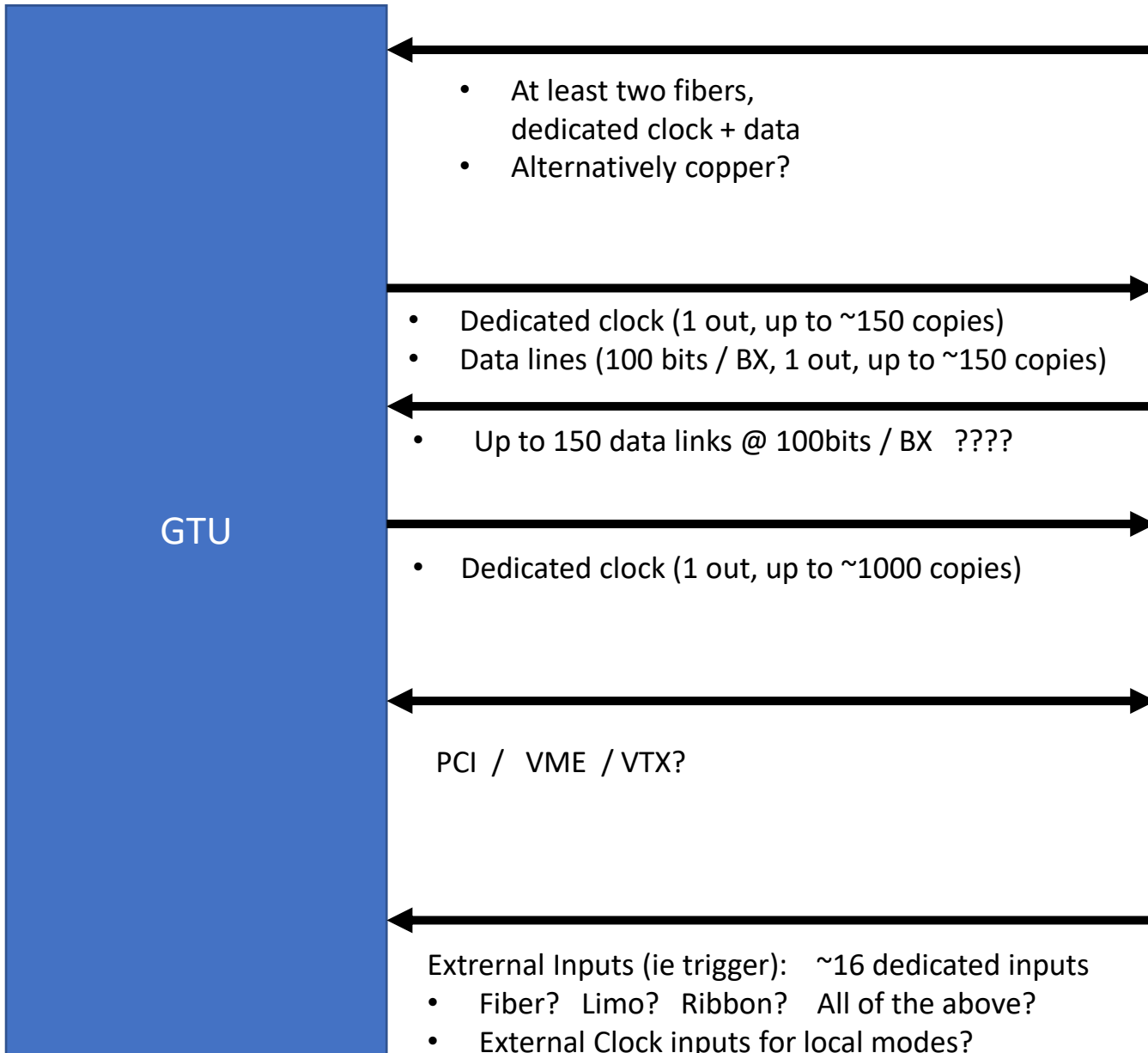
- MAPS
- AC-LGAD
- MCP-PMT
- SiPM
- LAPPD

- Sensor Specific
- Passive

- ASIC/ADC
- Discrete
- Serial Link



- Clock
 - 98.5Mhz frequency
 - ~1ps phase stability
- ~8 bits of information / bunch crossing
- Dedicated Clock
- Timing Information (100bits / BX)
- Flow control information (token?)
- Dedicated Clock Select Detectors (AC-LGAD / LAPPDs)
- Configuration
- “slow realtime”
 - Handled data up to 1ms time frames... every time frame via FIFO



Direct Fiber Output:

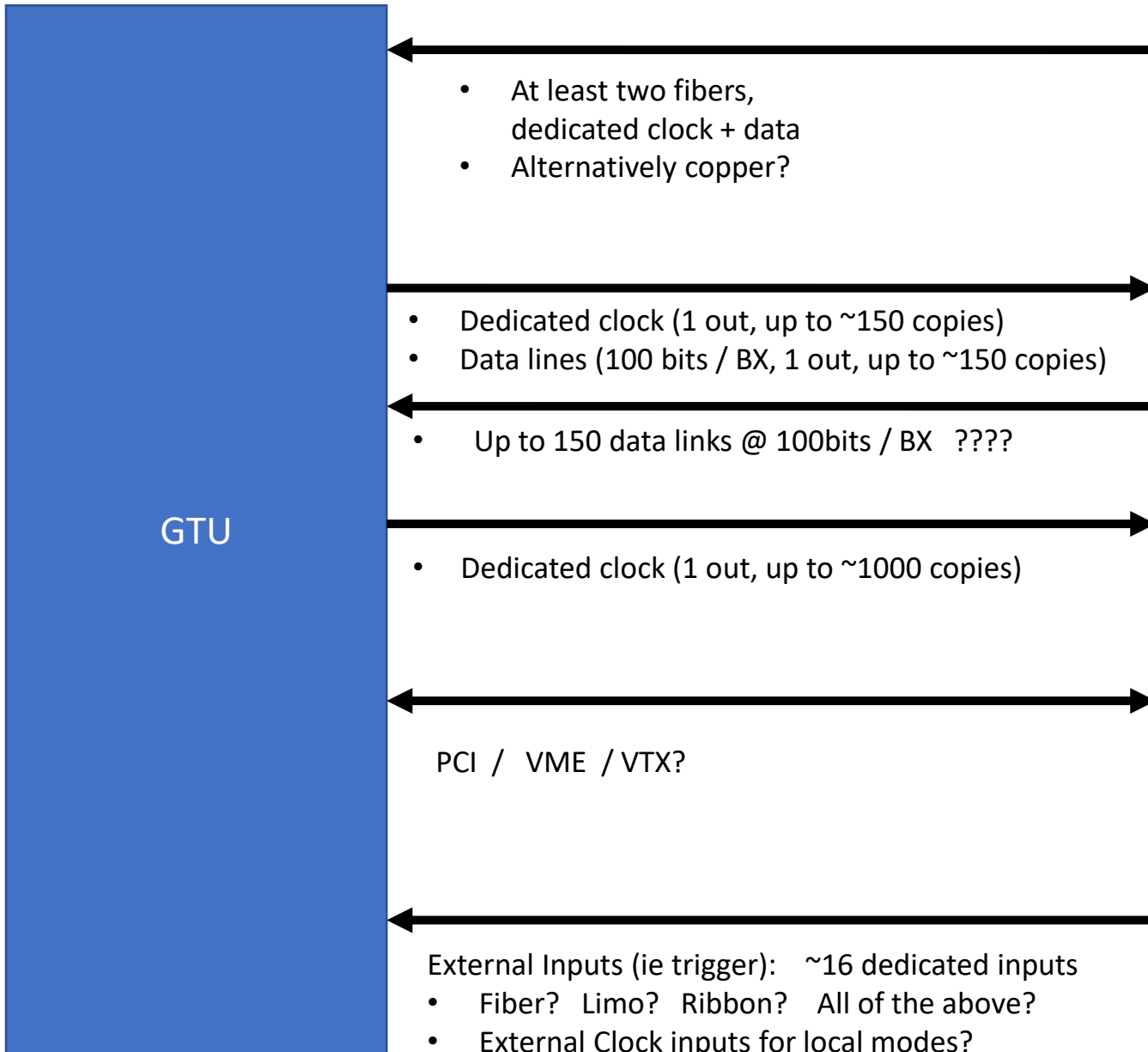
- 1 clock
- 1 data

Direct Fiber Input:

- $N \leq 30$ Dedicated clock
- 150 data links (or)
- Separate input aggregator with ability to determine states

BUS / Backplane computer communication

External inputs



Output aggregation unit?

What do we need?

- Patch panels
- Splitters?
- Same board with tree structure?
This would allow for independent operation of separate detectors
- Some combination of above?

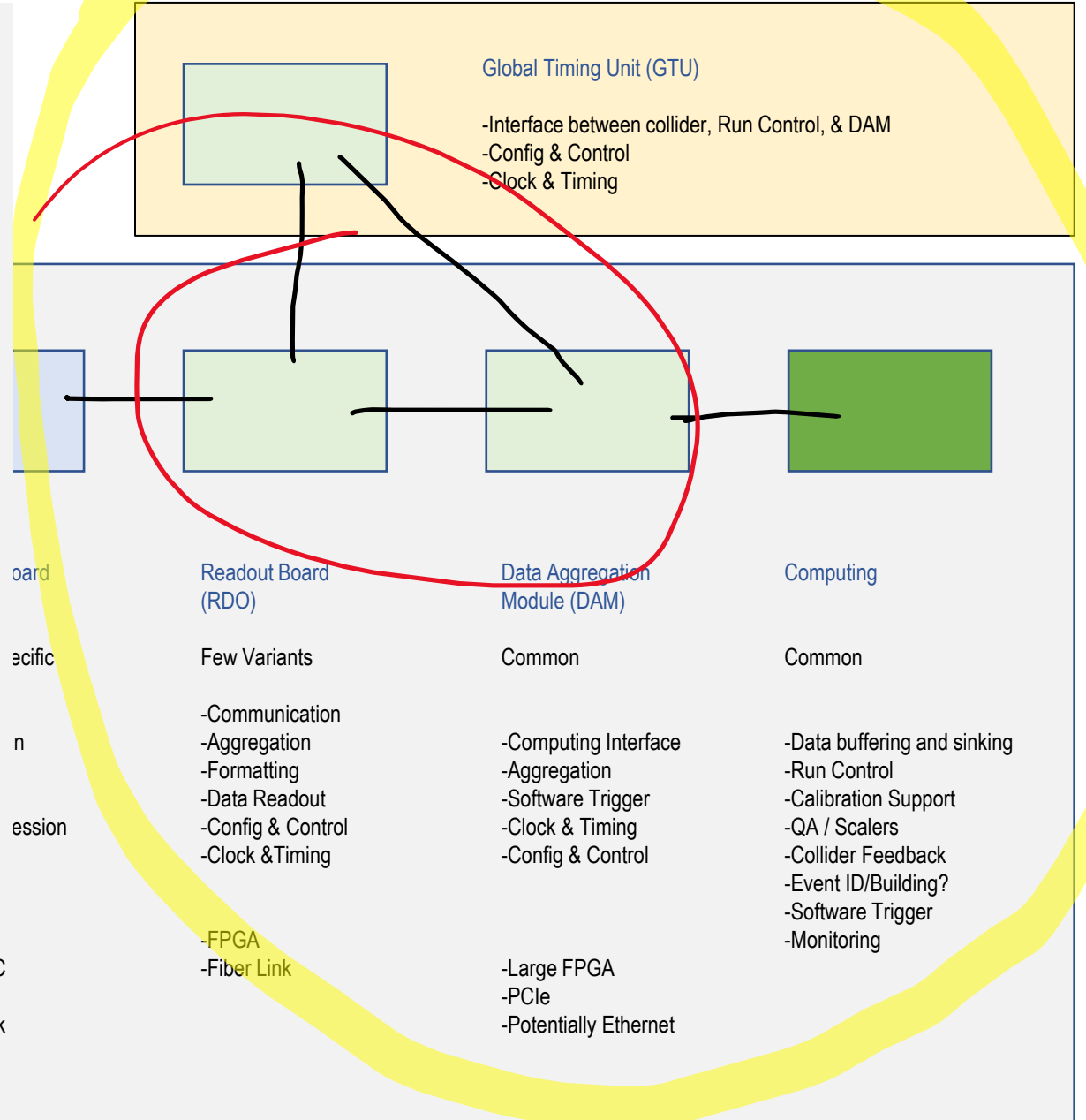
Input aggregation unit?

- Do we need this connection?
- Can we reasonably have 150 data links in, or do we need aggregation?

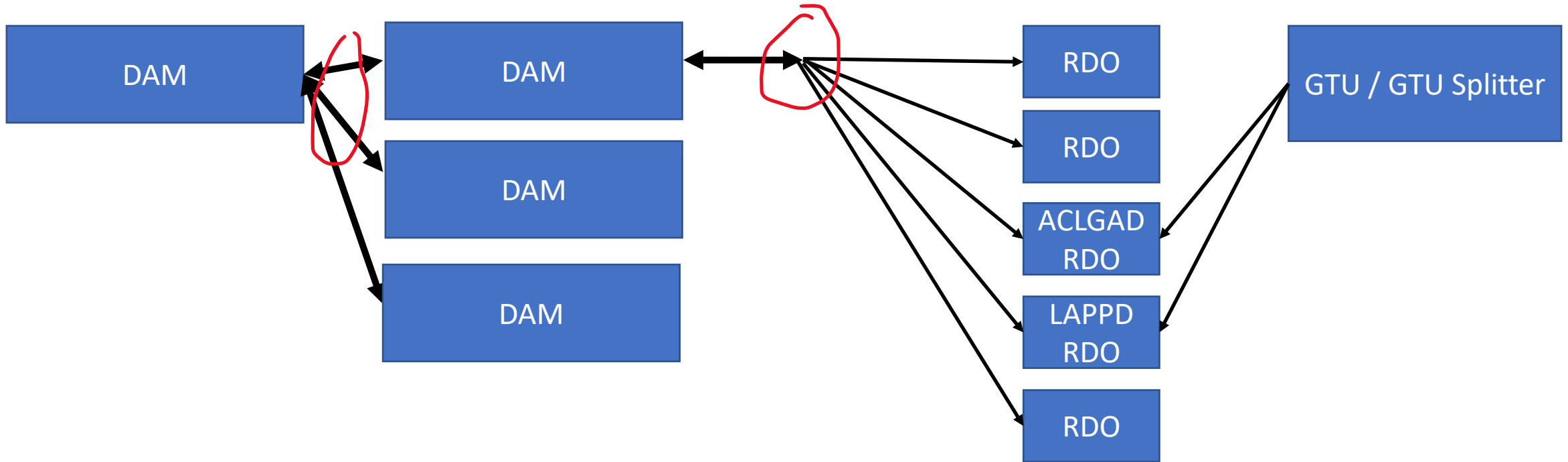
Form Factor?

- Boards in crates
- PCI?

RDO / DAM connections



DAM / RDO Boards Fiber connections

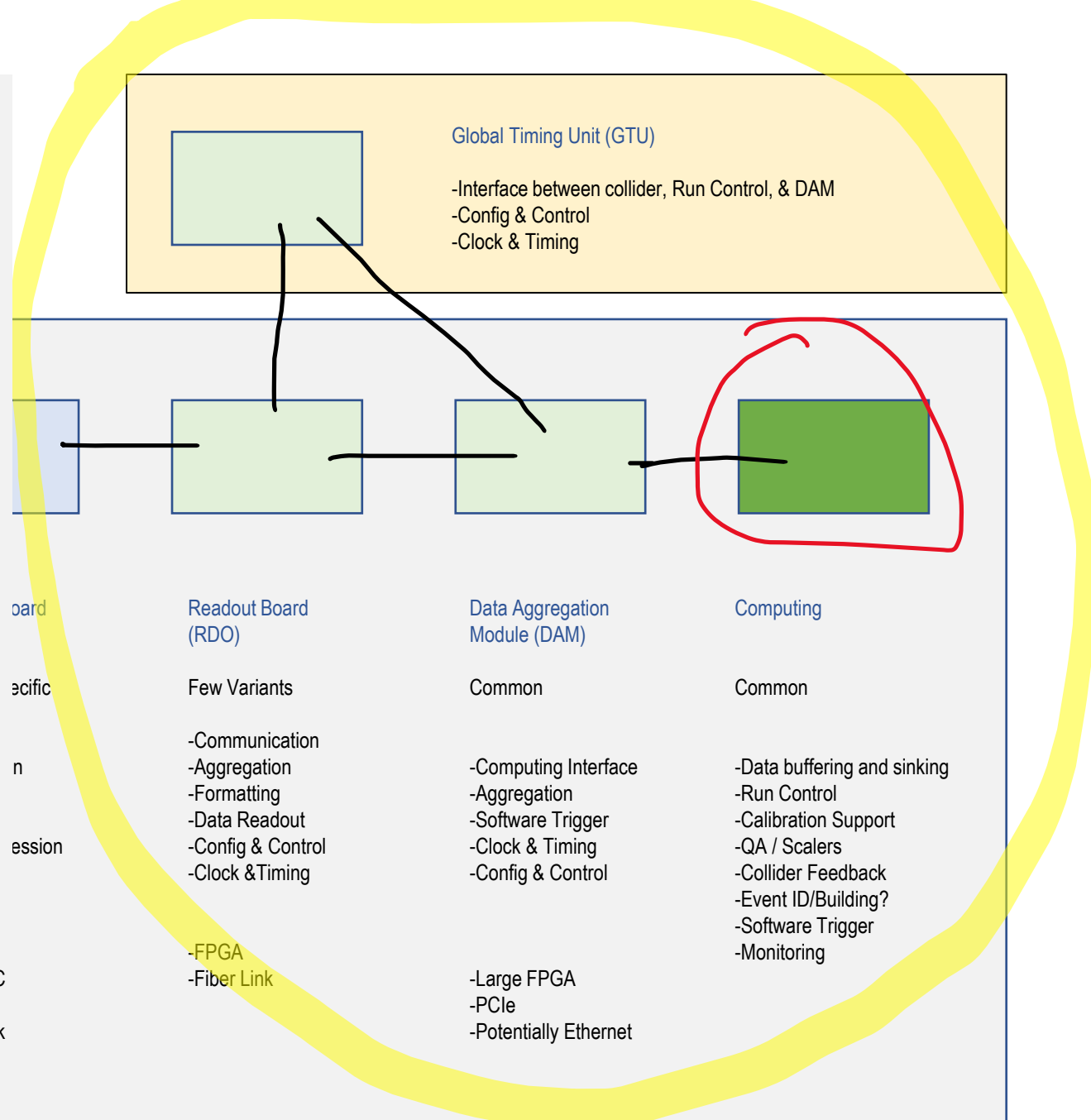


Many of us are assuming intermediate DAM boards
Are these housed in dedicated units, or in computers?

Complex Patch Panels (effectively electronics boards similar to sPHENIX SOB) Required. Is it enough to have single system or do we need this in multiple places?

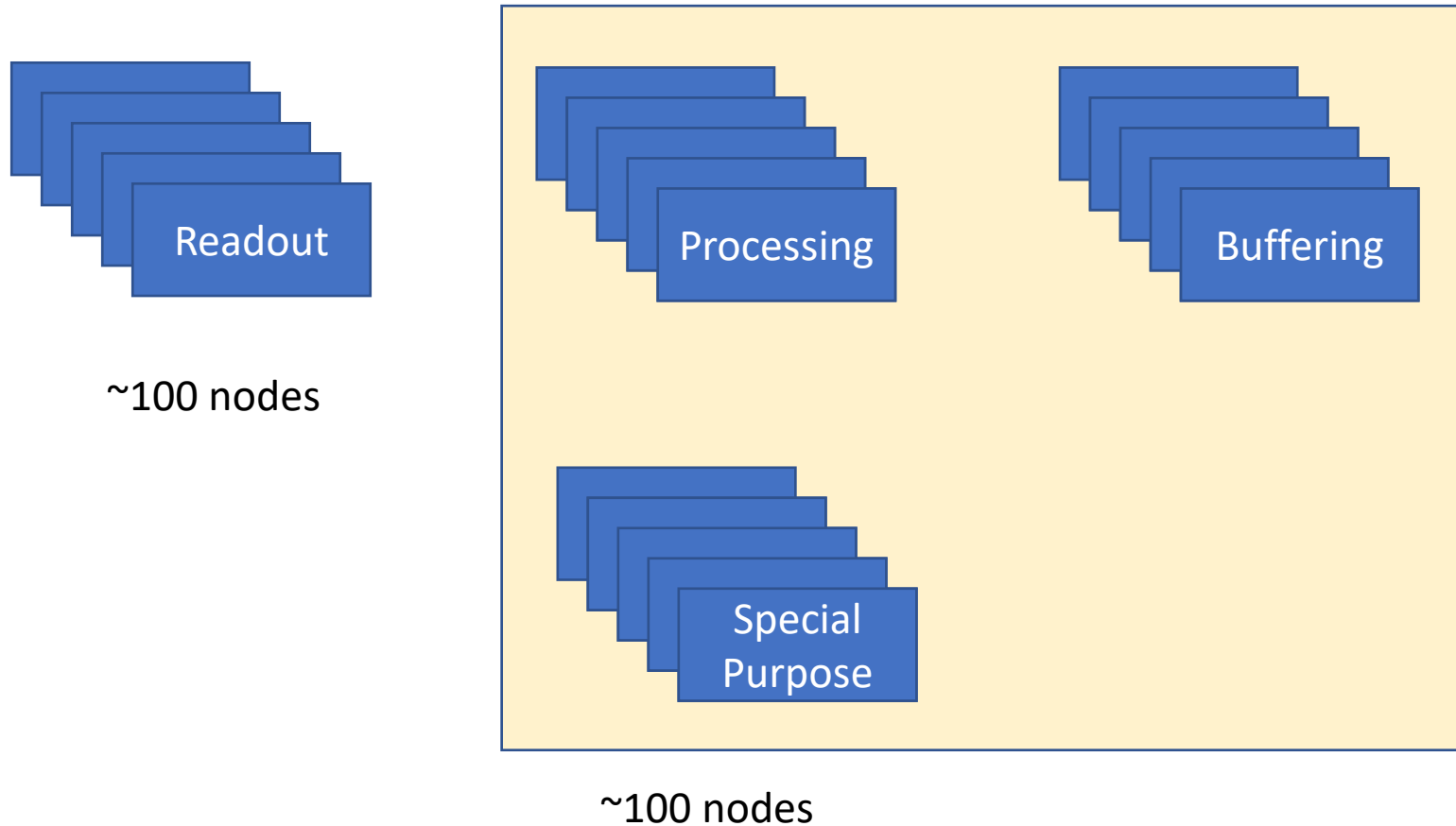
Is it important that fiber bundles be maintained as close to detector as possible, or can fibers be easily rebundled?

RDO / DAM connections



Attributes	Sensor Specific	ASIC/ADC	FPGA	Large FPGA
-MAPS -AC-LGAD -MCP-PMT -SiPM -LAPPD	-Sensor Specific -Passive	-Discrete -Serial Link	-FPGA -Fiber Link	-PCIe -Potentially Ethernet

Computing Farm Ethernet Connectivity



Expect 5 networks

- General EPIC Control Room
 - Small subset, mainly in special purpose category
- DAQ private
 - Large bladed switch system ~200 direct connections (patch panels for distribution)
- Slow Controls Private
 - Small Subset of DAQ computers
- Computing Center Private
 - Small subset, only in buffering category
- CAD private
 - Small subset