OAK RIDGE National Laboratory

Kapton Flex Hybrid R&D Plans for the ePIC TOF Barrel

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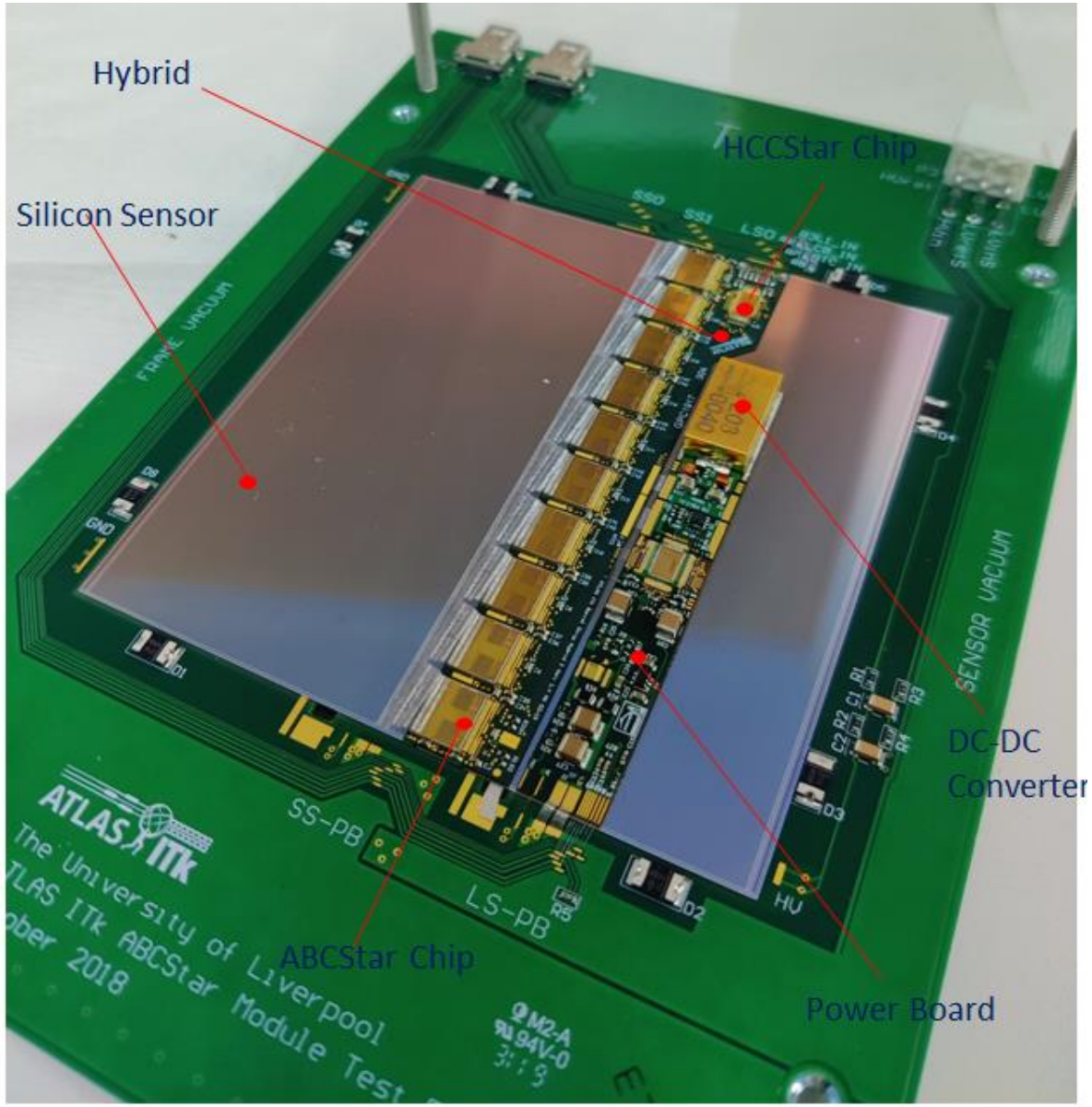
U.S. DEPARTMENT OF ENERGY

Barrel TOF Flex PCB

- Connect 64 ASICs (+X) along stave to RDO at end of stave
  - Low voltage, bias (HV), ground
  - Differential e-links, **clocks**, slowcontrol/I^2C?
  - Individual ASIC output data rate is only ~Mbit/s (based on Tonko's initial estimates)
- Low mass: 1% X/X_0 total barrel material budget
- Needs to fit barrel TOF geometry
  - ~1.2m length
- Kapton flex PCB:
  - Custom geometry "sandwich" of thin kapton and conductor layers
  - Used in other tracking detectors already

PID-TOF	3M-50M	240-500	6Gb/sec	12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm

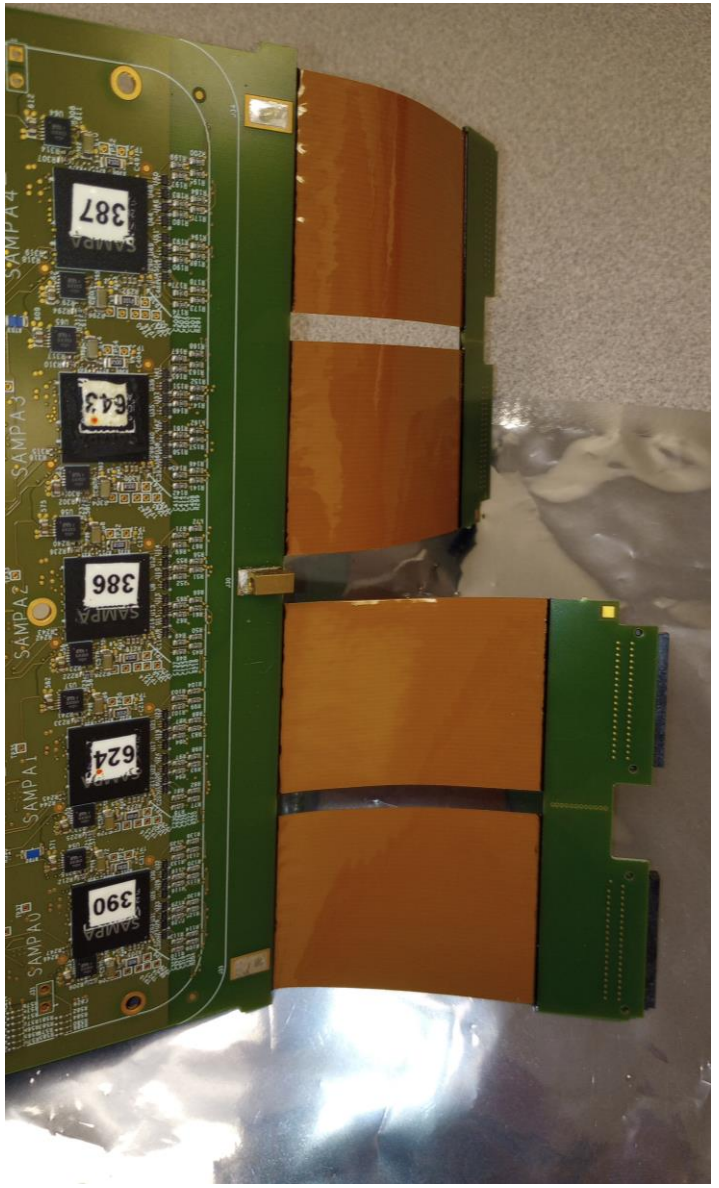
Example: ATLAS ITK Strip Module



Courtesy of Francesca Capocasa (Brandeis/BNL)

Technological Survey

- Available vendors
  - Available materials, thicknesses, sizes…
  - Cost, timelines, volume production capabilities
- Max size: 1m?
  - Might require connectors or "Origami" to cover full stave
- ORNL Flex PCB experience from ALICE BTU project
  - "TTM Technologies" produced ALICE BTU flex PCBs



Simulation and Design

- LV/HV
  - Required material budget for current requirements
  - How much DC-DC converters for given ASIC?
  - Serial powering?
  - Design requirements for HV conductors
- Differential links:
  - Insertion losses, analog bandwidth for different lengths
  - **Crosstalk on clock line(s)!**
  - Ultimately informs output drive strength
- Common flex foil, or separate for LV/HV/RF?
- Supported by ORNL electrical engineering

Test Structure and Measurements

- Cannot go for a functional prototype in any case.
  - Too many unknowns now and in the near future
- Design test prototype: As long as possible
  - Differential link loops at various lengths, geometries (?)
  - LV/HV conductors
- RF testing:
  - Confirm simulations: bandwidths, insertion losses, crosstalk
  - Test link speed/BER with FPGA, edge jitter
  - Ideally integration into timing distribution test bench at ORNL
- DC testing:
  - Acceptable voltages, currents, resistances
- Mechanical:
  - Thermal cycling
  - Handling, bending, folding

Summary/Timeline

- Technological survey: compare vendors and capabilities
- Design + simulation: by ORNL EE groups
  - by August ‘23
- Prototype fabrication at vendor
  - by November ‘23
- Prototype evaluation in lab

Budget Request

Inst.	Personnel		Budget (k$)
	Readout and Timing Distribution R&D		
BNL	Electrical Engineer		38
BNL	Staff Scientist	2x0.2 FTE	0 (in-kind)
BNL	Xilinx Dev. Kit		4
BNL	Timing Chips + Boards		15
BNL	Travel Support		5
	Barrel Service Hybrid R&D		
ORNL	Electrical Engineer		32
ORNL	Staff Scientist	0.1 FTE	0 (in-kind)
ORNL	Materials and Supplies		8
ORNL	Xilinx Dev. Kit		4
	Endcap Service Hybrid R&D		
Rice	Electrical Engineer	0.15 FTE	18
Rice	Faculty	0.1 FTE	0 (in-kind)
Total			**116**

Table 22: Budget request for the TOF system readout electronics R&D in FY23. All entries in thousands of dollars.