First ideas on serial powering for the ePIC SVT

L. Gonella (Birmingham), P. Phillips (RAL), I. Sedgwick (RAL), F. Wilson (RAL)

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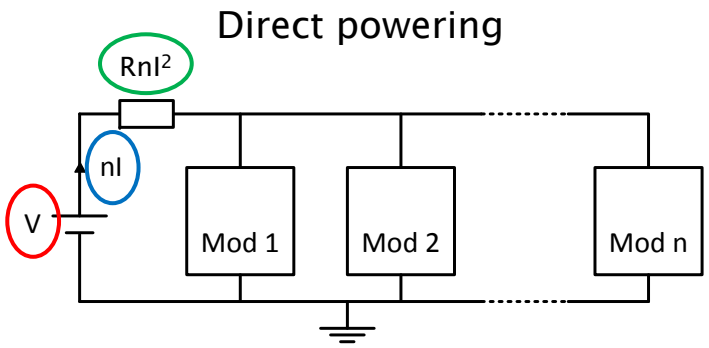
Outline

- Serial powering basics
- Example: ATLAS ITk pixel detector
- Possible implementation for ePIC SVT

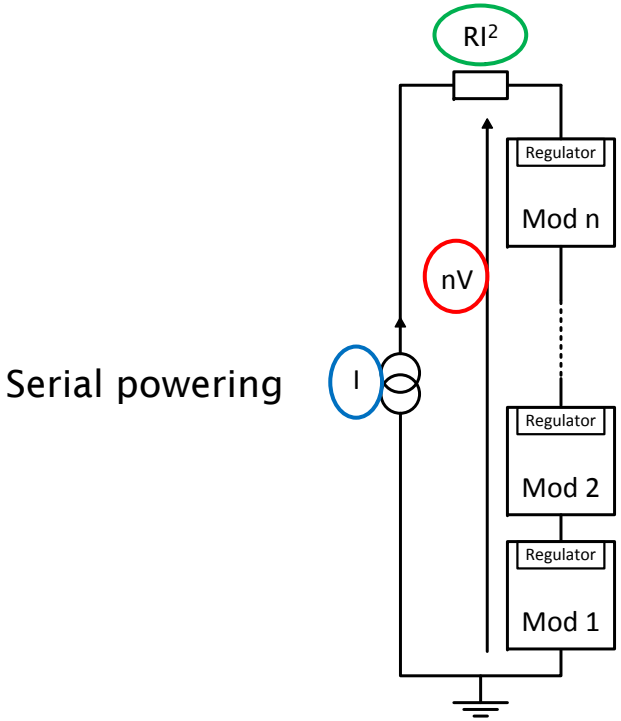
Serial powering basics

- Serial powering is a current based powering scheme, where modules are powered in series by a constant current.
  - The current to voltage conversion is done by regulators on module.



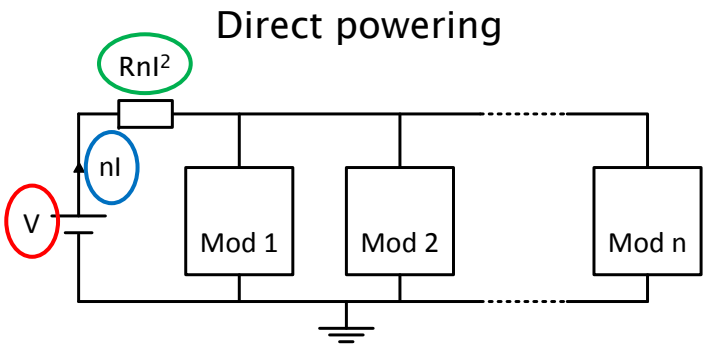
- In a serial powering chain made of n modules, the transmitted current is only the current needed by one module, I.

- For n modules powered in series, the current is reduced of a factor n with respect to a direct powering scheme → Higher power efficiency and reduced cable volume.
  - Cable cross-section and the power losses on the cables scale by the same factor.

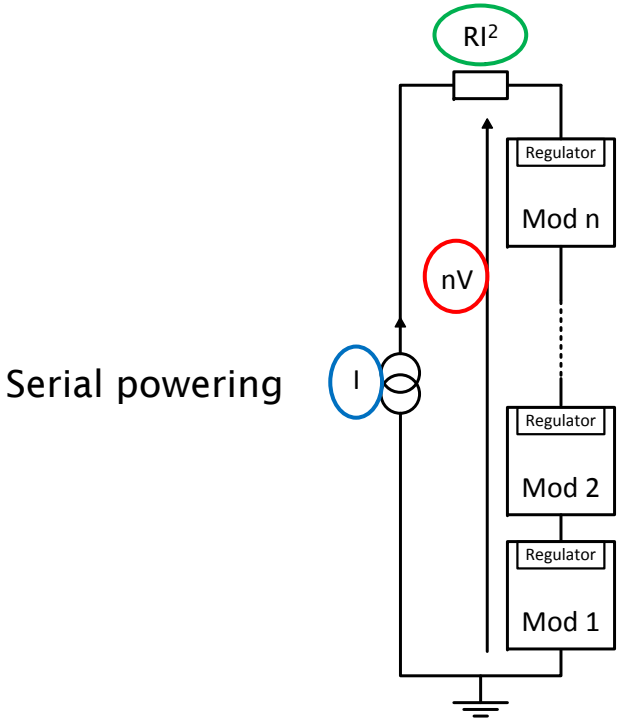


Serial powering basics

- As the modules are powered with a constant current, V_{drop} is not constrained as in a voltage based powering scheme.
  - It can in principle be chosen only depending on the output voltage capability of the current source and of the allowed power density (i.e. cooling capability).



- Higher V_{drop} can be allowed in the active area of the detector to reduce the material budget of the cables.
  - Outside the detector the voltage drop can be reduced to lower the power losses.

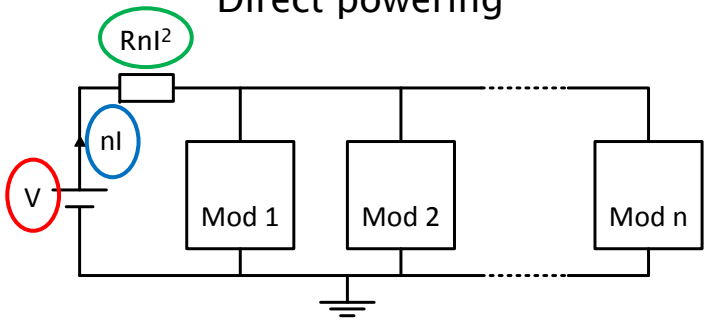


- With respect to voltage based powering schemes (incl. DC-DC), serial powering allows more flexibility in the optimization of material and power efficiency.

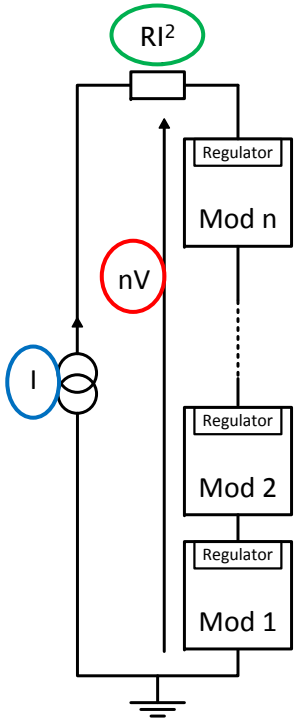
Serial powering basics

- The voltage across the chain is nV, where V is the voltage on a module.
- Each module sits at a different ground potential.
- AC coupled data transmission required.
  - DC balanced data protocol (e.g. 8b10b).
  - Self biased receiver inputs to set the common mode voltage.

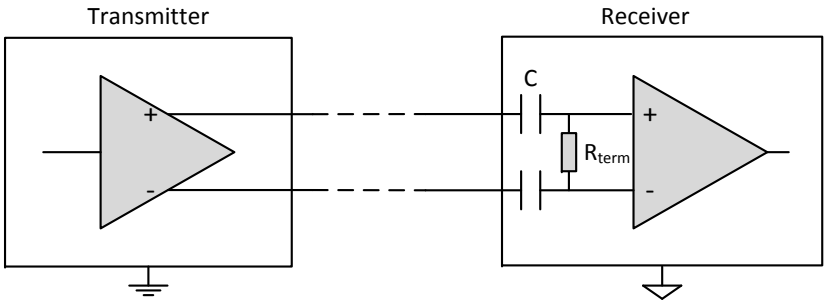
Direct powering



Serial powering

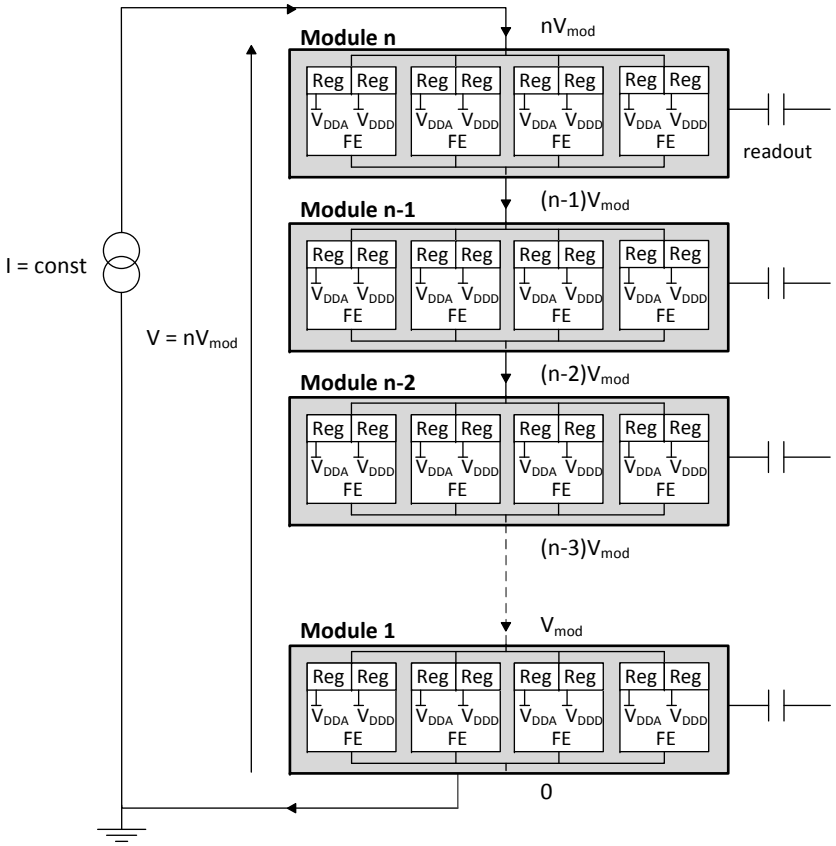


Sketch of a AC-coupled LVDS link



Example: ATLAS ITk detector

- The ATLAS pixel detector at the HL-LHC adopted serial powering (also the CMS pixel detector).
- Each module is made of a sensor bump bonded to a certain number of readout chips.
  - In the sketch, four readout chip per module (FE).
- The current flows in series between modules and in parallel between readout chips on a module.
- In each chip, two shunt-LDO regulators generate the analogue (V_{DDA}) and digital (V_{DDD}) voltages.

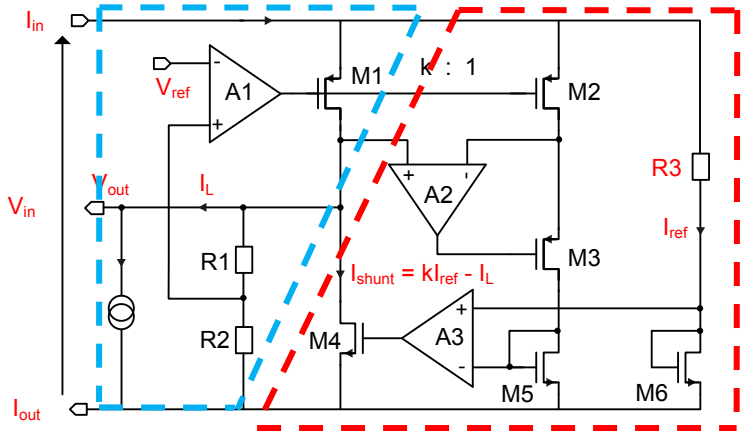


The shunt-LDO regulator

- For this powering scheme, on-chip regulators are needed that can:
  - Operate in parallel;
  - Generate different output voltages out of the current supply;
  - Shunt additional current in case of device failure.

- The Shunt-LDO regulator was designed to match these requirements.
  - First version in the ATLAS pixel FEI4 chip (180 nm process).
  - Full SP version in the RD53 chip (65 nm process).

- It combines two regulation loops.
  - Shunt regulation circuitry → regulates the current to the chip.
  - LDO (Low Drop Out) regulation loop → generates the voltage for the chip.

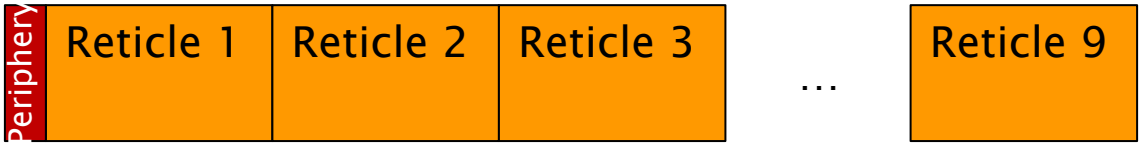


Some references on ATLAS SP & Shunt-LDO

- L. Gonella, PhD thesis, https://cds.cern.ch/record/1633150?ln=en
- L. Gonella, D. Arutinov, M. Barbero et al. 'A serial powering scheme for the ATLAS pixel detector at sLHC'. In: JINST 5 (2010), p. C12002. doi: 10.1088/1748-0221/5/12/C12002.
- M. Karagounis, D. Arutinov, M. Barbero et al. 'An Integrated Shunt-LDO Regulator for Serial Powered Systems'. In: Proc. of the European Solid-State Device Conference, ESSCIRC 2009 (2009), pp. 276–279. doi: 10.1109/ESSCIRC.2009.5325974.
- L. Gonella, M. Barbero, F. Huegging et al. 'The shunt-LDO regulator to power the upgraded ATLAS pixel detector'. In: JINST 7 (2012), p. C01034. doi: 10.1088/1748-0221/7/01/C01034.
- M. Karagounis, Shunt-LDO RD53B features, talk, 2020 https://indico.cern.ch/event/879686/contributions/3706455/attachments/1975390/3287622/SLDO_RD53B_Features.pdf
- F. Winkler, Verification of Shunt-LDO, Master Thesis, 2019 https://d-nb.info/1237320216/34

Possible configuration for the ePIC SVT

- The ePIC SVT will be made of MAPS sensors consisting of single rows of (up to 9) stitched reticles, with the periphery at one end.



- Consider the substrate of the MAPS as the sensor and the reticules as the chips → an epic SVT MAPS sensor can be seen as an ATLAS ITk pixel module.

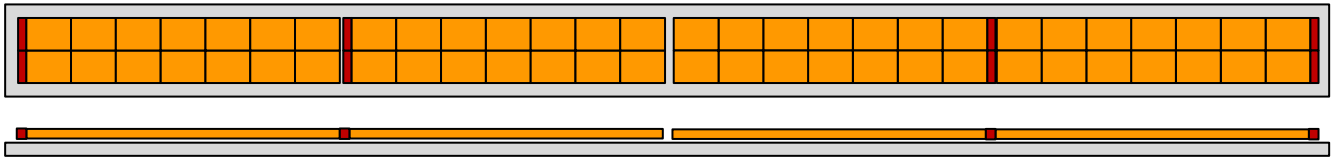
- Following the ATLAS scheme, for the ePIC SVT:
  - The current would flow in series between MAPS sensors.
  - Shunt-LDO regulators on the MAPS sensor will generate the required voltage(s) and regulate the current to the load.

- Note, direct powering is assumed for the vertex layers (for now).

Possible architecture for barrel layers

- The outermost sagitta layer, L4, is made of 1x7 sensors, it is two sensors wide and four sensor long (8 sensors per stave).
  - See baseline ePIC SVT configuration at https://indico.bnl.gov/event/17713/

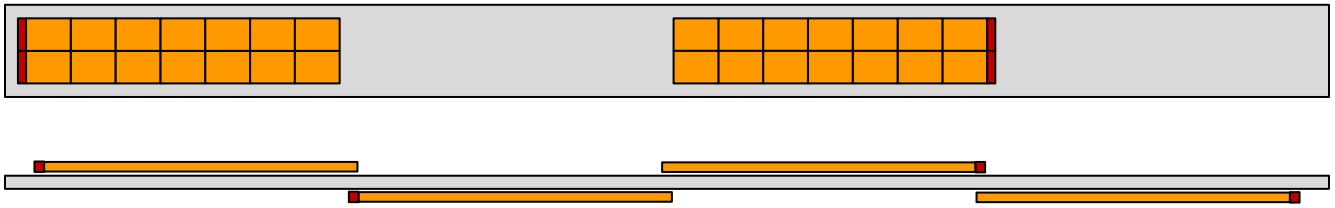
- Top and side view of L4 (the stave is in grey).
  - Services would come in from the two sides.
  - The orientation of the periphery is to reduce the amount of services running on the stave.



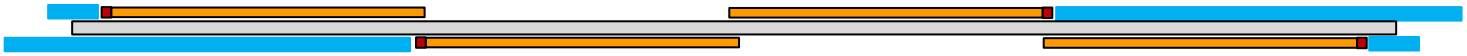
- This simple configuration however leaves dead areas between sensors.
  - Periphery will need to be bonded to services flex/tape on stave, space not shown in this drawing.

Possible architecture for barrel layers

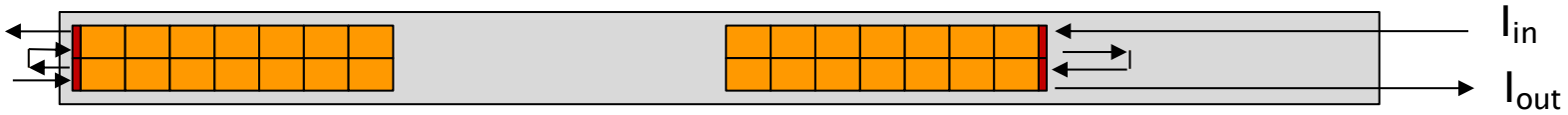
- Sensors will most likely be needed on two sides to provide overlap.
  - This has an impact on the stave design, i.e. a truss structure would not be possible.



- In this configuration services could run as shown in blue.



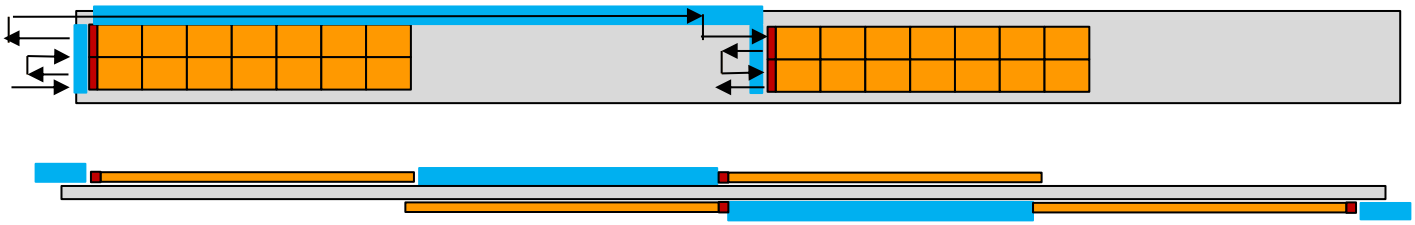
- If now serial powering is added, this would mean four chains of two sensors per stave → the total current to L4 scales of a factor 2



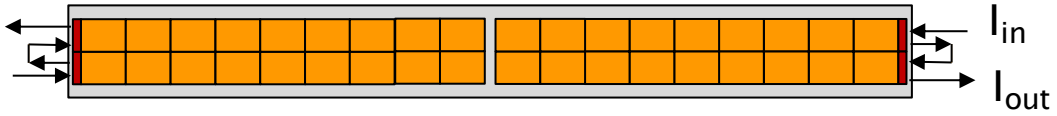
Similar on the bottom

Possible architecture for barrel layers

- Another possibility would be as shown below, giving a reduction factor 4 in the total current to L4



- For the innermost sagitta layer (L3), we would have chains of two sensors, giving a reduction factor 2 in the total current to L3
  - Made of 1x9 sensors, it is two sensors wide and two sensor long (4 sensors per stave).
  - Services come in from the side and connect to periphery at end of stave to minimise material.



  - Note that most likely also in this case we might need sensors on two sides to avoid the gap in the middle.

Shunt-LDO: integrated or standalone

- This scheme implies the use of the Shunt-LDO, ideally integrated in the MAPS sensor.
- Implement Shunt-LDO in TJ 65 nm stand-alone block in ER2 to evaluate performance.
- Integrated version would need to wait first EIC LAS submission (currently scheduled tentatively for Q2-24).
- Backup option: standalone regulator.
  - Prototype Shunt-LDO design in TJ 180 nm MPW.
  - This would be positioned on the stave flex/tape, where the AC-coupling capacitors also are.

Next steps

- Reach out to RD53/Shunt-LDO designers to discuss regulator design (possibly IP sharing) and start design for submission with ER2 and standalone.

- Work on the current ideas to study engineering aspects of power and data distribution.

- Start exercise of evaluating material saving, to be refined as concept gets more detailed.

- Start thinking of conceptual design of SP scheme for disks.

What about DC-DC conversion?

- Some ideas were also discussed by Birmingham & RAL, will be presented another time.