

ROC Port Status Sent to BNL

2023/02/09 Kazuma Fujiki

Port Status at Glance

FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		

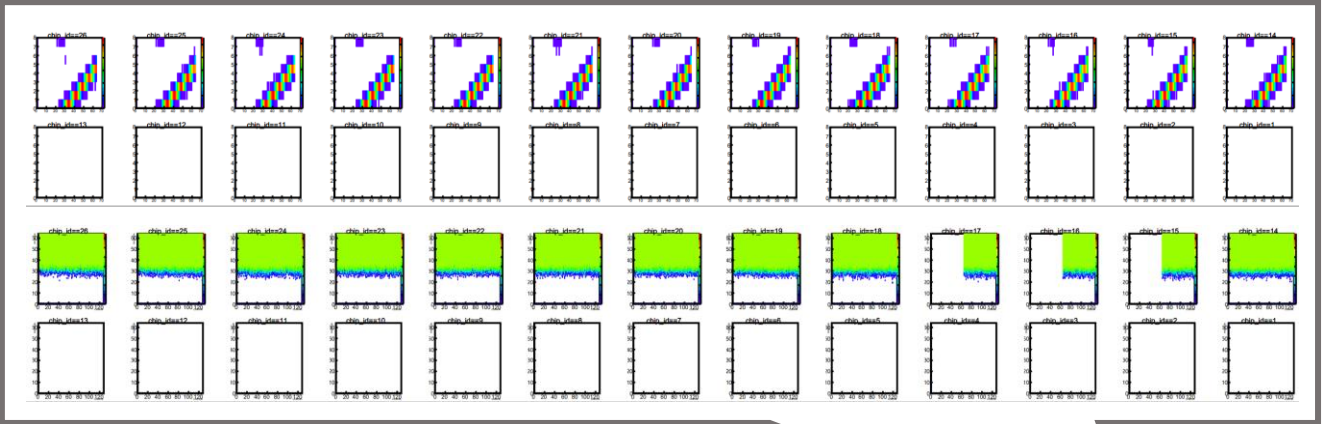
NW3

FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		

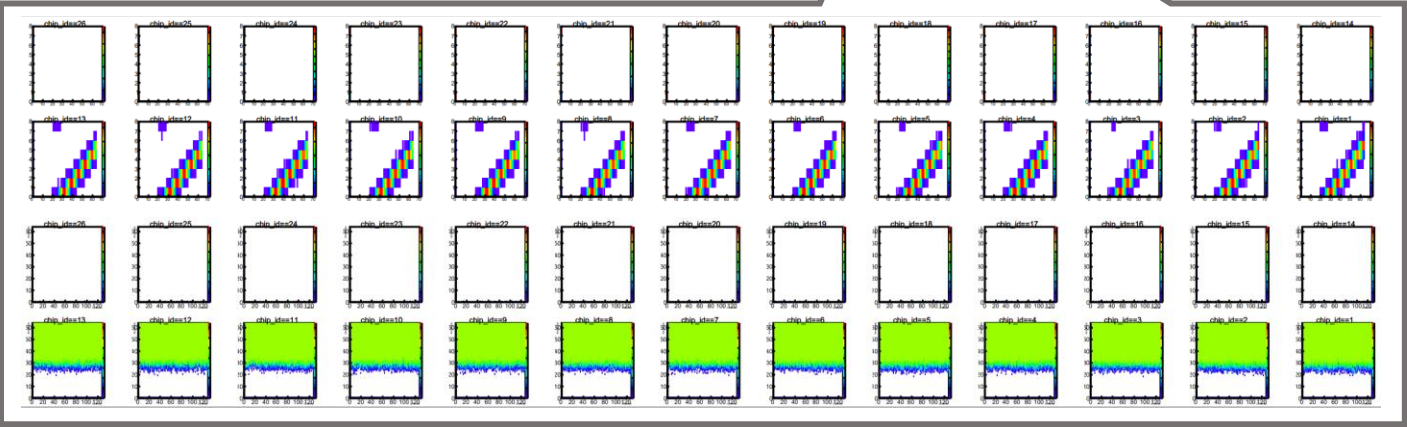
NW4

FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		

NW4



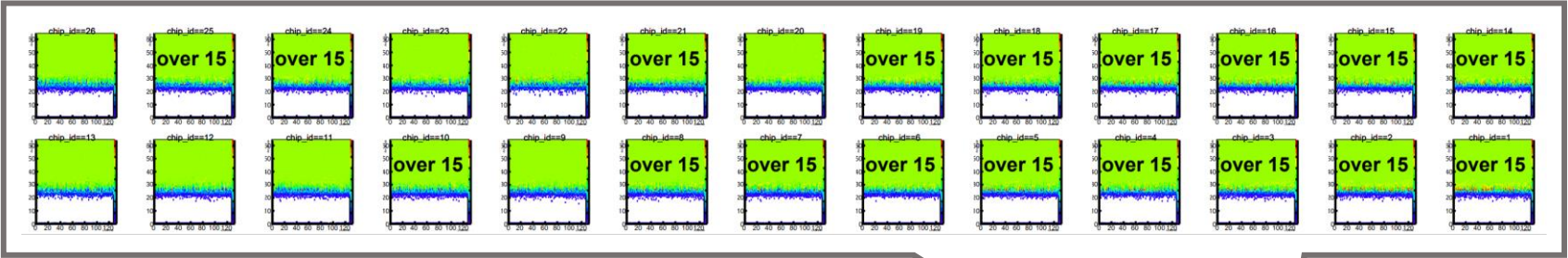
FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		



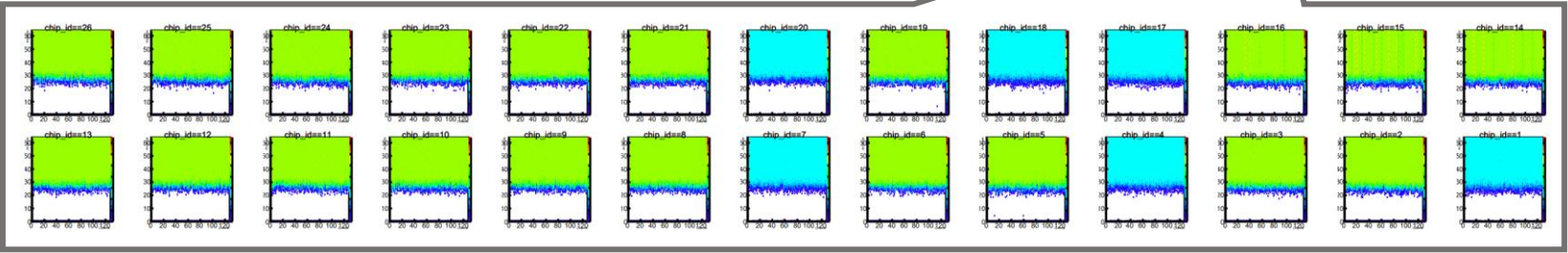
NE1

FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		

NE1



FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		



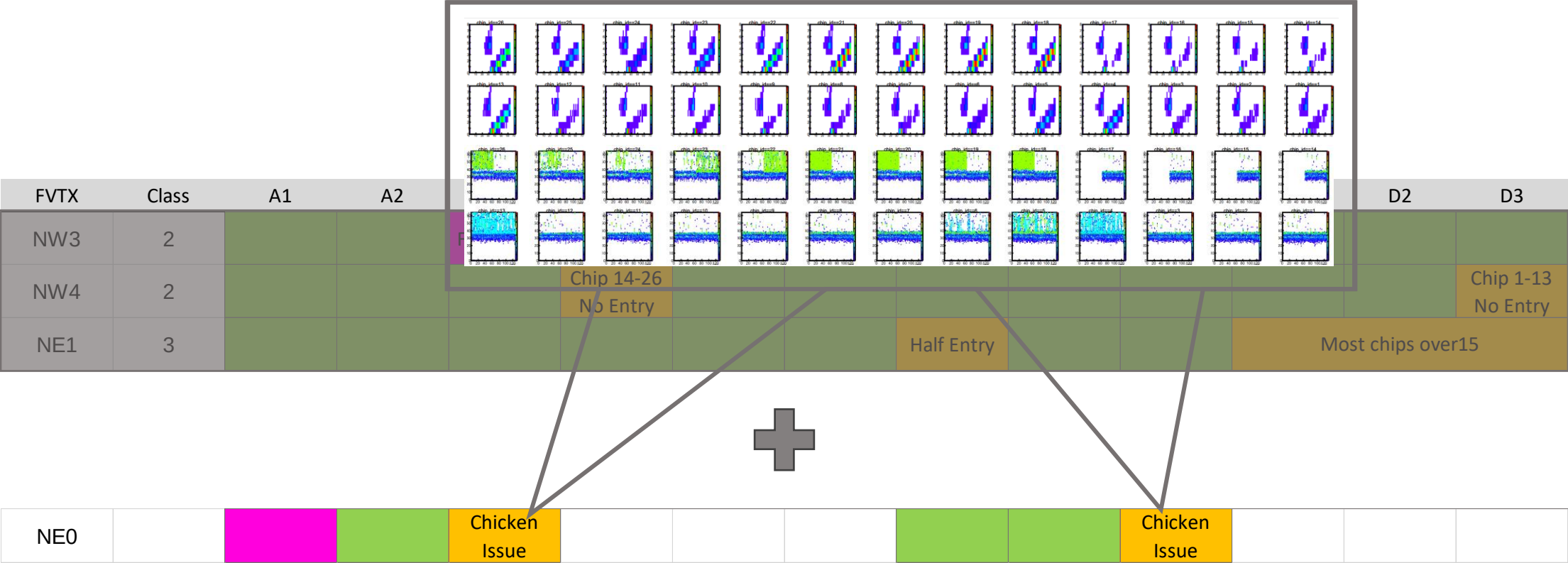
NE0

FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
NW3	2			Fiber Latch									
NW4	2				Chip 14-26 No Entry								Chip 1-13 No Entry
NE1	3							Half Entry			Most chips over15		



NE0				Chicken Issue						Chicken Issue			
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NE0



Improvement Plan

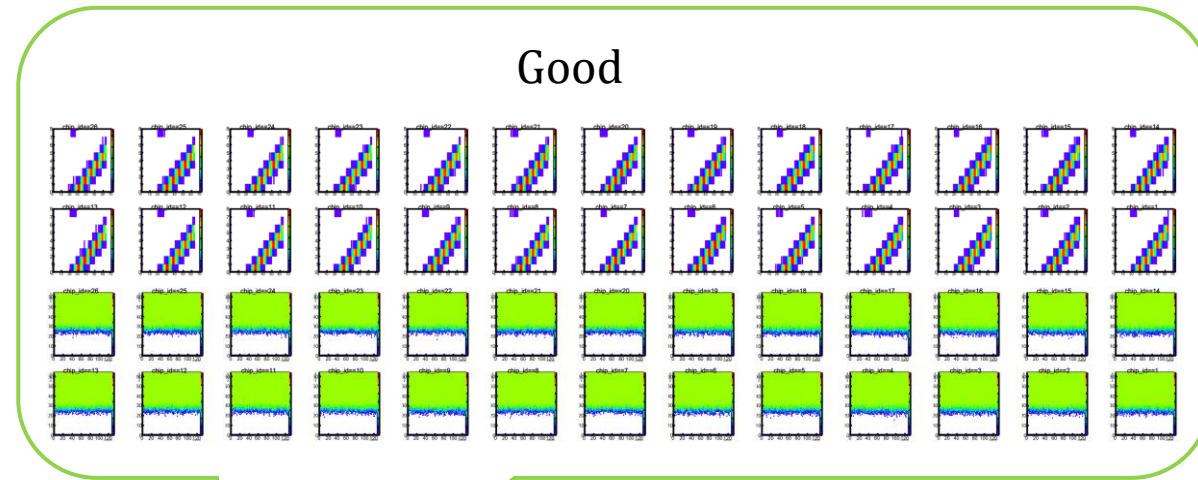
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Improvement Plan

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Back Up

Introduction



ROC #	FVTX	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3
22	SE2	2										F	F	
24	SE4	2									All Chips Few Entries		F	
17	NW3	4												
2	NW4	3				Chip 14~26 No Entry	Doesn't stick to DF18		F					Chip 1~13 No Entry
3	NW5	2						F						
21	-	2									Chip 1~13 Noisy			Chicken Issue

Class 1 ... 12 Good ports
 Class 2 ... 10, 11 Good ports
 Class 3 ... 8, 9 Good Ports
 Class 4 ... Less than 7 Good ports

No data at all

Bad

Improvement Plan

