Microelectronics (and HEP)

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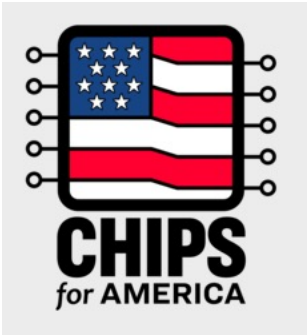
P5 Townhall at BNL
April 12 - 14, 2023

National Microelectronics Initiative

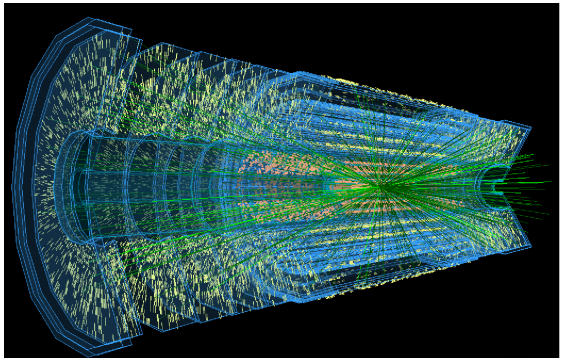
- Continued innovation and development in microelectronics is critical to US technological leadership, and to the country's economic and national security
- While the US remains a world leader in microelectronics design, it has fallen behind in manufacturing, currently accounting for only ~10% of global microelectronics production
- The "Chips and Science Act" ($280B over 10 years, signed into law on Aug. 9/2022) seeks to "boost American semiconductor research, development, and production, ensuring U.S. leadership in the technology that forms the foundation of everything from automobiles to household appliances to defense systems."
  - "The majority—$200 billion—is for scientific R&D and commercialization. Some $52.7 billion is for semiconductor manufacturing, R&D, and workforce development…"

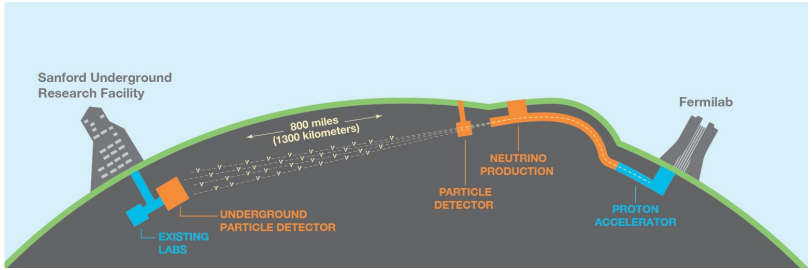
(https://www.mckinsey.com/industries/public-and-social-sector/our-insights/the-chips-and-science-act-heres-whats-in-it)

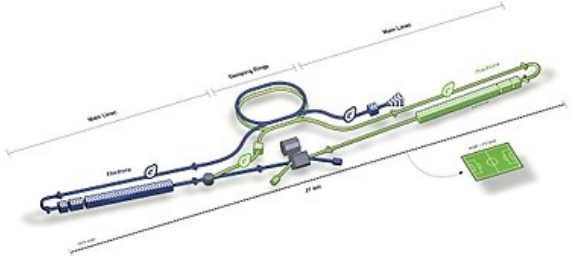


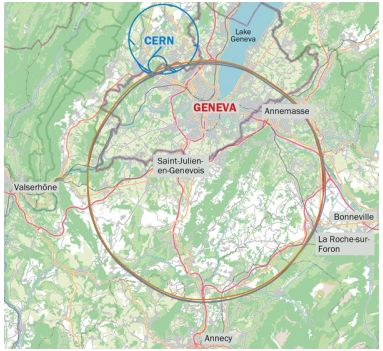
Microelectronics in HEP

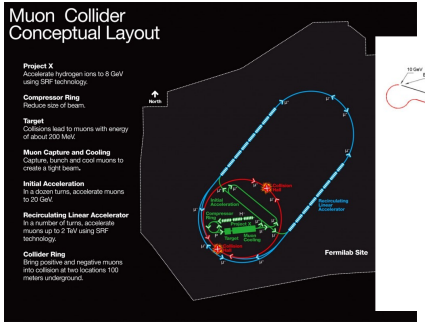
- We have many options being considered for “what comes next” in expt HEP
- An omnipresent theme is that our continued development of microelectronics, and the availability of advanced technology to enable us to do so, are critical to our ability to meet our ambitious physics goals

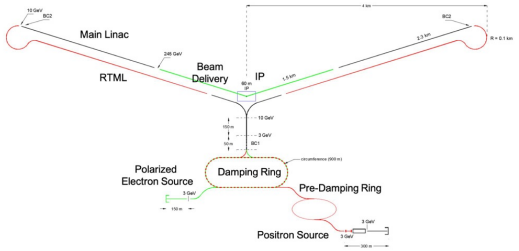






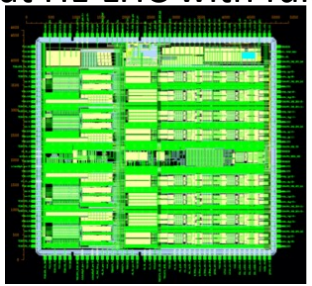




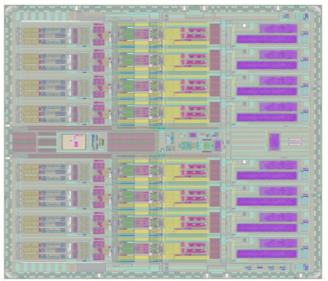


Selected Examples from HL-LHC

- HL-LHC calorimetry readouts need to maintain precision despite much higher readout rates than current LHC readout (at L1 trigger rate of up to 100 kHz)
  - ATLAS HL-LHC LAr will implement trigger-less readout at HL-LHC with full precision at 40 MHz bc rate, leading to ~200X larger readout data volume
  - LAr FE relies on several full-custom ASICs, including:
    1. "ALFE" Preamp/Shaper ASIC (130 nm CMOS) with 16-bit dynamic range
    2. "COLUTA" ADC ASIC (65 nm CMOS) with 15-bit dynamic range and ENOB > 11

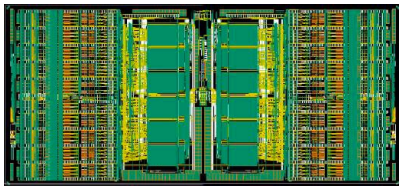


ALFE2 Layout: 4.6 mm x 5.3 mm



COLUTAv4 Layout: 5.5 mm x 5.8 mm

  - CMS High Granularity Endcap Calorimeter (HGCAL) has > 6 million readout channels, and DAQ path will be read out at 750 kHz rate. Again, replying on full-custom ASICs, including:
    1. "HGROC" ASIC (130 nm CMOS) with 16-bit dynamic range and providing both Q and t values
    2. ECON-T provides data concentration/compression on trigger path, and includes configurable neural net (NN)



HGROC3 Layout: 15 mm x 6 mm

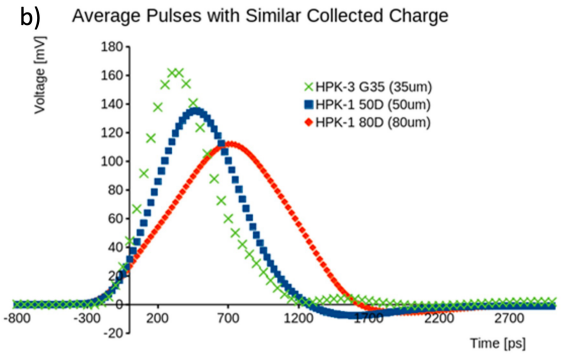
Input from Snowmass

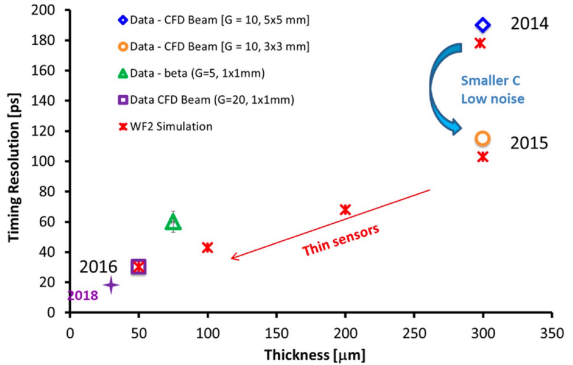
- As part of the Snowmass 2021 process, the Instrumentation Frontier included a working group on Electronics and ASICs [convened by G. Cabrini (BNL), M. Newcomer (U Penn), JP]. The report (see https://www.slac.stanford.edu/econf/C210711/reports/2209.15519.pdf) identified several overarching goals for enabling continued progress in the future:
  - Development and support of the workforce for HEP instrumentation
  - Providing broader and shared access to advanced technology
  - Continue to adapt to enable operation in extreme environments (such deep cryo., ultra-radio pure materials, radiation-harsh settings, low power budgets, long duration expts)
  - Develop novel techniques to manage very high data rates
  - Create framework and platform for easy access to design tools
- These themes align with the conclusions of the 2019 BRN report (see https://doi.org/10.2172/1659761)
- The Snowmass 2021 Electronics and ASICs working group also identified a number of areas of focus to meet the needs of future HEP experiments; I give a few selected examples in the subsequent slides

Electronics for Fast Timing

https://arxiv.org/abs/2204.00149

- Future (and even current) detectors are moving toward “4D” readout (x,y,z,t) for tracking, and “5D” for calorimetry (adding in energy also)
- Timing information is becoming increasingly important in implementation of “particle flow” reconstruction techniques
- Recent advancements achieved on both detectors (eg. LGADs being deployed by both CMS and ATLAS in HL-LHC) and required fast electronics (SiGe or CMOS)
  - Interesting potential for other applications, such as medical imaging, accelerator monitoring, ...

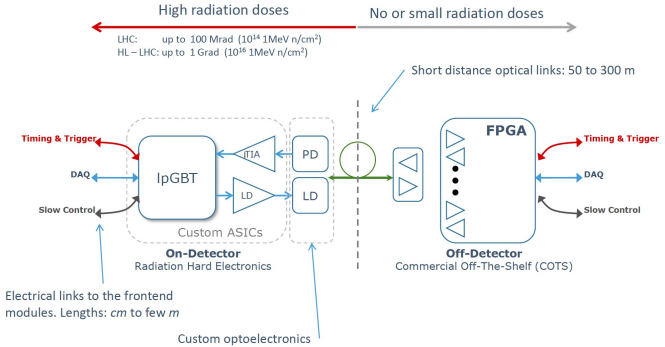




Optical Links

https://arxiv.org/abs/2203.15062

- The 10.24 Gbps links developed for HL-LHC (including lpGBT ASIC and VTRx+ optical transceiver) are not keeping up with rates of ~56 Gbps in industry.



  - Lower bit-rate per fiber results in inefficient fiber plants and low efficiency use of off-detector FPGA serdes inputs (eg. ATLAS HL-LHC LAr readout requires 33,528 readout fibers at 10.24 Gbps each)
- Future expts will need higher rates, which will require moving beyond 65 nm processes.
- R&D efforts include a shorter-term goal of reaching 20 Gbps in 65 nm, and also aiming for 56 Gbps per fiber in 28 nm CMOS

RF Electronics

https://arxiv.org/abs/2204.01809

- Industry-led advances in wireless communication (eg. RFSoC) have dramatically improved the sensitivity and capabilities of RF-related detection systems
- These advances can be exploited for a wide variety of physics measurements (eg. CMB, 21 cm cosmology, UHE neutrinos and cosmic rays, axion searches)

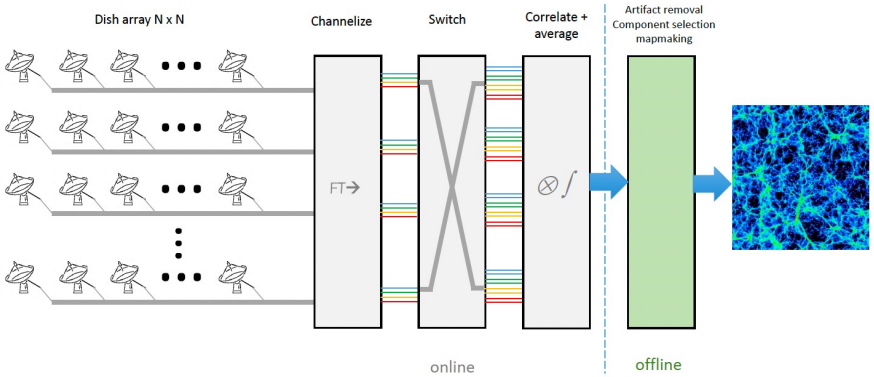
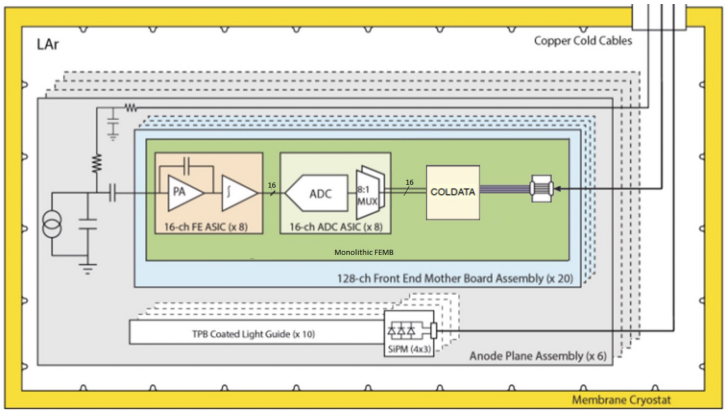


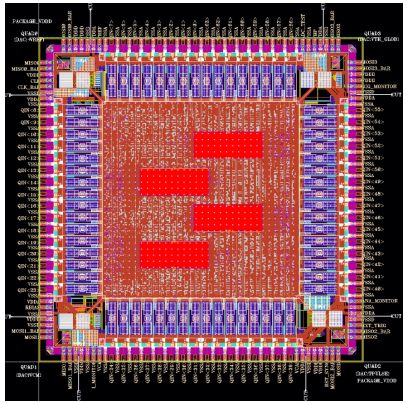
Figure 7: Illustration of anticipated data flow in a large interferometric array. Conversion of waveform data to frequency space, e.g. channelization, is accomplished close to each receiver; coincident data for each frequency bin are collected from all stations through a cross-bar switch (also called a "corner-turn" operation); correlations are constructed for each frequency bin, which can then be time-averaged and stored, followed by physics analysis.

Cryogenic Readout

- Many HEP applications (eg. direct Dark Matter searches, LAr-TPC neutrino expts) require electronics operating at temperatures from (typ.) few K to 90K. Extra development effort is needed since process models do not usually cover these temperature ranges
  - eg. the scale of the DUNE Far Detector (FD) dictates the need for cryo FE readout, which has been implemented in set of 3 custom ASICs (PA/S, 2 MSPS ADC, Serializer).



- LArPix ASIC developed for pixelated LAr readout for DUNE Near Detector (ND), needed due to high neutrino-interaction event rates (concept also considered as option for Modules 3-4 of DUNE Phase 2)

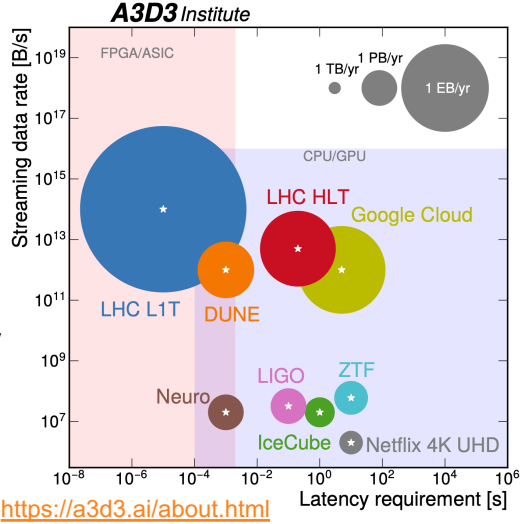


- Deep cryo. (ie. mK) performance is also increasingly important, driven by needs of quantum computing (see separate QIS talk at this P5 Townhall)

Smart Sensors Using AI/ML

https://arxiv.org/abs/2204.13223

- Across many aspects (scientific, industrial, commerical) of society, the use of AI/ML techniques is exploding (see separate AI/ML talk in this P5 Townhall)
- In HEP, AI/ML techniques are very widely used in offline data analysis, and are being increasingly used in real-time applications in off-detector electronics (eg. TDAQ)
- However, the rapidly increasing FE data volumes will require real-time data reduction as close to the data source and sensors as possible, naturally leading toward the implementation of AI/ML techniques in on- and near-detector electronics.
- In many ways, the HEP requirements exceed those of other applications, and will require specialized developments
  - Advances very applicable to provide a broader impact to society

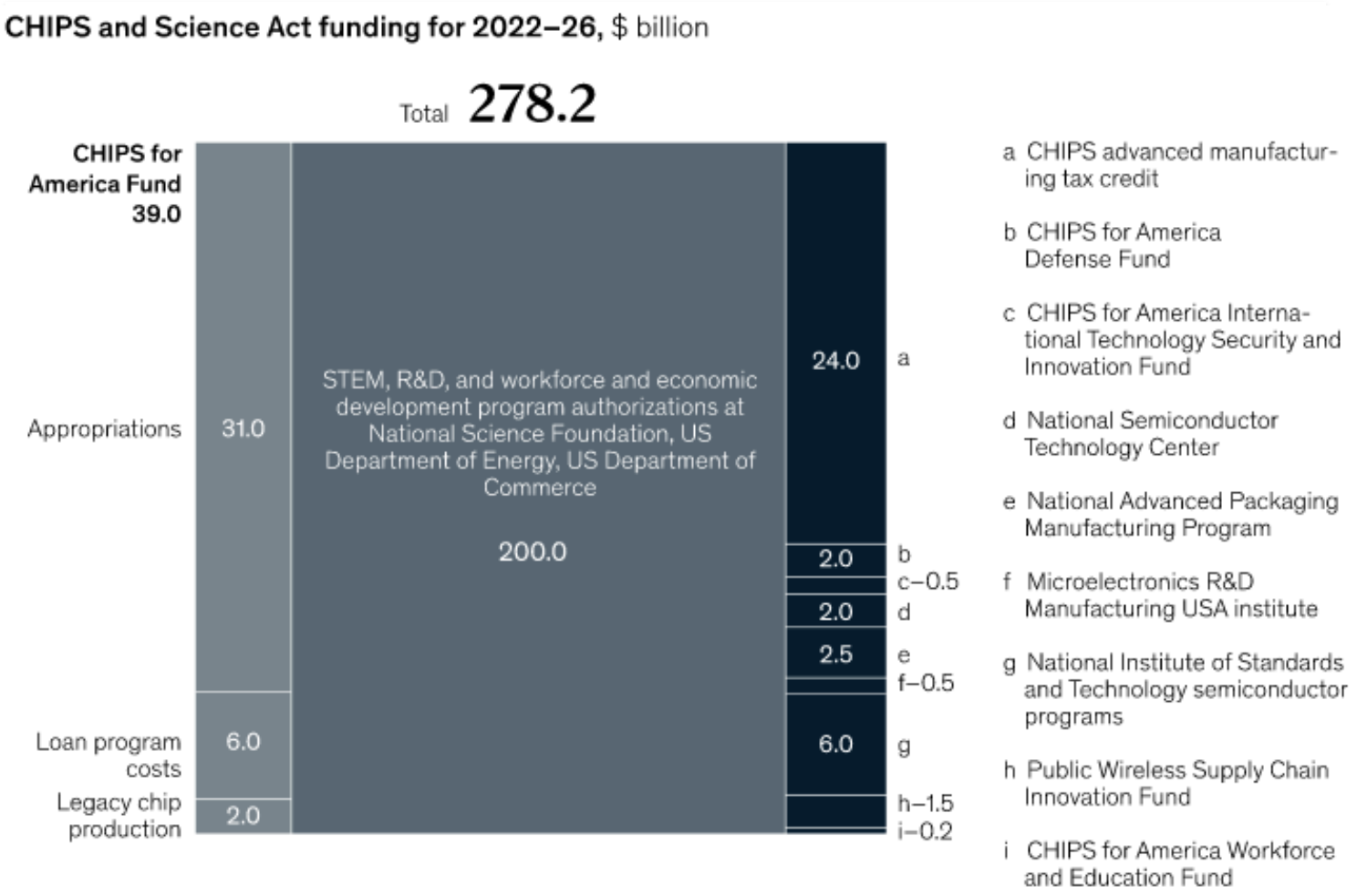


https://a3d3.ai/about.html

Closing Remarks

- As in the past, our prospects for meeting the physics goals of future HEP experiments will depend critically on our ability to develop “beyond-the-start-of-the-art” instrumentation and techniques, including new detectors and the requisite microelectronics, novel algorithms and analysis techniques, etc.
- We face a variety of very interesting and challenging issues to continue to evolve our microelectronics to meet the needs of future HEP experiments, including:
  - Challenging environments (eg. high radiation, cryo temperatures, low power budgets, little to no accessibility for maintenance over long durations, etc.),
  - Ever-increasing performance demands (finer granularity, improved resolution, etc.) that lead to enormous growth in data volumes and processing requirements,
  - Maintaining and supporting (despite the long timescales) the skilled and experienced workforce that is essential to success,
  - Providing broad access to advanced technology.
- The national microelectronics initiative provides an opportunity for us to both advance our field and to contribute to developments that will lead to the wider advancement of society

Backup


CHIPS and Science Act funding for 2022–26, $ billion
Total 278.2
CHIPS for America Fund 39.0
Appropriations
31.0
Loan program costs
6.0
Legacy chip production
2.0
STEM, R&D, and workforce and economic development program authorizations at National Science Foundation, US Department of Energy, US Department of Commerce
200.0
24.0 a
2.0 b
c–0.5
2.0 d
2.5 e
f–0.5
6.0 g
h–1.5
i–0.2
a CHIPS advanced manufacturing tax credit
b CHIPS for America Defense Fund
c CHIPS for America International Technology Security and Innovation Fund
d National Semiconductor Technology Center
e National Advanced Packaging Manufacturing Program
f Microelectronics R&D Manufacturing USA institute
g National Institute of Standards and Technology semiconductor programs
h Public Wireless Supply Chain Innovation Fund
i CHIPS for America Workforce and Education Fund