Discrepancy of MIP Peak between 2019 and 2021 Beam Tests

RIKEN/RBRC

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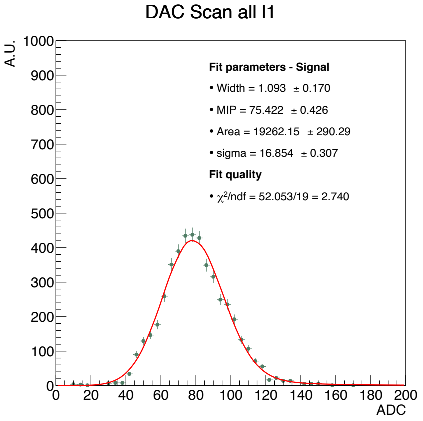
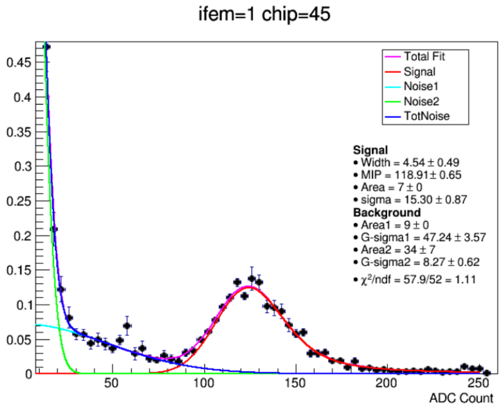
DAC scan comparison

https://indico.bnl.gov/event/15657/contributions/63079/attachments/40865/68318/INTT_energydeposit_summary.pdf

Testbeam2021, 50 V
Positron beam, 1 GeV



Testbeam2019, 100 V
Proton beam, 120 GeV



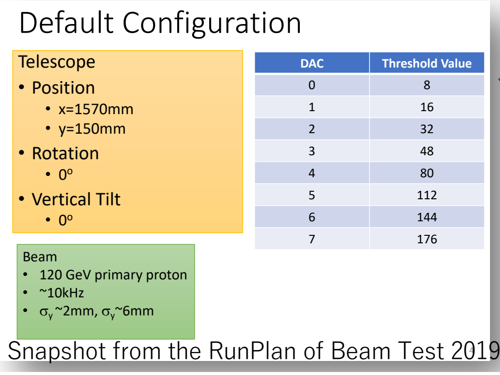
2021 Test beam was operated at 50V instead of 100V. However, observed MIP peak position (collected charge) was too low compared to what we expect from theoretical prediction.

$$\frac{MIP_{2021BT}}{MIP_{2019BT}} = \frac{75}{118} \sim 0.63$$

The peaks are different
Original though : because of the difference of the supplied voltage

2019 Beam Test

- RCDAQ. FPHX parameters were operated via expert-GUI.
- I couldn't find the exact records of FPHX parameters for the 2019 beam test though, it is likely FPHXs were operated with default parameters.



Default Configuration

Telescope
- Position
  - x=1570mm
  - y=150mm
- Rotation
  - 0°
- Vertical Tilt
  - 0°

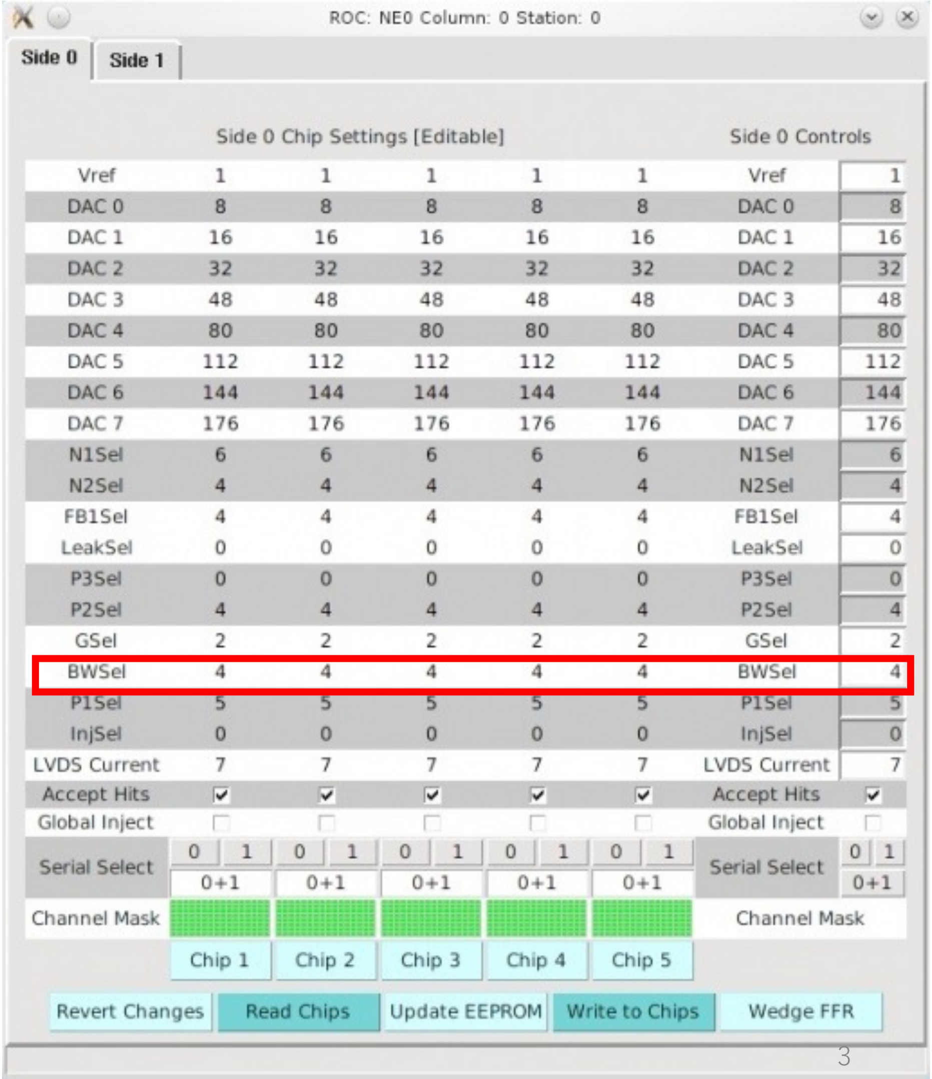
Beam
- 120 GeV primary proton
- ~10kHz
- σ_y~2mm, σ_y~6mm

DAC	Threshold Value
0	8
1	16
2	32
3	48
4	80
5	112
6	144
7	176

Snapshot from the RunPlan of Beam Test 2019

No specification in the gain setting. Unless we customize parameters via expert-GUI, FPHX just runs with default parameters (or loaded from a default setting file?)

Expert GUI Screenshot provided from Jin Huang
(Typical FVTX Operating Condition)

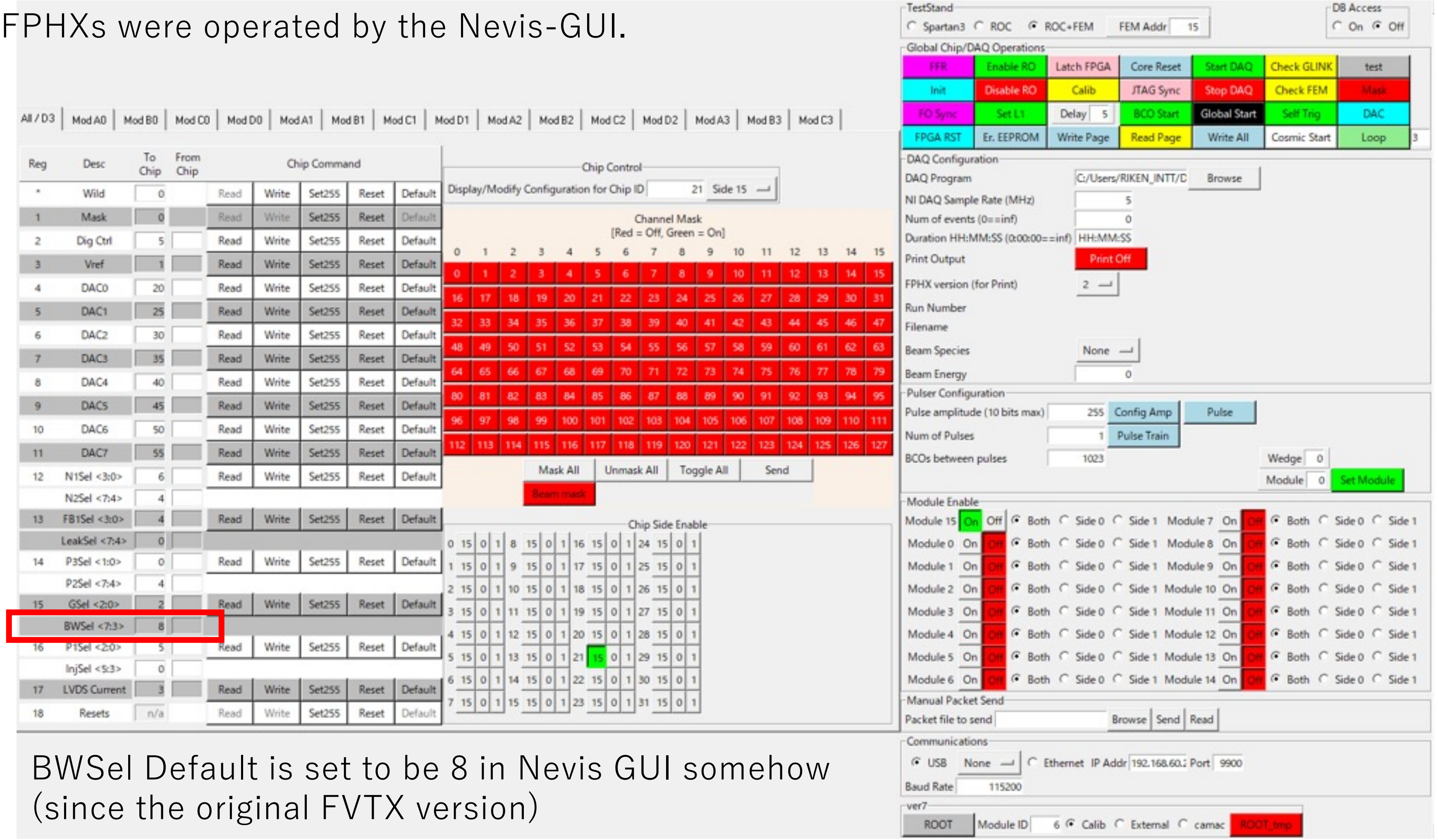


Side 0 Chip Settings [Editable] — Side 0 Controls

Vref	1	1	1	1	1	Vref	1
DAC 0	8	8	8	8	8	DAC 0	8
DAC 1	16	16	16	16	16	DAC 1	16
DAC 2	32	32	32	32	32	DAC 2	32
DAC 3	48	48	48	48	48	DAC 3	48
DAC 4	80	80	80	80	80	DAC 4	80
DAC 5	112	112	112	112	112	DAC 5	112
DAC 6	144	144	144	144	144	DAC 6	144
DAC 7	176	176	176	176	176	DAC 7	176
N1Sel	6	6	6	6	6	N1Sel	6
N2Sel	4	4	4	4	4	N2Sel	4
FB1Sel	4	4	4	4	4	FB1Sel	4
LeakSel	0	0	0	0	0	LeakSel	0
P3Sel	0	0	0	0	0	P3Sel	0
P2Sel	4	4	4	4	4	P2Sel	4
GSel	2	2	2	2	2	GSel	2
BWSel	4	4	4	4	4	BWSel	4
P1Sel	5	5	5	5	5	P1Sel	5
InjSel	0	0	0	0	0	InjSel	0
LVDS Current	7	7	7	7	7	LVDS Current	7
Accept Hits	☑	☑	☑	☑	☑	Accept Hits	☑
Global Inject	☐	☐	☐	☐	☐	Global Inject	☐
Serial Select	0 1 0+1	0 1 0+1	0 1 0+1	0 1 0+1	0 1 0+1	Serial Select	0 1 0+1
Channel Mask	🟩	🟩	🟩	🟩	🟩	Channel Mask	
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5		

2021 Beam Test

- FPHXs were operated by the Nevis-GUI.



Reg	Desc	To Chip	From Chip	Chip Command				
*	Wild	0		Read	Write	Set255	Reset	Default
1	Mask	0		Read	Write	Set255	Reset	Default
2	Dig Ctrl	5		Read	Write	Set255	Reset	Default
3	Vref	1		Read	Write	Set255	Reset	Default
4	DAC0	20		Read	Write	Set255	Reset	Default
5	DAC1	25		Read	Write	Set255	Reset	Default
6	DAC2	30		Read	Write	Set255	Reset	Default
7	DAC3	35		Read	Write	Set255	Reset	Default
8	DAC4	40		Read	Write	Set255	Reset	Default
9	DAC5	45		Read	Write	Set255	Reset	Default
10	DAC6	50		Read	Write	Set255	Reset	Default
11	DAC7	55		Read	Write	Set255	Reset	Default
12	N1Sel <3:0>	6		Read	Write	Set255	Reset	Default
	N2Sel <7:4>	4						
13	FB1Sel <3:0>	4		Read	Write	Set255	Reset	Default
	LeakSel <7:4>	0						
14	P3Sel <1:0>	0		Read	Write	Set255	Reset	Default
	P2Sel <7:4>	4						
15	GSel <2:0>	2		Read	Write	Set255	Reset	Default
	BWSel <7:3>	8						
16	P1Sel <2:0>	5		Read	Write	Set255	Reset	Default
	InjSel <5:3>	0						
17	LVDS Current	3		Read	Write	Set255	Reset	Default
18	Resets	n/a		Read	Write	Set255	Reset	Default

Chip Control

Display/Modify Configuration for Chip ID 21 Side 15

Channel Mask
[Red = Off, Green = On]

TestStand ○ Spartan3 ○ ROC ● ROC+FEM FEM Addr 15

DB Access ○ On ● Off

Global Chip/DAQ Operations

DAQ Configuration

DAQ Program C:/Users/RIKEN_INTT/D Browse

NI DAQ Sample Rate (MHz) 5

Num of events (0==inf) 0

Duration HH:MM:SS (0:00:00==inf) HH:MM:SS

Print Output Print Off

FPHX version (for Print) 2

Run Number

Filename

Beam Species None

Beam Energy 0

Pulser Configuration

Pulse amplitude (10 bits max) 255 Config Amp Pulse

Num of Pulses 1 Pulse Train

BCOs between pulses 1023

Wedge 0

Module 0 Set Module

Module Enable

Module 15	On	Off	● Both	○ Side 0	○ Side 1	Module 7	On	Off	● Both	○ Side 0	○ Side 1
Module 0	On	Off	● Both	○ Side 0	○ Side 1	Module 8	On	Off	● Both	○ Side 0	○ Side 1
Module 1	On	Off	● Both	○ Side 0	○ Side 1	Module 9	On	Off	● Both	○ Side 0	○ Side 1
Module 2	On	Off	● Both	○ Side 0	○ Side 1	Module 10	On	Off	● Both	○ Side 0	○ Side 1
Module 3	On	Off	● Both	○ Side 0	○ Side 1	Module 11	On	Off	● Both	○ Side 0	○ Side 1
Module 4	On	Off	● Both	○ Side 0	○ Side 1	Module 12	On	Off	● Both	○ Side 0	○ Side 1
Module 5	On	Off	● Both	○ Side 0	○ Side 1	Module 13	On	Off	● Both	○ Side 0	○ Side 1
Module 6	On	Off	● Both	○ Side 0	○ Side 1	Module 14	On	Off	● Both	○ Side 0	○ Side 1

Manual Packet Send

Packet file to send Browse Send Read

Communications

● USB None ○ Ethernet IP Addr 192.168.60.: Port 9900

Baud Rate 115200

ver7

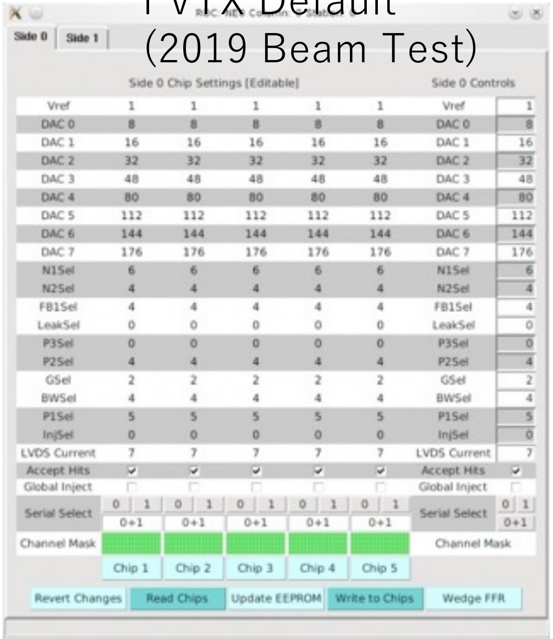
ROOT Module ID 6 ● Calib ○ External ○ camac ROOT_imp

BWSel Default is set to be 8 in Nevis GUI somehow (since the original FVTX version)

FPHX Parameters

Name	Description	Default	2019 Beam Test (FVTX)	2021 Beam Test
Vref		1	1	1
DAC0		8	8	15
DAC1		16	16	30
DAC2		32	32	60
DAC3		48	48	90
DAC4		80	80	120
DAC5		112	112	150
DAC6		144	144	180
DAC7		176	176	210
N1Sel		6	6	6
N2Sel		4	4	4
FB1Sel		4	4	4
LeakSel		0	0	0
P3Sel		0	0	0
P2Sel		4	4	4
GSel	Gain Select	2	2	2
BWSel	**Bandwidth Select**	**4**	**4**	**8**
P1Sel		5	5	5
InjSel		0	0	0
LVDS Current [mA]		1	3	2

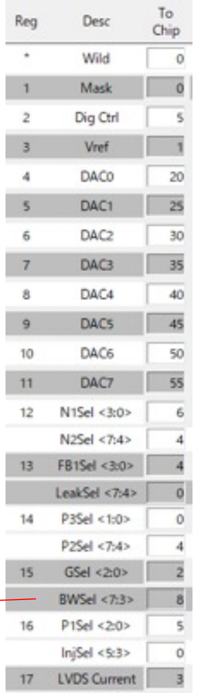
FVTX Default
(2019 Beam Test)



Side 0 | Side 1

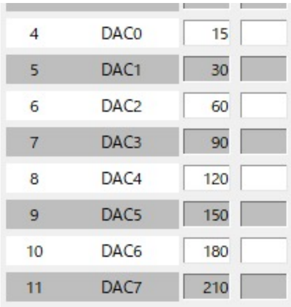
Side 0 Chip Settings [Editable] | Side 0 Controls

Vref	1	1	1	1	1	Vref	1
DAC 0	8	8	8	8	8	DAC 0	8
DAC 1	16	16	16	16	16	DAC 1	16
DAC 2	32	32	32	32	32	DAC 2	32
DAC 3	48	48	48	48	48	DAC 3	48
DAC 4	80	80	80	80	80	DAC 4	80
DAC 5	112	112	112	112	112	DAC 5	112
DAC 6	144	144	144	144	144	DAC 6	144
DAC 7	176	176	176	176	176	DAC 7	176
N1Sel	6	6	6	6	6	N1Sel	6
N2Sel	4	4	4	4	4	N2Sel	4
FB1Sel	4	4	4	4	4	FB1Sel	4
LeakSel	0	0	0	0	0	LeakSel	0
P3Sel	0	0	0	0	0	P3Sel	0
P2Sel	4	4	4	4	4	P2Sel	4
GSel	2	2	2	2	2	GSel	2
BWSel	4	4	4	4	4	BWSel	4
P1Sel	5	5	5	5	5	P1Sel	5
InjSel	0	0	0	0	0	InjSel	0
LVDS Current	7	7	7	7	7	LVDS Current	7
Accept Hits	☑	☑	☑	☑	☑	Accept Hits	☑
Global Inject	□	□	□	□	□	Global Inject	□
Serial Select	0 1 0+1	0 1 0+1	0 1 0+1	0 1 0+1	0 1 0+1	Serial Select	0 1 0+1
Channel Mask	🟩	🟩	🟩	🟩	🟩	Channel Mask	
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5		



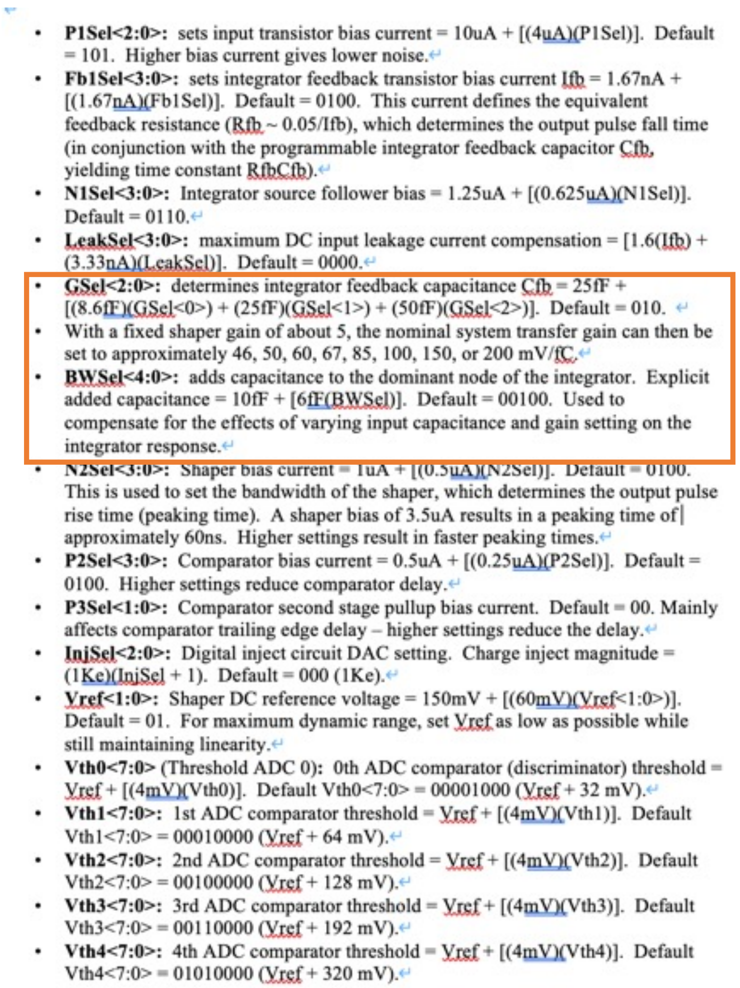
Reg	Desc	To Chip
*	Wild	0
1	Mask	0
2	Dig Ctrl	5
3	Vref	1
4	DAC0	20
5	DAC1	25
6	DAC2	30
7	DAC3	35
8	DAC4	40
9	DAC5	45
10	DAC6	50
11	DAC7	55
12	N1Sel <3:0>	6
	N2Sel <7:4>	4
13	FB1Sel <3:0>	4
	LeakSel <7:4>	0
14	P3Sel <1:0>	0
	P2Sel <7:4>	4
15	GSel <2:0>	2
	BWSel <7:3>	8
16	P1Sel <2:0>	5
	InjSel <5:3>	0
17	LVDS Current	3

Nevis GUI defaults
(Even from 2013)



4	DAC0	15	
5	DAC1	30	
6	DAC2	60	
7	DAC3	90	
8	DAC4	120	
9	DAC5	150	
10	DAC6	180	
11	DAC7	210	

FPHX Gain Parameters



- **P1Sel<2:0>:** sets input transistor bias current = 10uA + [(4uA)(P1Sel)]. Default = 101. Higher bias current gives lower noise.
- **Fb1Sel<3:0>:** sets integrator feedback transistor bias current Ifb = 1.67nA + [(1.67nA)(Fb1Sel)]. Default = 0100. This current defines the equivalent feedback resistance (Rfb ~ 0.05/Ifb), which determines the output pulse fall time (in conjunction with the programmable integrator feedback capacitor Cfb, yielding time constant RfbCfb).
- **N1Sel<3:0>:** Integrator source follower bias = 1.25uA + [(0.625uA)(N1Sel)]. Default = 0110.
- **LeakSel<3:0>:** maximum DC input leakage current compensation = [1.6(Ifb) + (3.33nA)(LeakSel)]. Default = 0000.
- **GSel<2:0>:** determines integrator feedback capacitance Cfb = 25fF + [(8.6fF)(GSel<0>) + (25fF)(GSel<1>) + (50fF)(GSel<2>)]. Default = 010.
- With a fixed shaper gain of about 5, the nominal system transfer gain can then be set to approximately 46, 50, 60, 67, 85, 100, 150, or 200 mV/fC.
- **BWSel<4:0>:** adds capacitance to the dominant node of the integrator. Explicit added capacitance = 10fF + [6fF(BWSel)]. Default = 00100. Used to compensate for the effects of varying input capacitance and gain setting on the integrator response.
- **N2Sel<3:0>:** Shaper bias current = 1uA + [(0.5uA)(N2Sel)]. Default = 0100. This is used to set the bandwidth of the shaper, which determines the output pulse rise time (peaking time). A shaper bias of 3.5uA results in a peaking time of approximately 60ns. Higher settings result in faster peaking times.
- **P2Sel<3:0>:** Comparator bias current = 0.5uA + [(0.25uA)(P2Sel)]. Default = 0100. Higher settings reduce comparator delay.
- **P3Sel<1:0>:** Comparator second stage pullup bias current. Default = 00. Mainly affects comparator trailing edge delay – higher settings reduce the delay.
- **InjSel<2:0>:** Digital inject circuit DAC setting. Charge inject magnitude = (1Ke)(InjSel + 1). Default = 000 (1Ke).
- **Vref<1:0>:** Shaper DC reference voltage = 150mV + [(60mV)(Vref<1:0>)]. Default = 01. For maximum dynamic range, set Vref as low as possible while still maintaining linearity.
- **Vth0<7:0>** (Threshold ADC 0)**:** 0th ADC comparator (discriminator) threshold = Vref + [(4mV)(Vth0)]. Default Vth0<7:0> = 00001000 (Vref + 32 mV).
- **Vth1<7:0>:** 1st ADC comparator threshold = Vref + [(4mV)(Vth1)]. Default Vth1<7:0> = 00010000 (Vref + 64 mV).
- **Vth2<7:0>:** 2nd ADC comparator threshold = Vref + [(4mV)(Vth2)]. Default Vth2<7:0> = 00100000 (Vref + 128 mV).
- **Vth3<7:0>:** 3rd ADC comparator threshold = Vref + [(4mV)(Vth3)]. Default Vth3<7:0> = 00110000 (Vref + 192 mV).
- **Vth4<7:0>:** 4th ADC comparator threshold = Vref + [(4mV)(Vth4)]. Default Vth4<7:0> = 01010000 (Vref + 320 mV).

FPHX manual

- GSel<2:0> Def=010

$$C_{fb}[fF] = 25 + 8.6 \cdot GSel\langle 0\rangle + 25 \cdot GSel\langle 1\rangle + 50 \cdot GSel\langle 2\rangle$$

- BWSel<4:0> Def=00100

$$C_{add}[fF] = 10 + 6 \cdot BWSel$$

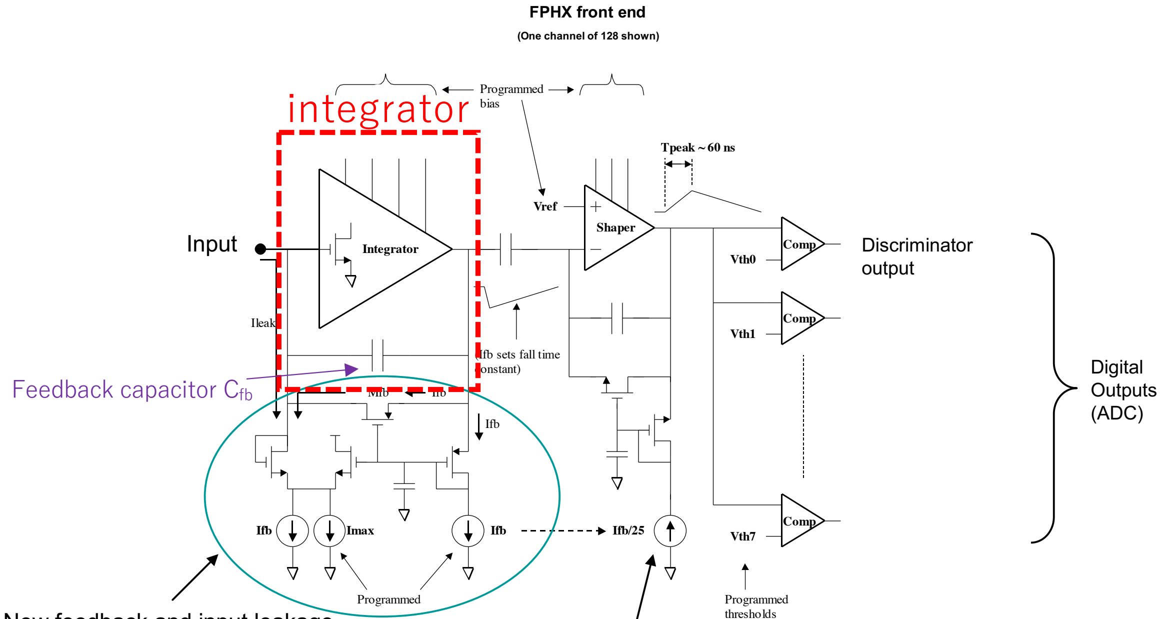
Total Capacitance

$$C_{Total} = C_{fb} + C_{add}$$?

FPHX Integrator Schematic

- A new type of continuous reset and leakage compensation circuit has been designed for the integrator. In Figure 6, a programmable current labeled Ifb sets the effective reset resistance. Mfb acts exactly like a resistor of value 1/gm for small signals, where gm depends directly on Ifb since Mfb is in weak inversion. This programmed resistance, in conjunction with the feedback capacitor, sets the RC fall time (return to baseline) of the shaped signal. For large signals, when the output swings more than a hundred mV or so, Mfb no longer looks like a resistor, but a constant current source. The return to baseline then becomes linear until the output approaches the reset level, at which point it becomes an exponential RC decay again.

Simplified conceptual diagram of one channel



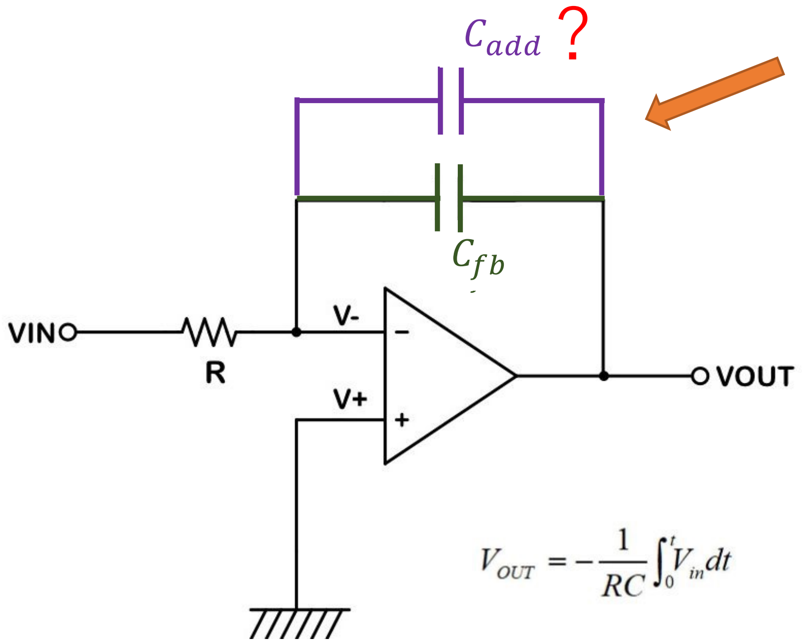
New feedback and input leakage current compensation circuit

Shaper Rfb >> Integrator Rfb so that the shaper output pulse fall time is determined by the integrator only

Figure 6.

FPHX Integrator Schematic

- The integrator is shown in detail in Figure 7. The input transistor feeds a regulated cascode (to keep the open loop gain high), and is biased by a cascode current source. Additional input transistor bias current is programmed through switched current sources. The integrator bandwidth is adjustable via switched capacitors on the amplifier dominant node. The transfer gain is set with programmable feedback capacitors. A source follower drives the integrator output.



$$V_{OUT} = -\frac{1}{RC}\int_0^t V_{in}\,dt$$

Integrator schematic

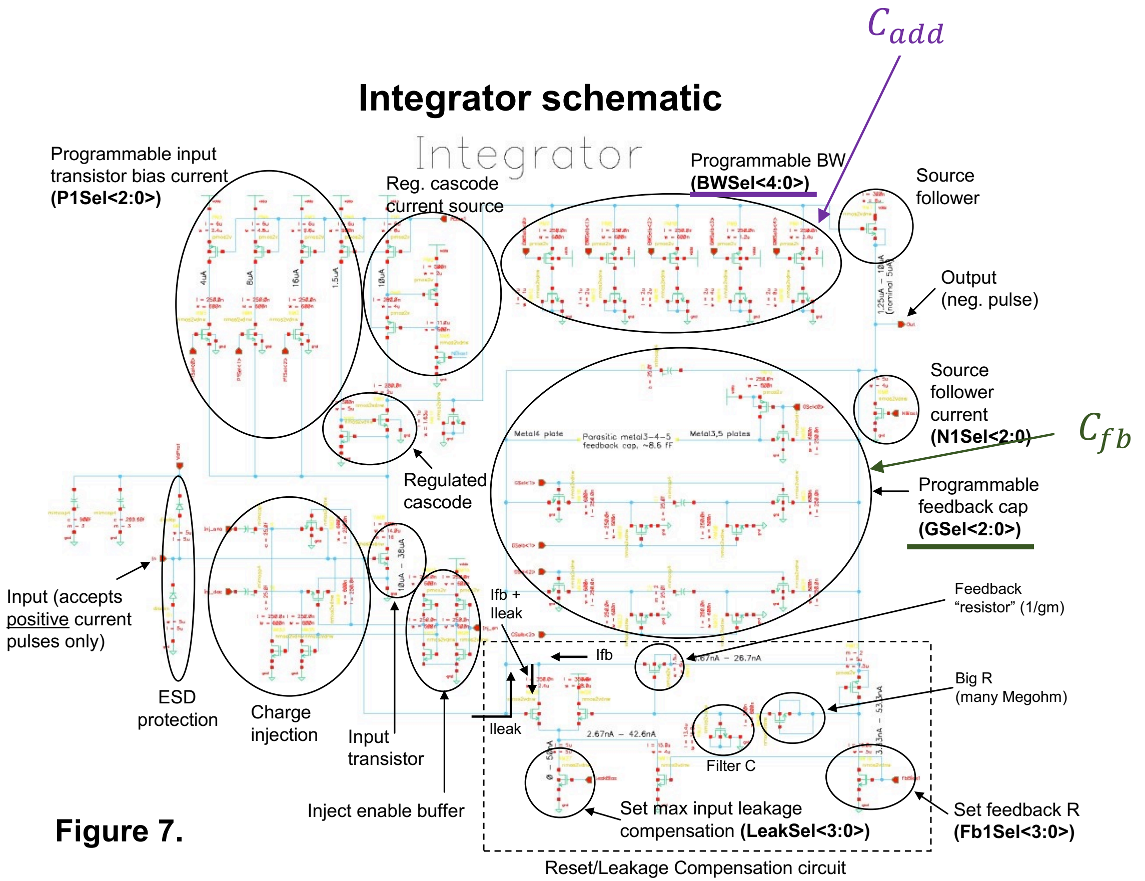

C_{add}
Integrator
Programmable input transistor bias current (P1Sel<2:0>)
Reg. cascode current source
Programmable BW (BWSel<4:0>)
Source follower
Output (neg. pulse)
Source follower current (N1Sel<2:0>)
C_{fb}
Regulated cascode
Programmable feedback cap (GSel<2:0>)
Feedback "resistor" (1/gm)
Input (accepts positive current pulses only)
Ifb + Ileak
Ifb
Big R (many Megohm)
ESD protection
Charge injection
Input transistor
Ileak
Filter C
Inject enable buffer
Set max input leakage compensation (LeakSel<3:0>)
Set feedback R (Fb1Sel<3:0>)
Reset/Leakage Compensation circuit

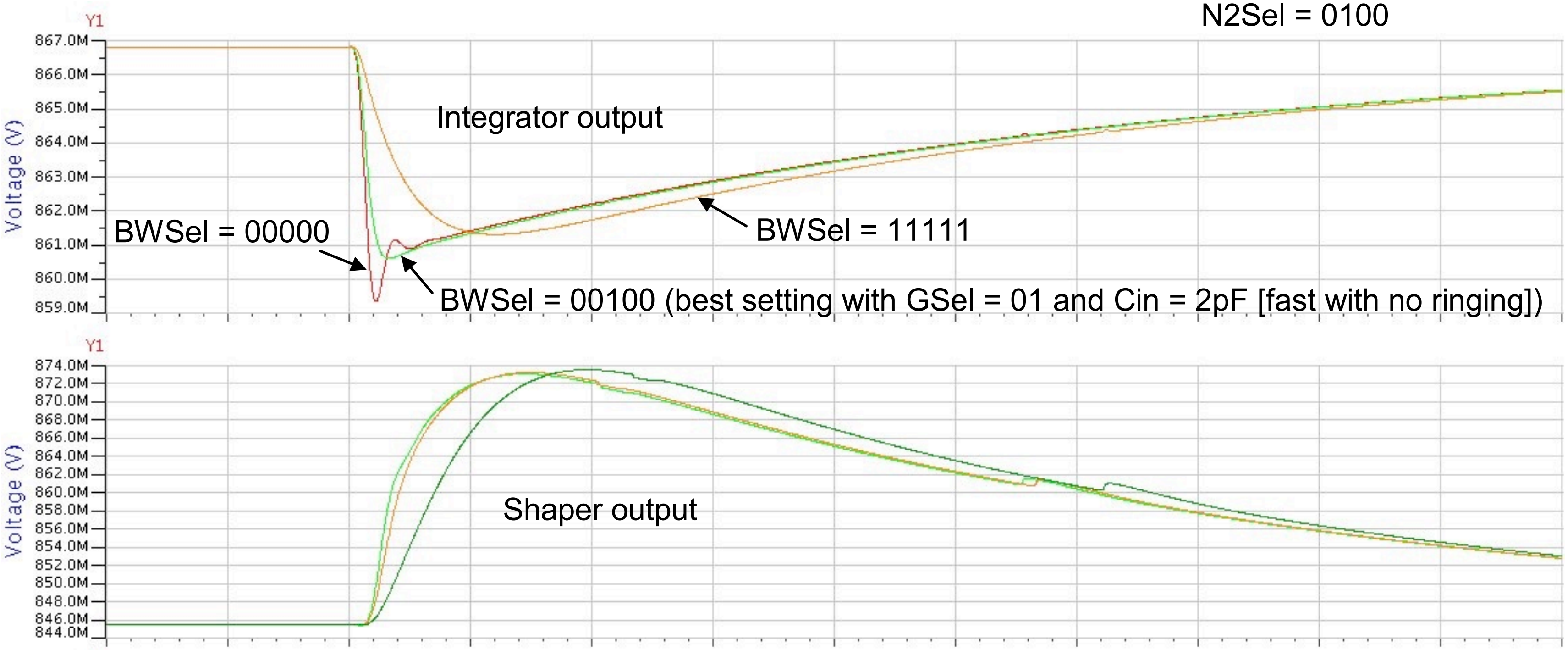
Figure 7.

FPHX manual

Effect of BWSel Parameter

Effect of BWSel parameter on integrator response

Qin = 2000e
Cin = 2pF (total)
GSel = 010
Fb1Sel = 0100
N2Sel = 0100



Integrator output

BWSel = 00000

BWSel = 11111

BWSel = 00100 (best setting with GSel = 01 and Cin = 2pF [fast with no ringing])

Shaper output

FPHX Gain Calculation

- GSel<2:0> Def=010

$$C_{fb}[fF] = 25 + 8.6 \cdot GSel\langle 0\rangle + 25 \cdot GSel\langle 1\rangle + 50 \cdot GSel\langle 2\rangle$$

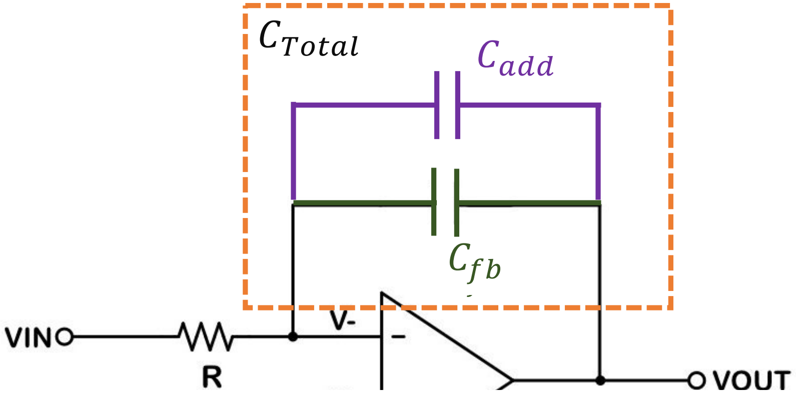
- BWSel<4:0> Def=00100

$$C_{add}[fF] = 10 + 6 \cdot BWSel$$

Total Capacitance

$$C_{Total} = C_{fb} + C_{add}$$

Assuming following circuit is correct



Beam Test	2019	2021
GSel	2 <010>	2 <010>
BWSel	4 <00100>	8 <01000>
C_{fb}[fF]	25+25=50	25+25=50
C_{add} [fF]	10+6•4=34	10+6•8=58
C_{total} [fF]	84	108
V_{out} [a.u.]	1	**0.78**

$$V_{OUT} = -\frac{1}{RC}\int_0^t V_{in}\,dt$$

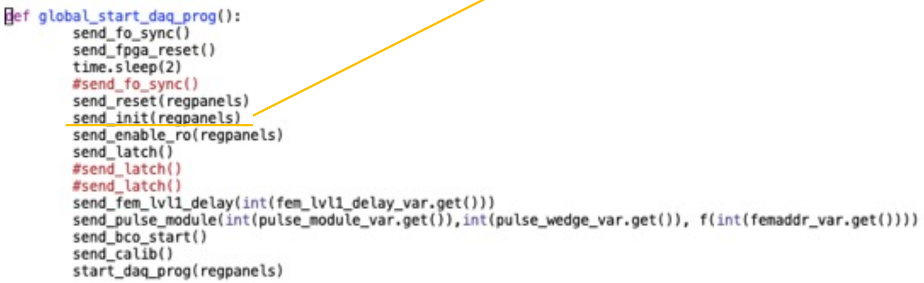
↕ Still not sufficient

Observation

$$\frac{MIP_{2021BT}}{MIP_{2019BT}} = \frac{75}{118} \sim 0.63$$

Global Start

Initialization Sequence

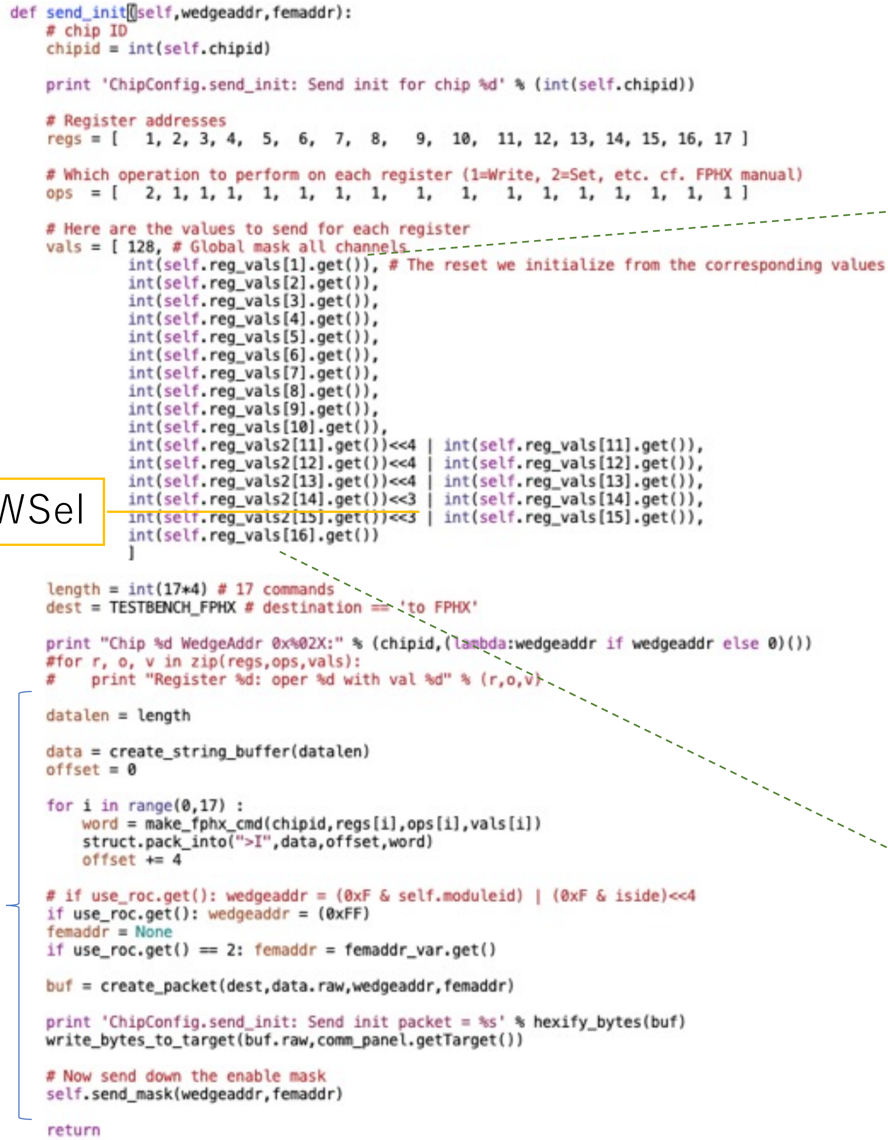


```
def global_start_daq_prog():
        send_fo_sync()
        send_fpga_reset()
        time.sleep(2)
        #send_fo_sync()
        send_reset(regpanels)
        send_init(regpanels)
        send_enable_ro(regpanels)
        send_latch()
        #send_latch()
        #send_latch()
        send_fem_lvl1_delay(int(fem_lvl1_delay_var.get()))
        send_pulse_module(int(pulse_module_var.get()),int(pulse_wedge_var.get()), f(int(femaddr_var.get())))
        send_bco_start()
        send_calib()
        start_daq_prog(regpanels)
```

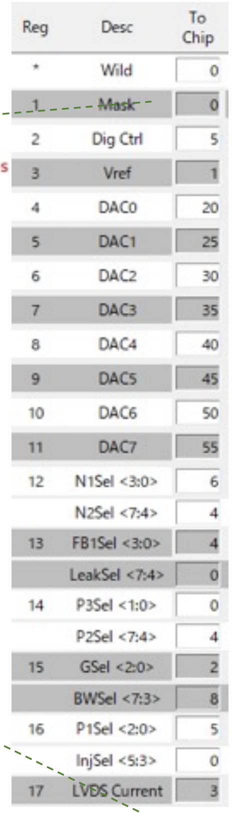
Are the parameters automatically loaded to FPHX at the beginning of run?

Sending parameters routine?

BWSel



```
def send_init(self,wedgeaddr,femaddr):
    # chip ID
    chipid = int(self.chipid)

    print 'ChipConfig.send_init: Send init for chip %d' % (int(self.chipid))

    # Register addresses
    regs = [   1, 2, 3, 4,  5,  6,  7,  8,   9,  10,  11, 12, 13, 14, 15, 16, 17 ]

    # Which operation to perform on each register (1=Write, 2=Set, etc. cf. FPHX manual)
    ops  = [   2, 1, 1, 1,  1,  1,  1,  1,   1,   1,   1,  1,  1,  1,  1,  1,  1 ]

    # Here are the values to send for each register
    vals = [ 128, # Global mask all channels
             int(self.reg_vals[1].get()), # The reset we initialize from the corresponding values
             int(self.reg_vals[2].get()),
             int(self.reg_vals[3].get()),
             int(self.reg_vals[4].get()),
             int(self.reg_vals[5].get()),
             int(self.reg_vals[6].get()),
             int(self.reg_vals[7].get()),
             int(self.reg_vals[8].get()),
             int(self.reg_vals[9].get()),
             int(self.reg_vals[10].get()),
             int(self.reg_vals2[11].get())<<4 | int(self.reg_vals[11].get()),
             int(self.reg_vals2[12].get())<<4 | int(self.reg_vals[12].get()),
             int(self.reg_vals2[13].get())<<4 | int(self.reg_vals[13].get()),
             int(self.reg_vals2[14].get())<<3 | int(self.reg_vals[14].get()),
             int(self.reg_vals2[15].get())<<3 | int(self.reg_vals[15].get()),
             int(self.reg_vals[16].get())
             ]

    length = int(17*4) # 17 commands
    dest = TESTBENCH_FPHX # destination == 'to FPHX'

    print "Chip %d WedgeAddr 0x%02X:" % (chipid,(lambda:wedgeaddr if wedgeaddr else 0)())
    #for r, o, v in zip(regs,ops,vals):
    #    print "Register %d: oper %d with val %d" % (r,o,v)

    datalen = length

    data = create_string_buffer(datalen)
    offset = 0

    for i in range(0,17) :
        word = make_fphx_cmd(chipid,regs[i],ops[i],vals[i])
        struct.pack_into(">I",data,offset,word)
        offset += 4

    # if use_roc.get(): wedgeaddr = (0xF & self.moduleid) | (0xF & iside)<<4
    if use_roc.get(): wedgeaddr = (0xFF)
    femaddr = None
    if use_roc.get() == 2: femaddr = femaddr_var.get()

    buf = create_packet(dest,data.raw,wedgeaddr,femaddr)

    print 'ChipConfig.send_init: Send init packet = %s' % hexify_bytes(buf)
    write_bytes_to_target(buf.raw,comm_panel.getTarget())

    # Now send down the enable mask
    self.send_mask(wedgeaddr,femaddr)

    return
```



Reg	Desc	To Chip
*	Wild	0
1	Mask	0
2	Dig Ctrl	5
3	Vref	1
4	DAC0	20
5	DAC1	25
6	DAC2	30
7	DAC3	35
8	DAC4	40
9	DAC5	45
10	DAC6	50
11	DAC7	55
12	N1Sel <3:0>	6
	N2Sel <7:4>	4
13	FB1Sel <3:0>	4
	LeakSel <7:4>	0
14	P3Sel <1:0>	0
	P2Sel <7:4>	4
15	GSel <2:0>	2
	BWSel <7:3>	8
16	P1Sel <2:0>	5
	InjSel <5:3>	0
17	LVDS Current	3

To be confirmed

- FPHX operation conditions for 2019 and 2021 beam tests.
    - Does default parameters in Nevis-GUI really loaded to FPHX automatically in the initialization routine of the global start?
- Integrator circuit. If $C_{Total} = C_{fb} + C_{add}$ is correct.
- Actual measurement and comparison of MIP position BWSel=4 vs BWSel=8 is mandatory to observe the actual response.

Programming Strategy

- First determine **GSel** based on the desired approximate transfer gain (approx. 50 – 200 mV/fC).
- Then depending on the value of the input capacitance (Cin), program **BWSel** to achieve fast integrator response without ringing.
- For Cin = 2 pF (1.5 pF detector + 0.5 pF parasitic):
  - If **GSel** = 000, set **BWSel** = 00000
  - If **GSel** = 010, set **BWSel** = 00100
  - If **GSel** = 100, set **BWSel** = 01000
  - If **GSel** = 110, set **BWSel** = 01100

Physics	Dec	Bin
GSel	2	010
BWSel	4	1000

Relevant setting for INTT

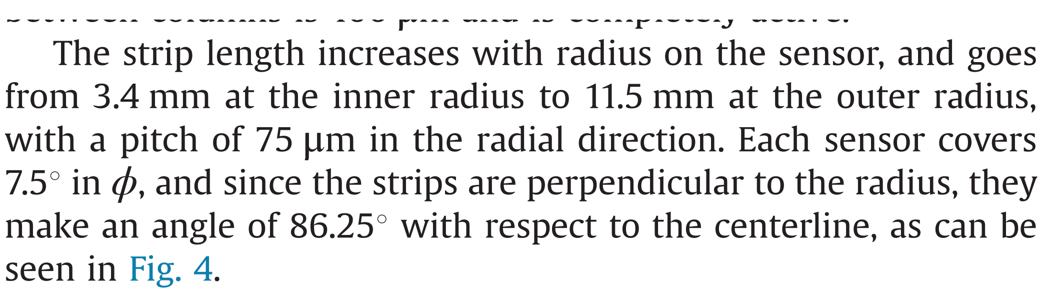
- For Cin = 1.5 pF (1 pF detector + 0.5 pF parasitic):
  - If **GSel** = 000, set **BWSel** = 00001
  - If **GSel** = 010, set **BWSel** = 00110
  - If **GSel** = 100, set **BWSel** = 01010
  - If **GSel** = 110, set **BWSel** = 01110
- For Cin = 1 pF (0.5 pF detector + 0.5 pF parasitic):
  - If **GSel** = 000, set **BWSel** = 00010
  - If **GSel** = 010, set **BWSel** = 01000
  - If **GSel** = 100, set **BWSel** = 01110
  - If **GSel** = 110, set **BWSel** = 10101

Nevis	Dec	Bin
GSel	2	010
BWSel	8	1000

- Program **Fb1Sel** based on the desired fall time constant
- Then program **N2Sel** to achieve the desired rise time/peaking time (rise and fall times will have some effect on the transfer gain)
- Program **Vref** to the lowest value possible that allows linear response (nominally 00)
- Based on the transfer gain, set the desired comparator thresholds

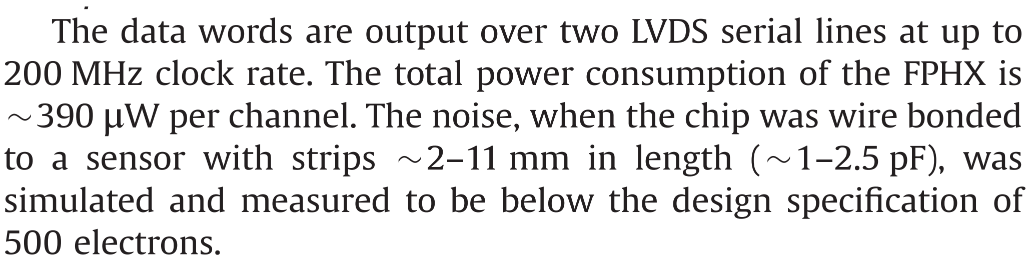
From FPHX Operation Manual

FVTX NIM



between columns is 100 μm and is completely active.

The strip length increases with radius on the sensor, and goes from 3.4 mm at the inner radius to 11.5 mm at the outer radius, with a pitch of 75 μm in the radial direction. Each sensor covers 7.5° in ϕ, and since the strips are perpendicular to the radius, they make an angle of 86.25° with respect to the centerline, as can be seen in Fig. 4.



The data words are output over two LVDS serial lines at up to 200 MHz clock rate. The total power consumption of the FPHX is ∼390 μW per channel. The noise, when the chip was wire bonded to a sensor with strips ∼2–11 mm in length (∼1–2.5 pF), was simulated and measured to be below the design specification of 500 electrons.

INTT Type-A ~ 2.5pF (78um, 12mm)
Type-B ~ 3pF or so?