MPGD digitazation model for bkg studies – GD/I WG 2/13/23

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- Many unknowns:
  - Detector configuration, still to be finalized
  - FEE ASIC, development just started, specs not yet finalized
  - Readout pattern: strips for 2D readout, pitch to be defined
- Detector geometry:
  - Barrel layer: cylindrical tiles 50x70cm^2
- Readout model foreseen:
  - Orthogonal strips for 2D measurement.
- Current implementation in simulation:
  - Orthogonal smearing with ~150µm on both direction
  - Plans to update the geometry soon

Channels	Integration time	Threshold	Intrinsic noise
30k--50k	50ns – 1µs	~0.25keV	0

- ASIC with programmable integration time
- MIP in a 3mm gap, ~30 electrons
- gain ~10k
- S/N ~20
- Threshold = 5*N