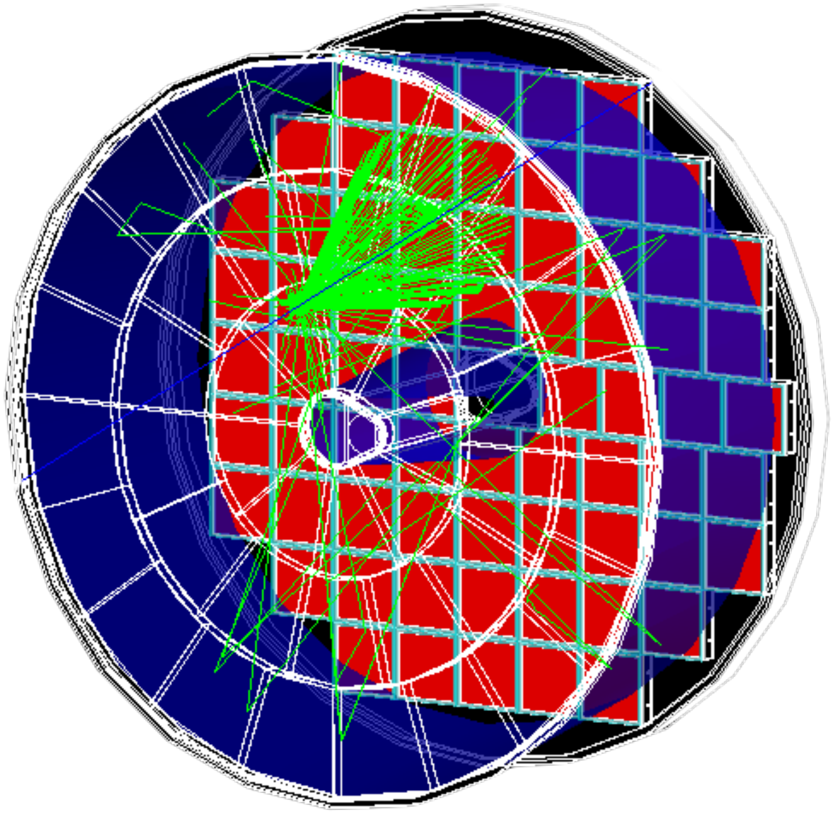
Sensors and Front End Electronics



ePIC pfRICH:

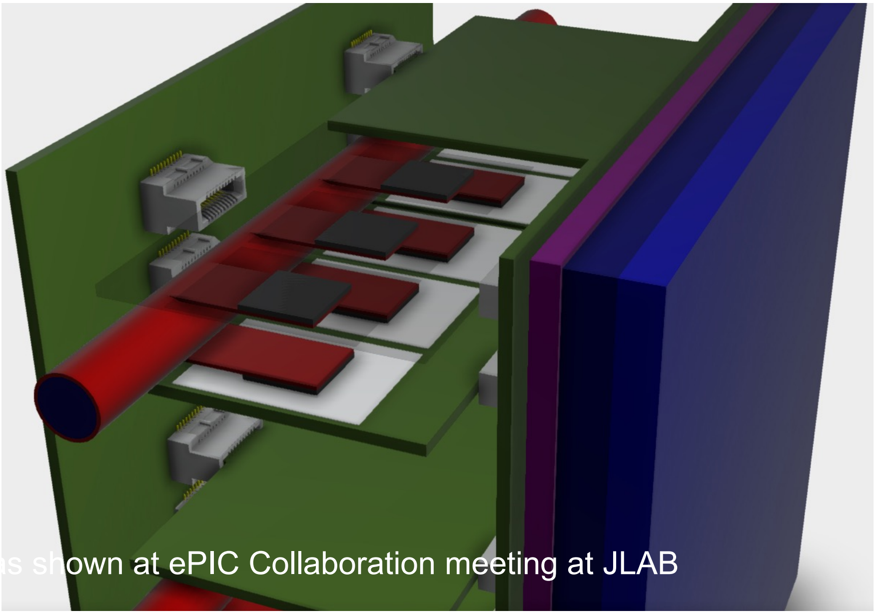
- ❑ Photosensor: DC-coupled HRPPD
- ❑ ASIC: EICROC in a 256-channel version
- ❑ Integrated sensor concept

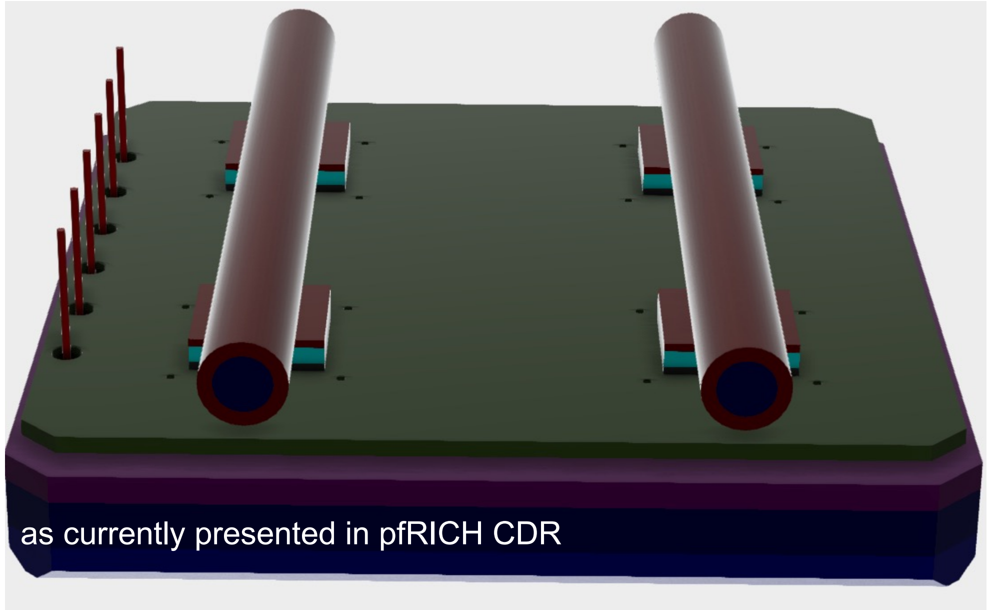
Alexander Kiselev (BNL)

Charge Topics addressed in this Talk

5. **Sensors and FEE**:
    1. Status of **photosensor selection** (a single consolidated option, more options under consideration); please provide photo sensor and pixel segmentation characteristics?
    2. **Status of the sensor** development and related potential issues?
    3. **Perspectives of sensor mass production** and timelines for the production period?
    4. **Characteristics of the ASIC and FEEs** considered?
    5. Status of **FEE identification** (a single consolidated option, more options under consideration)? Present a plan for realization on the FEE development in the context of technology choice and in conjunction with the project.
    6. Status of the **FEE development** and related potential issues?
    7. Perspectives of **FEE mass production** and timelines for the production period?

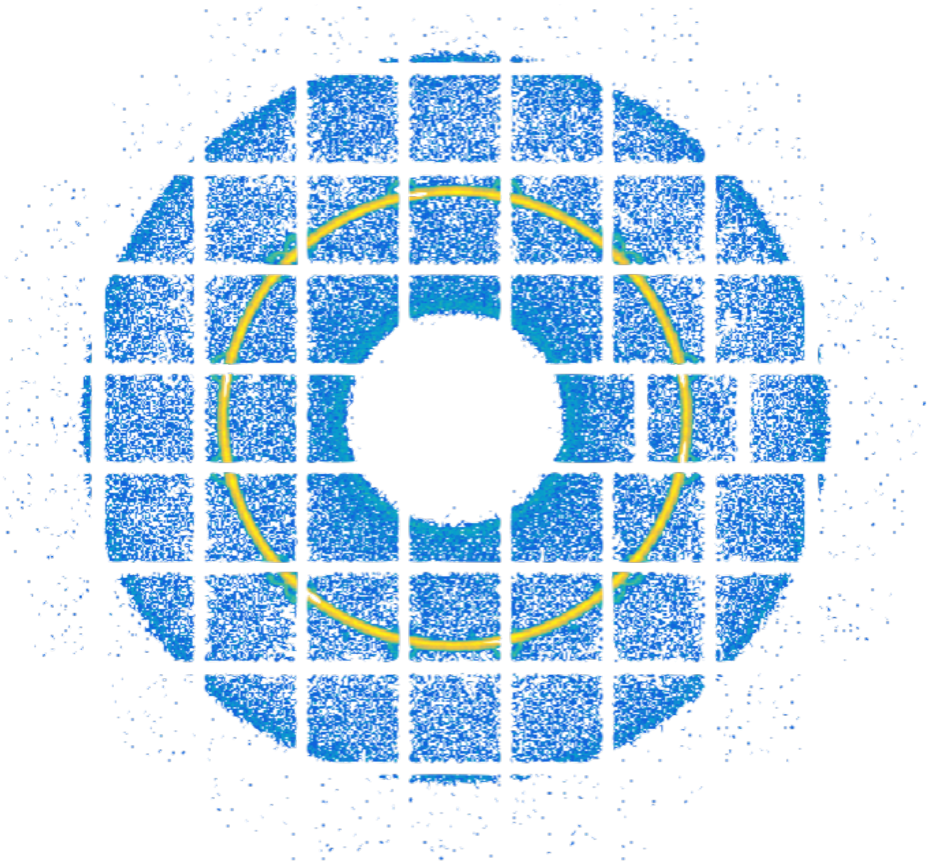
Conceptual evolution since January 2023





- Capacitively coupled HRPPDs
- 24x24 pad pixellation
- Waveform digitizer ASIC (Nalu)
- Vertical integration + a backplane

- DC-coupled HRPPDs
- 32x32 pad pixellation
- TOA / ADC ASIC (EICROC)
- Flat integration



Sensor: HRPPD

1. Status of photosensor selection

- **pfRICH choice: HRPPD by Incom Inc.**
  - High intrinsic SPE timing resolution: <50 ps
  - Low Dark Count Rate (compared to SiPMs): ~1 kHz/cm^2
  - Low cost (compared to other MCP-PMTs): <$20k for a 120mm x 120mm sensor

<u>Capacitively coupled (Gen II)</u>

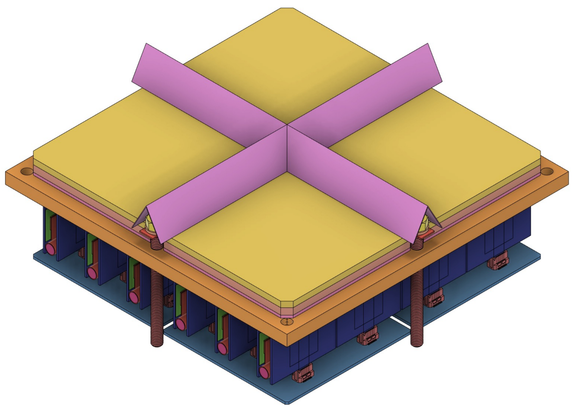
- Pros
  - All our experience is based on Gen II LAPPDs
  - Flexibility in the readout board design
- Cons
  - Broad clusters -> occupancy, overlaps, etc
  - Resistive layer -> additional R&D topic
  - Somewhat smaller amplitudes

<u>DC-coupled</u>

- Pros
  - Single pad hits -> better for timing
  - Same design for pfRICH & DIRC
- Cons
  - Missing interface to the readout board
  - Performance yet to be verified
  - Spatial resolution limited by pitch/$\sqrt{12}$

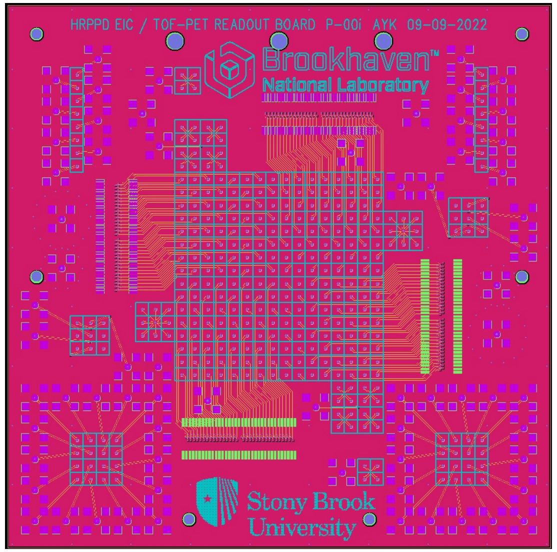
1. Status of photosensor selection

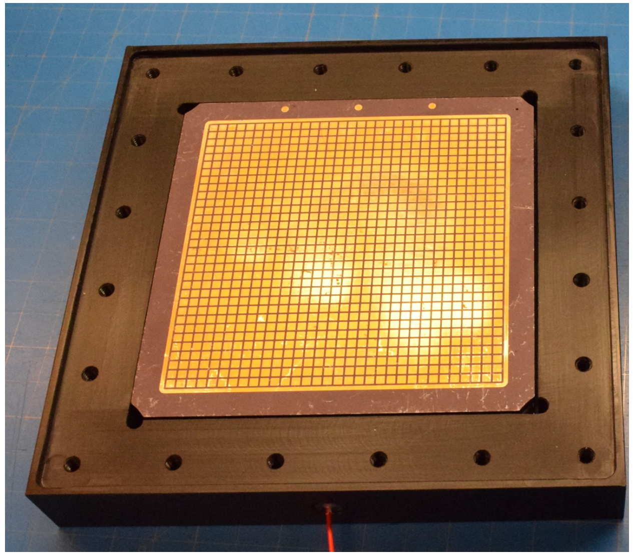
- **Alternative solutions**
  - Capacitively coupled HRPPDs is still an option
  - Other commercially available MCP-PMTs (like PHOTONIS Planacon)
    - One seemingly can over-tilt the outer conical mirror, give up η acceptance above -1.65, and reduce the sensor plane by a factor of 2-3
    - Occupancy stays the same (or becomes even better) since a 2” Planacon has 32x32 pixel segmentation
    - Interfacing without dead zones becomes an issue …
    - .. yet may want to consider funneling pyramid mirrors around dead zones
  - SiPMs
    - Noise is becoming an issue
    - Cooling system is certainly more involved
    - Less space left for the expansion volume

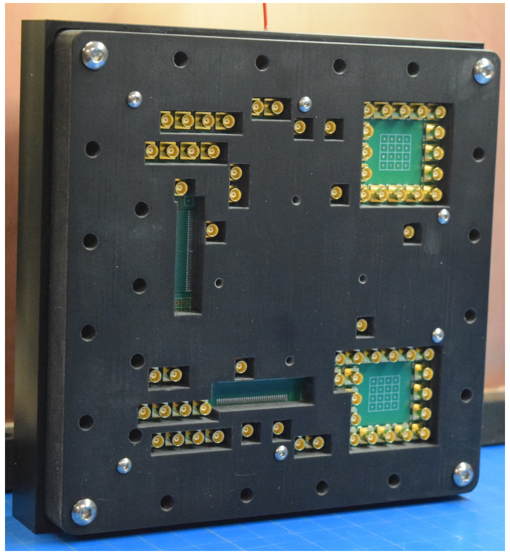


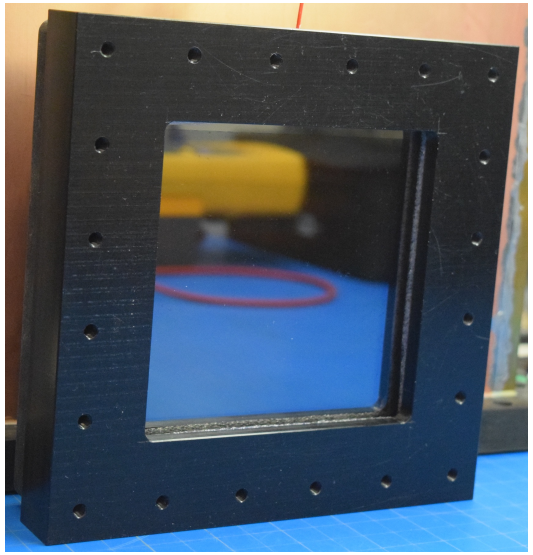
2. Status of photosensor development

- **We are developing HRPPDs with Incom as part of the eRD110 consortium activities**
  - HRPPD #6 will be sent to BNL this week, right after magnetic field resilience tests at Argonne
  - Pogo pin interface for these preliminary investigations was built from scratch since August 2022



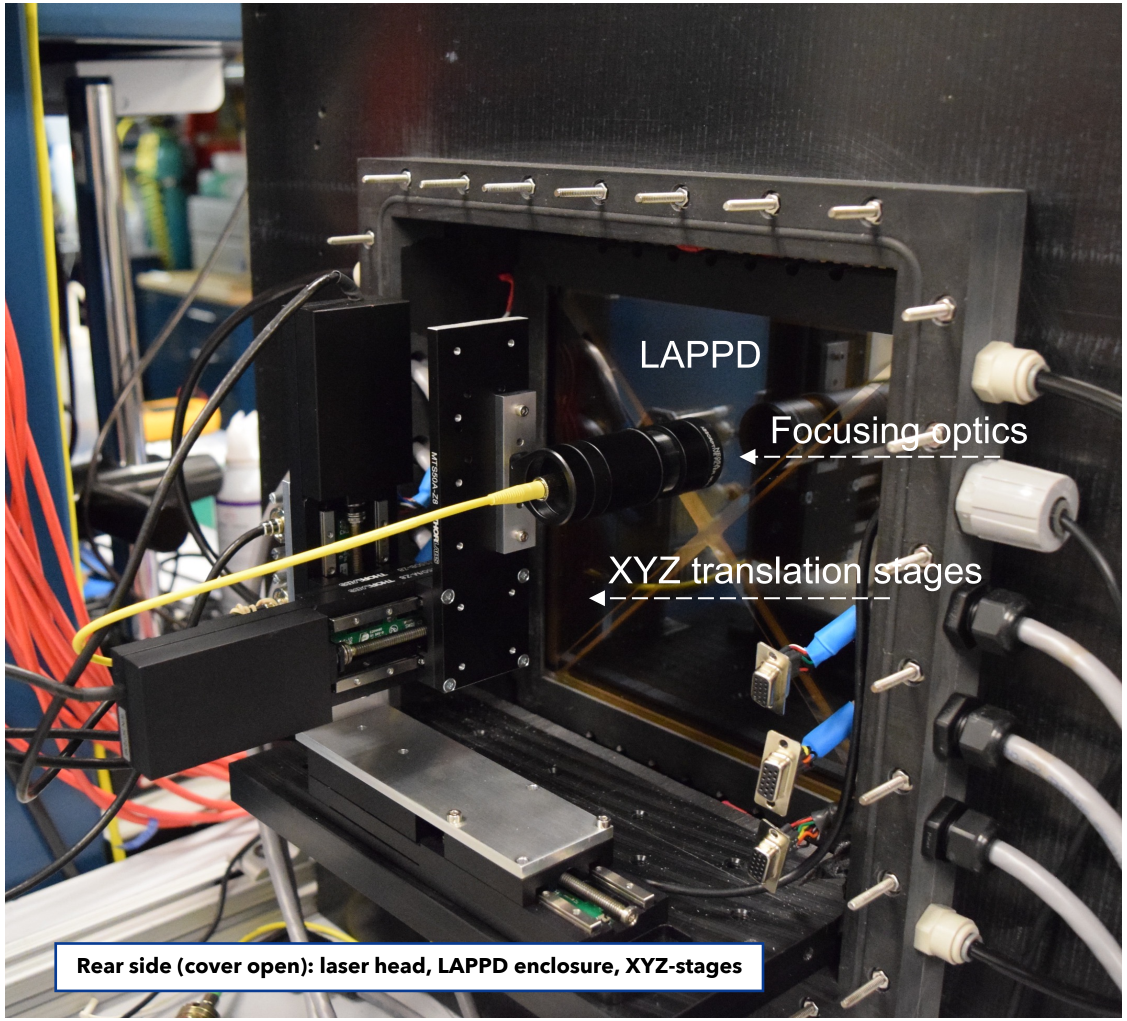






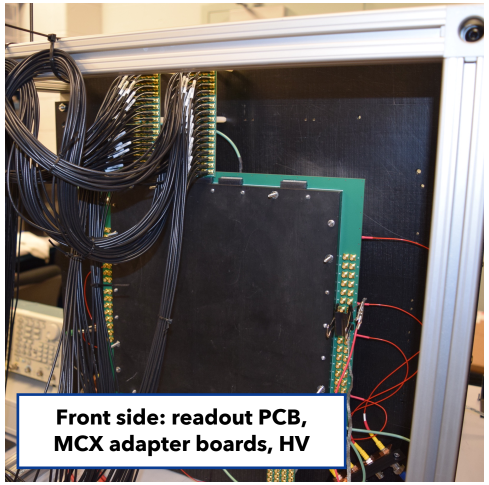
  - Specifications for the EIC-Incom PED contract are being finalized
  - First five tiles to be produced by Incom after the final round of design modifications in 2023

Test bench setup at BNL

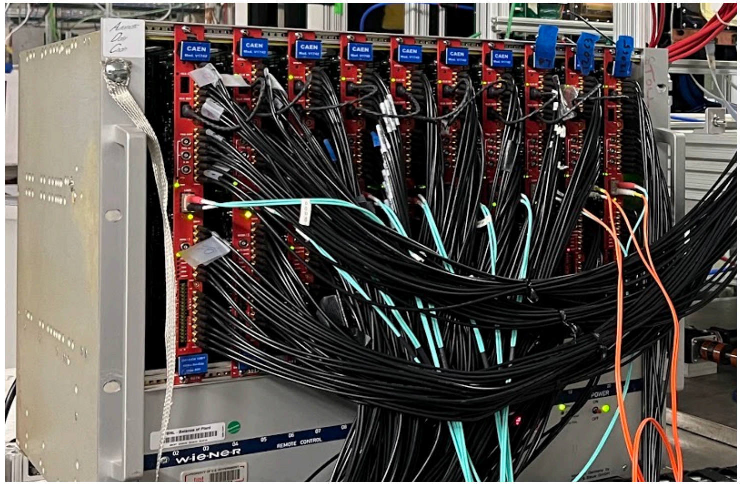


Rear side (cover open): laser head, LAPPD enclosure, XYZ-stages

- Picosecond PiLas laser
- Coming soon: Menlo Systems femtosecond laser
- Compact light-tight enclosure
- 512 DRS4 channels (V1742 digitizers)
- MCX to high-density Samtec adapter cards
- 8 GHz analogue bandwidth 50 GS/s scope

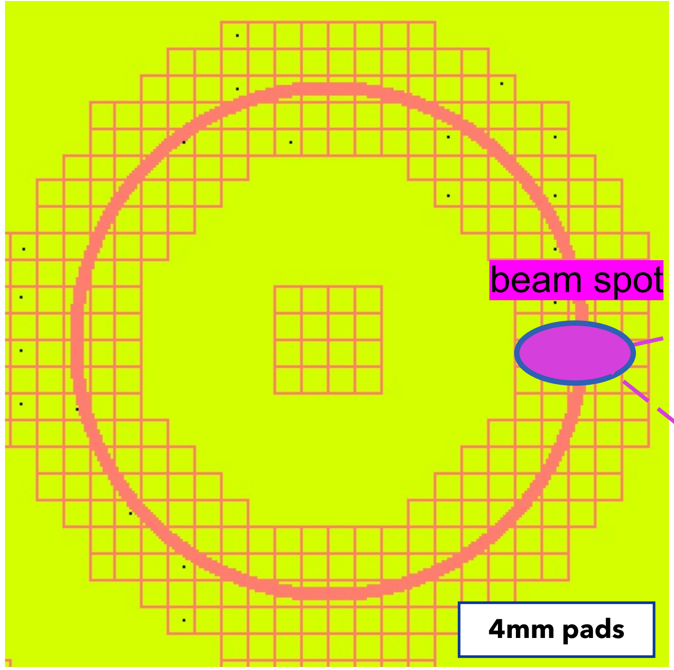


Front side: readout PCB, MCX adapter boards, HV

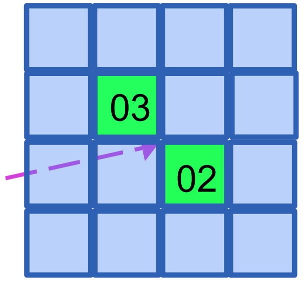


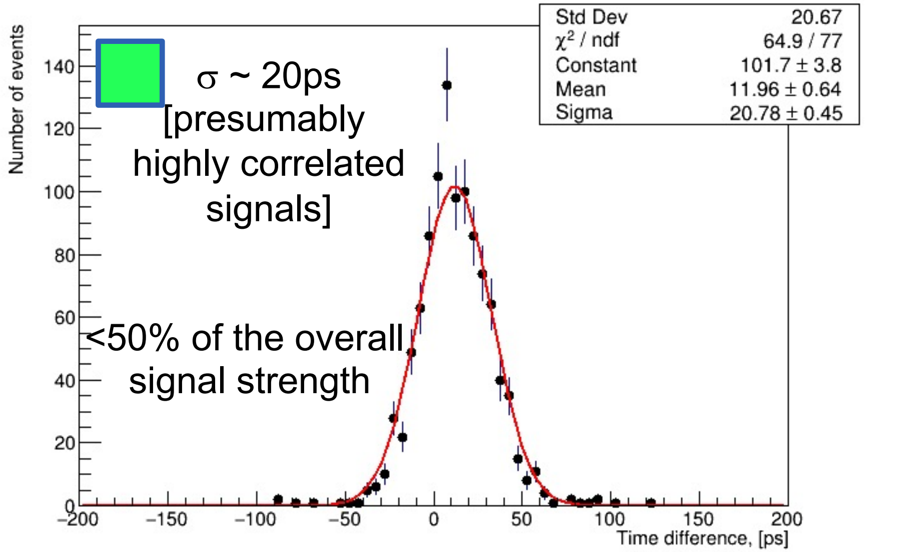
Similar type of equipment exists at INFN Trieste

Beam tests at Fermilab (BNL & Co)



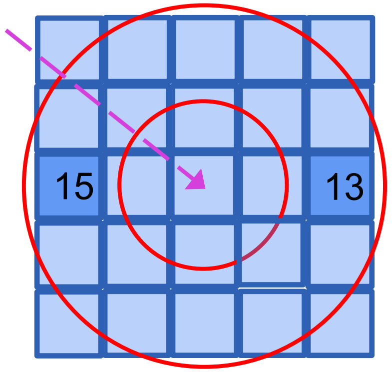
Event selection (A)

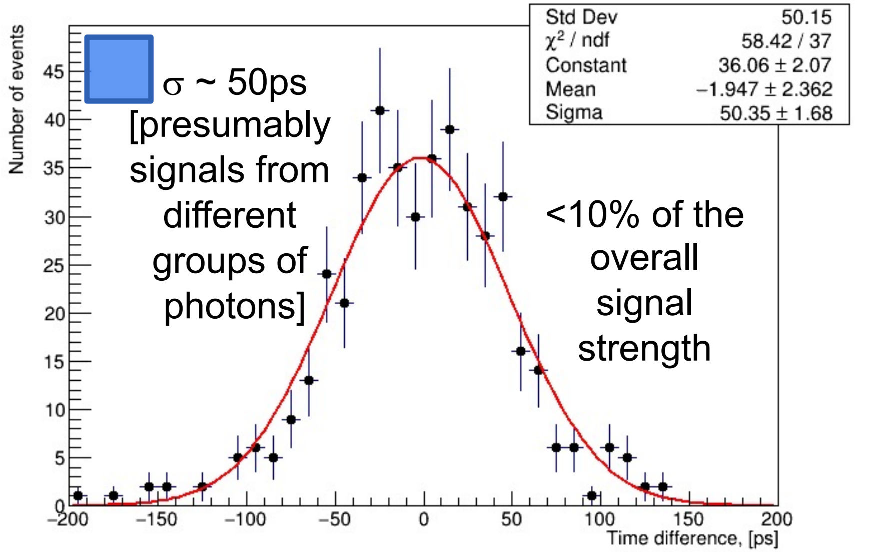




DRS4 chip#0: time(ch#03) – time(ch#02

Event selection (B)





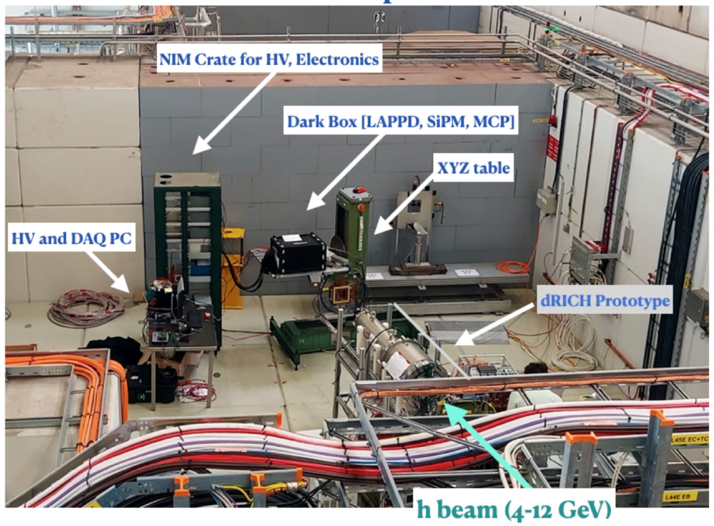
DRS4 chip#1: time(ch#15) – time(ch#13)

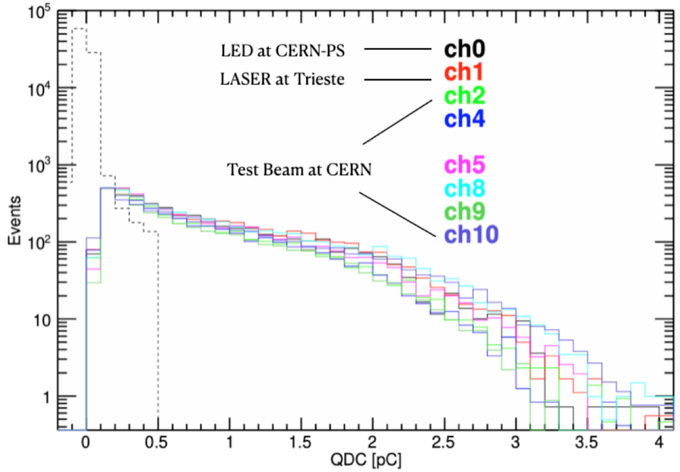
- *Single* photon TTS <50 ps
- 5mm thick UV grade quartz window: a 120 GeV proton produces a **blob of ~100 p.e.'s**

Due to the TIR, photons only hit the PC in a radial band ~[5.5 .. 12.0] mm

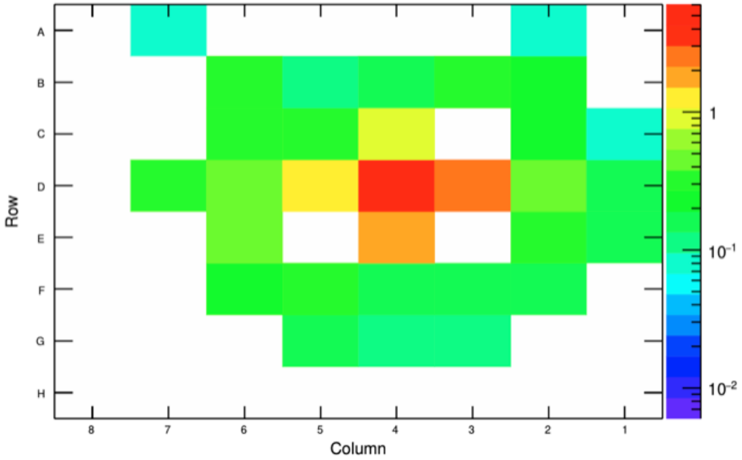
Beam tests at CERN (INFN Trieste / Genova & Co)

First Beam Test of LAPPD in parasitic mode at CERN-PS

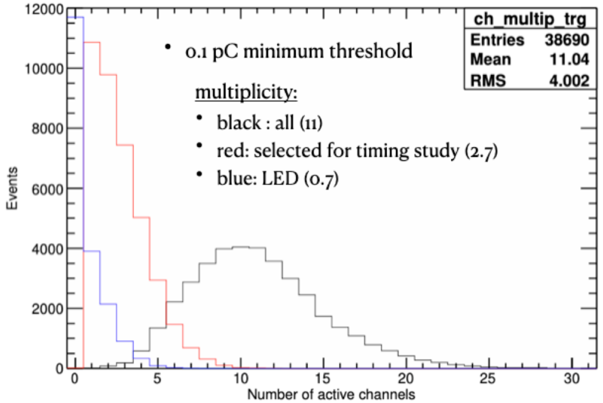




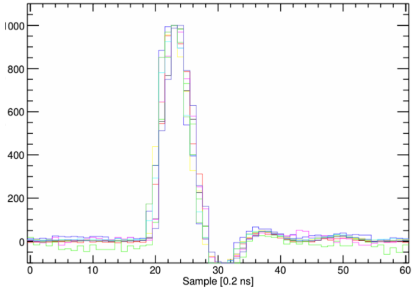
- Primary charge-spectra calibration in SPE is performed.

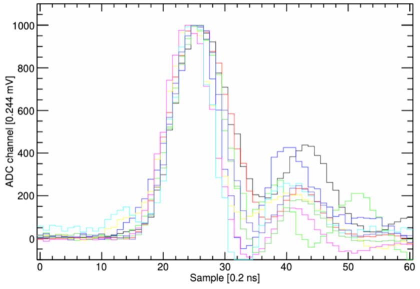


- Average charge collected in the Ring is lower that the SPE .



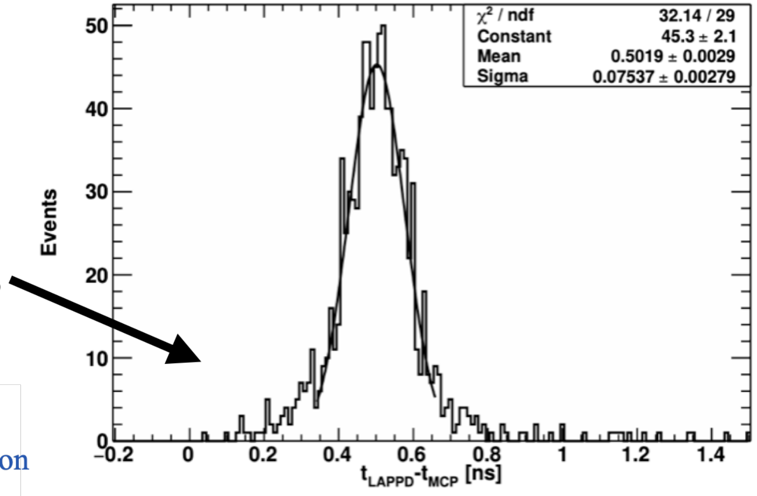
- Central Pad was flooded
- Only 24% of the hits were selected for timing





- Digitised MCP signal
- Digitised LAPPD signal

- The time difference is fitted by a Gaussian within 2σ
- The mean of 0.5 ns agrees with a preliminary GEAN4 simulation
- The obtained σ varies within 80-130 ps, within <10 ps error
- The best resolution found in Channel 2 is 75 +-3 ps



- Timing difference between channel 2 and MCP

3. Perspectives of photosensor mass production

- **We set up a meeting between EIC leadership and Incom**
  - A site visit on January 12th this year, and a facility tour

  - Incom is producing thousands of large area Micro-Channel Plates for medical applications
  - EIC pfRICH demand is 2x68 12cm x 12cm plates
  - In terms of HRPPDs: pfRICH requires 68, DIRC requires 72, for a total of 130 tiles

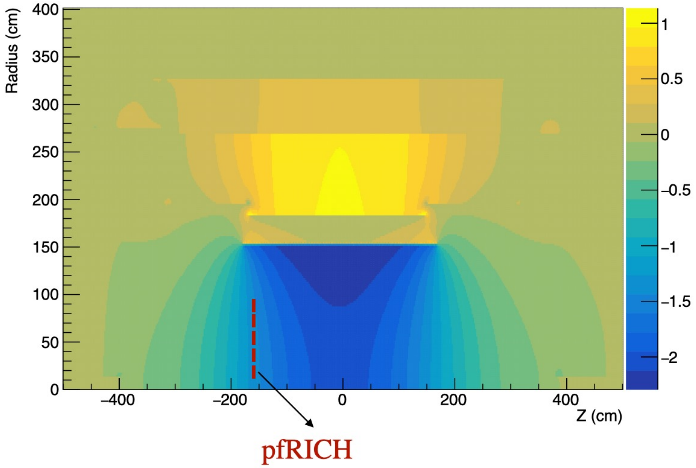
  - Currently Incom is able to successfully seal one LAPPD / HRPPD tile a week
  - With a minor modification of the sealing tank should be able to process two tiles in parallel
  - Incom CEO assured us that they can ramp up the HRPPD production once the order is placed

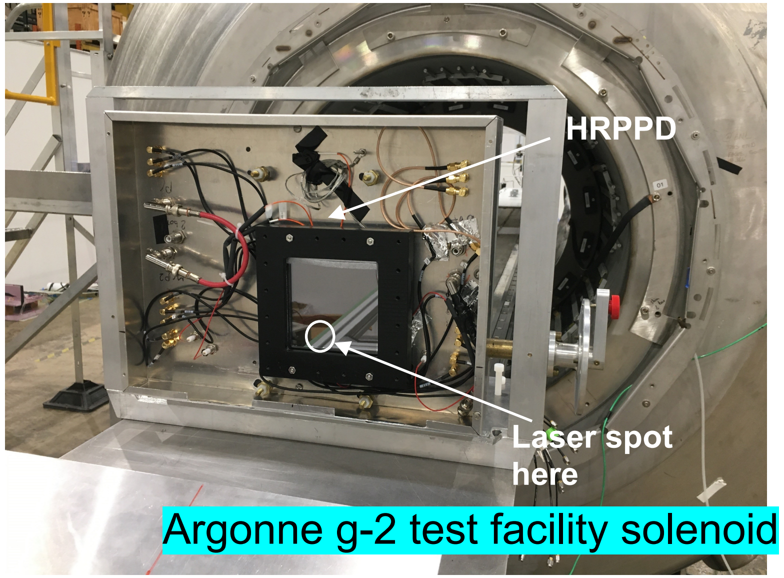
  - Should the first batch of five HRPPDs be successful, Incom must be able to finalize the remaining small design modifications by EIC CD-3 in Spring 2025

  - In case anything goes wrong, see slide 6 for the alternative solutions

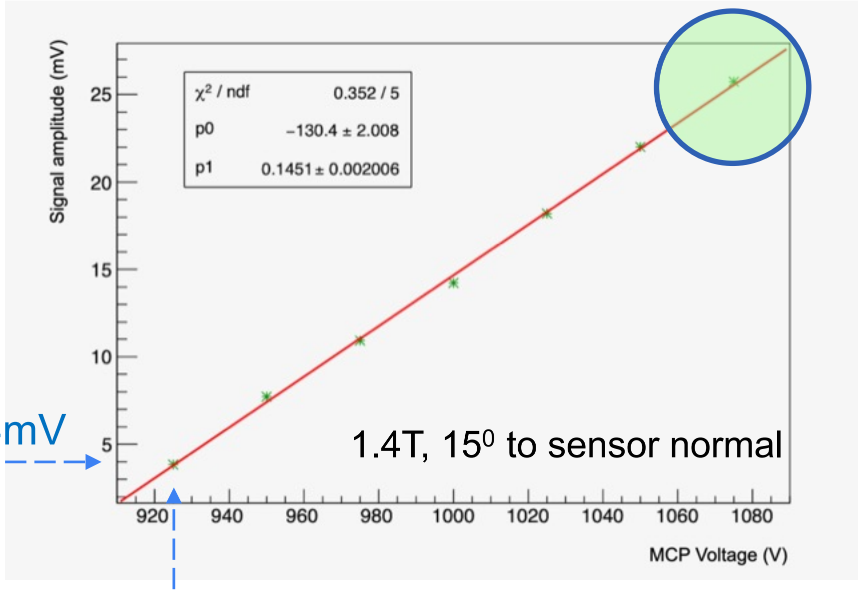
HRPPDs in the Magnetic Field

ePIC solenoid magnetic field (Tesla) in **Z direction**;





by Zhengqiao Zhang (BNL) and Deb Sankar Bhattacharya (INFN Trieste)

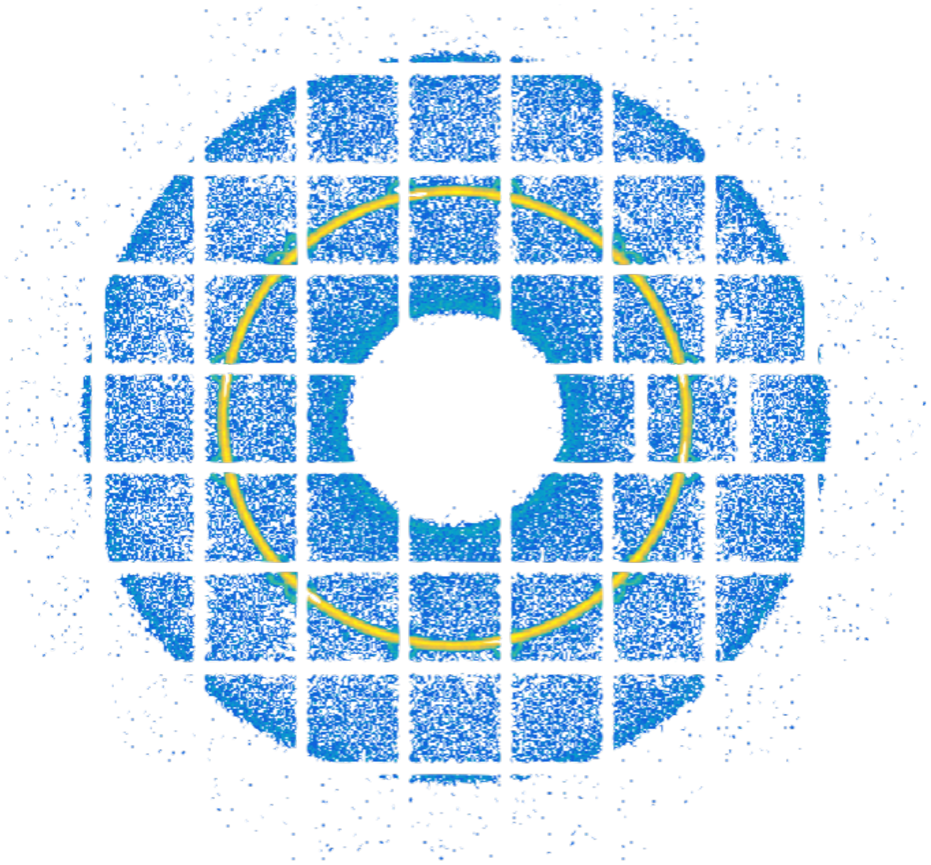


~4mV

Nominal HV to achieve 25mV signals at B=0T

- ➢ In ePIC pfRICH HRPPDs will be exposed to a magnetic field of ~1.4 Tesla at an angle up to 12.6 degrees
- ➢ Tests of a HRPPD prototype in a high magnetic field were carried out by Argonne and Incom using g-2 calibration solenoid
- ➢ Data analysis by eRD110 members of pfRICH team

Preliminary conclusion: gain in this high magnetic field can be fully restored by increasing HV from 925V to ~1075V



ASIC: EICROC

4. Characteristics of ASICs and FEEs considered?

- **A standard requirement list**
  - Provide timing resolution <20ps and amplitude measurement
  - Work with collected charge from few dozens to few hundred fC
  - Work with a relatively high detector capacitance up to 10 pF
  - Have high channel density (64 channels per ASIC and more) and few mW/ch power dissipation
  - Streaming mode

<u>Waveform digitizer (by Nalu Scientific)</u>

- Pros
  - Expect higher timing resolution overall
  - Performance less affected by signal shape
- Cons
  - High expected power dissipation
  - None is readily available with a high channel density
  - Therefore realistically one should consider more space

<u>TOA/ADC (by OMEGA group)</u>

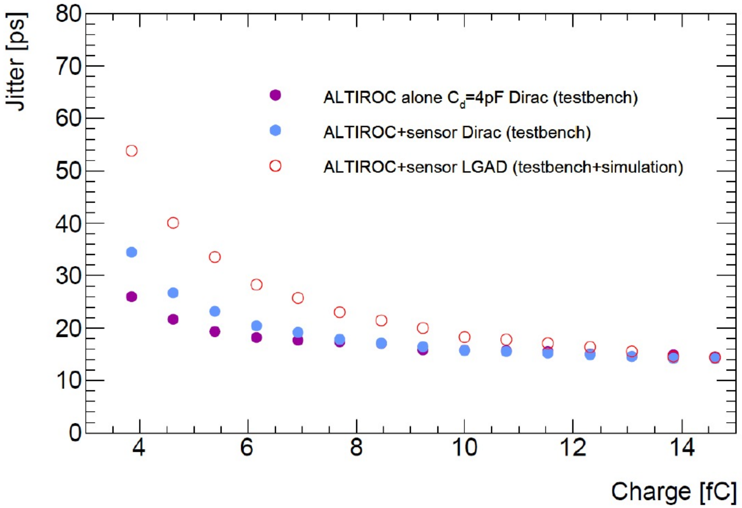
- Pros
  - EICROC is supported by the EIC project
  - Expected power dissipation <3mW/ch
  - Should work with HRPPDs at a lower gain
  - Should provide <20ps timing for C_d ~ 5pF
- Cons
  - Assumes signals have a “regular” shape

5. Status of FEE identification

- ➢ Together with eRD109 consortium we set up a meeting with MCP-PMT experts, m(pf)RICH and DIRC representative and EICROC ASIC designers: https://indico.bnl.gov/event/18539/

- ➢ **pfRICH ASIC choice: EICROC by OMEGA group**
  - ➢ Meets the overall requirements
  - ➢ Will be available in 256+ channel configuration
  - ➢ Will be developed for ePIC AC-LGADs anyway

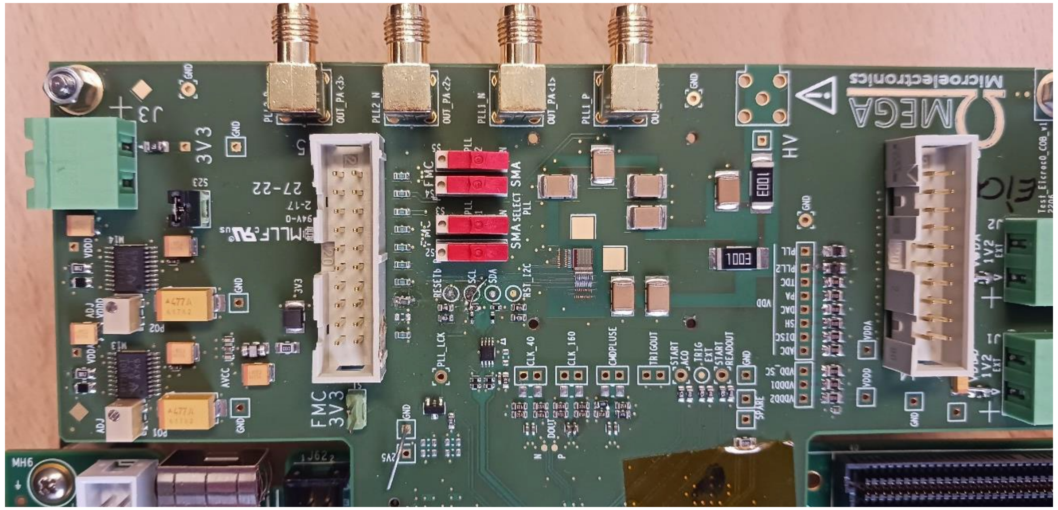
One pixel design
- Preamp, discri taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout : FIFO depth 8 (200 ns)



- 16 channels COB
- Sensor : AC LGAD Cd~1 pF
- Dyn range 0.3 fC to 100 fC
- Noise : 0.3 fC
- TOA Min threshold ~4 fC (Cd=4 pF)
- Time walk ~0.7 ns (Cd=4 pF)
- Jitter ~100 ps/Q(fC) (Cd=4 pF)
- Pd = 3 mW/ch

6. Status of FEE development

- 4x4 EICROC0 ASIC version exists
- Evaluation boards are distributed
  - EICROC0 is a 16-channel testchip for AC-LGADs at EIC
    - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
    - Reads 500x500 um pixels for sensor evaluation
    - Readout designed for testbeam (not EIC)
    - Fabricated in march 2022, received beg july 2022
    - now under test at IJCLAB and OMEGA.



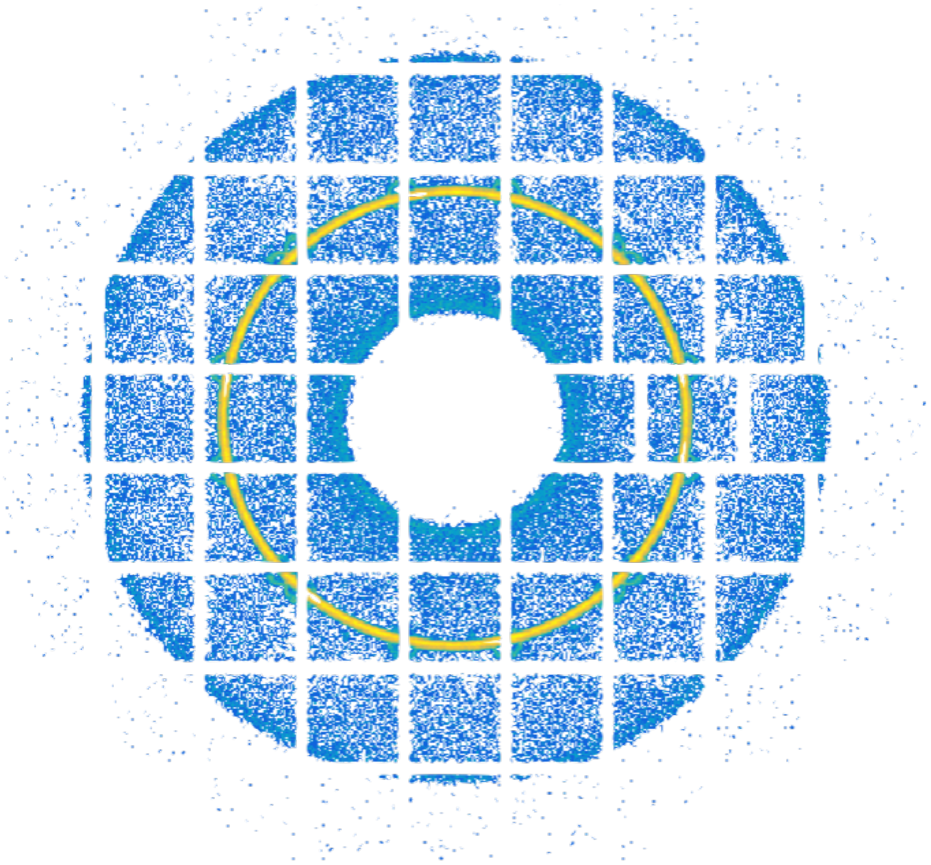
- 256-channel version will not become available until end of 2024
  - pfRICH prototyping will proceed using existing 64-channel HGCROC ASIC
  - BNL has 512 DRS4 channels, sufficient to perform a proof-of-principle π/K separation measurement in spring 2024, should HGCROC path does not work

7. Perspectives of FEE mass production

- 256-channel version will become available towards end of 2024 (?)
- This modification would meet pfRICH packaging requirements

- ePIC AC-LGAD pixel detectors will need ~9M channels
- pfRICH channel count is <70k

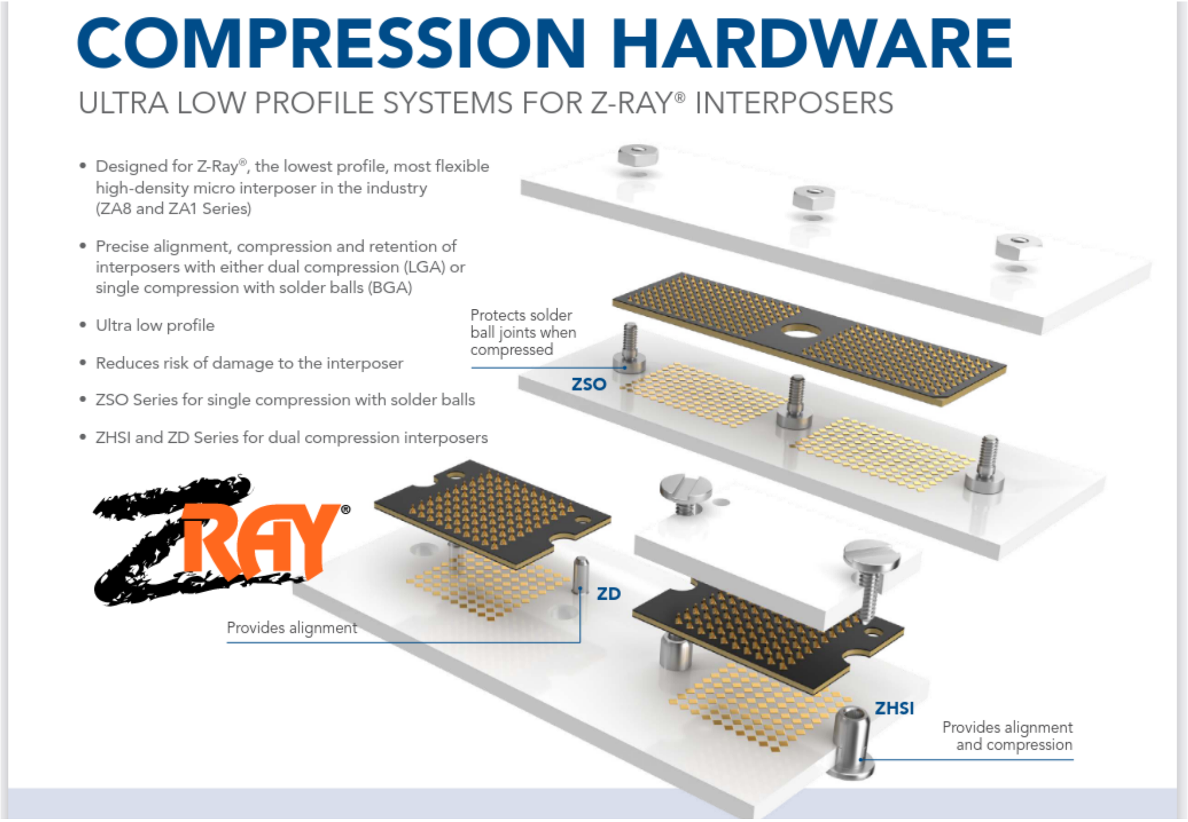
- pfRICH may benefit from a final 32x32 channel modification
  - Reduce occupancy for quartz window photons
  - Improve spatial resolution of the sensor plane



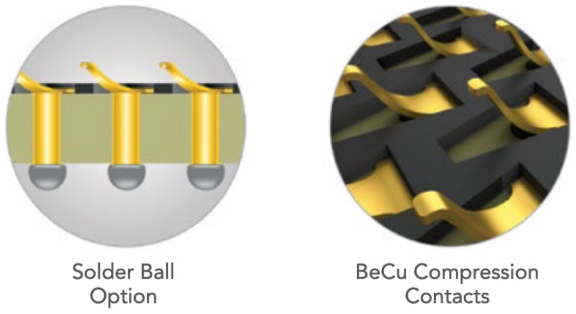
Integration

HRPPD interface to an ASIC readout board

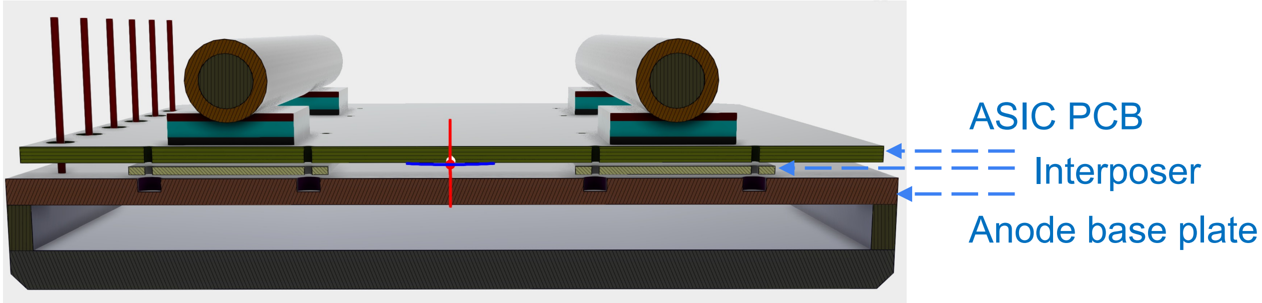
- Samtec compression interposers as a lead option
- Fallback: conductive epoxy or semi-manual soldering



HRPPD anode plate side



ASIC PCB side



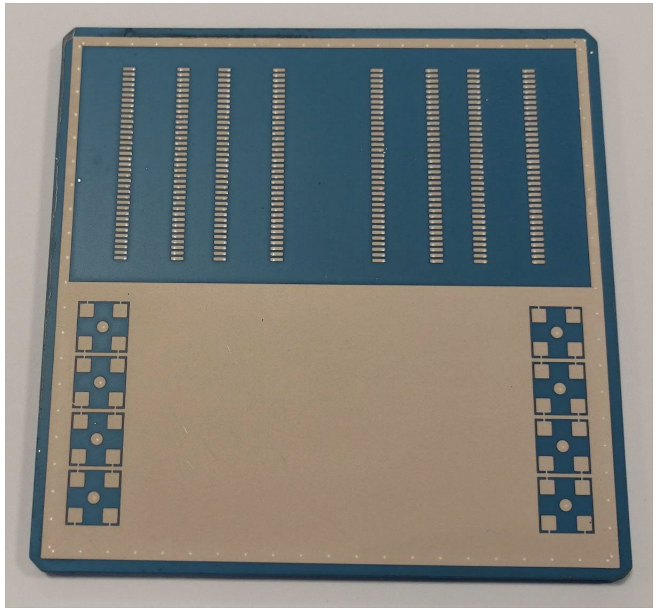
HRPPD face down

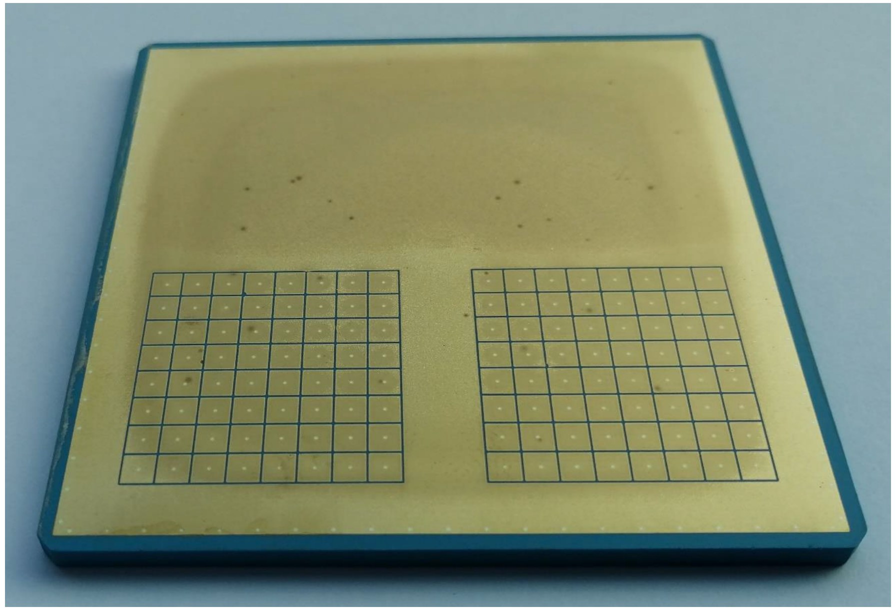
- Will give it a shot in the next few weeks
- This R&D is actually led by BNL

HRPPD anode base plate re-design

- **Need to match interposers to inner volume pixellation and to ASIC PCB**
  - PCB part is “easy” -> reduce 16x16 pad field with a pitch of 1.0mm to pitch 0.5mm in PCB stack
  - What about the HRPPD anode base plate?

    Do the same: consider HRPPD anode plate as a custom multi-layer ceramic PCB





- The first 3” size samples arrived to Incom last week for metrology, electric & vacuum tests
- By early summer 2023 we should have a working solution

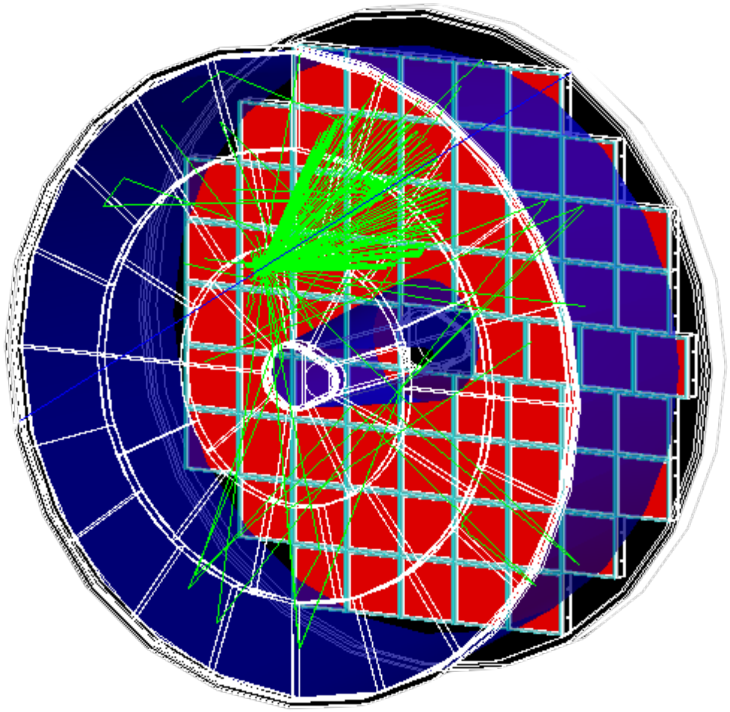
Summary of Sensors and Front End Electronics

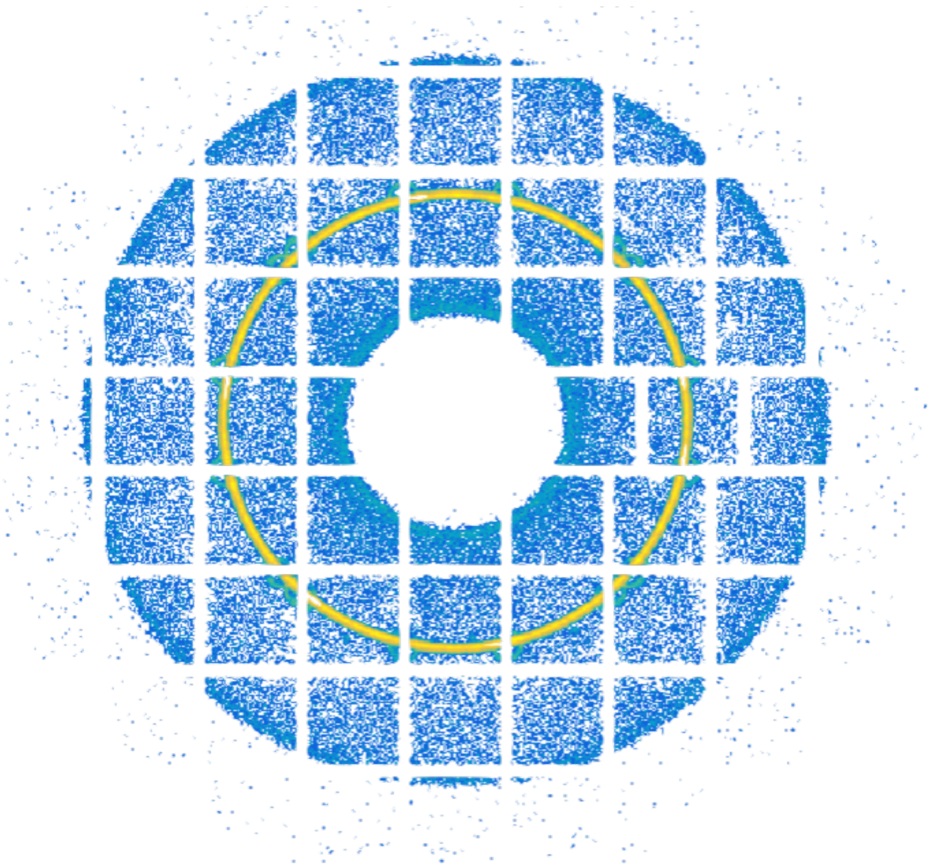
pfRICH photosensors & FEE:

- Photosensor type is selected
- Fallback strategies exist

- ASIC choice is blessed by the EIC project
- ASIC prototyping is being planned

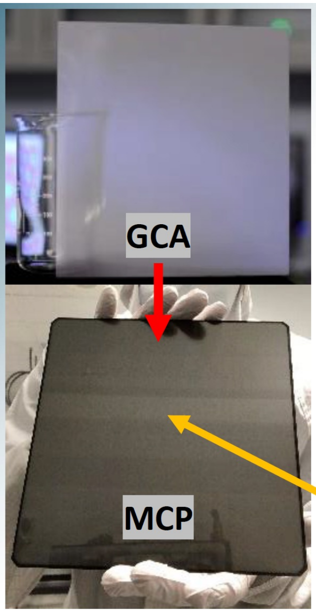
- Sensor to ASIC interface is being actively developed along with the HRPPD modifications required for EIC





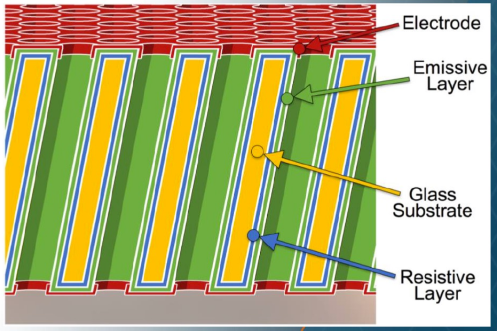
Backup

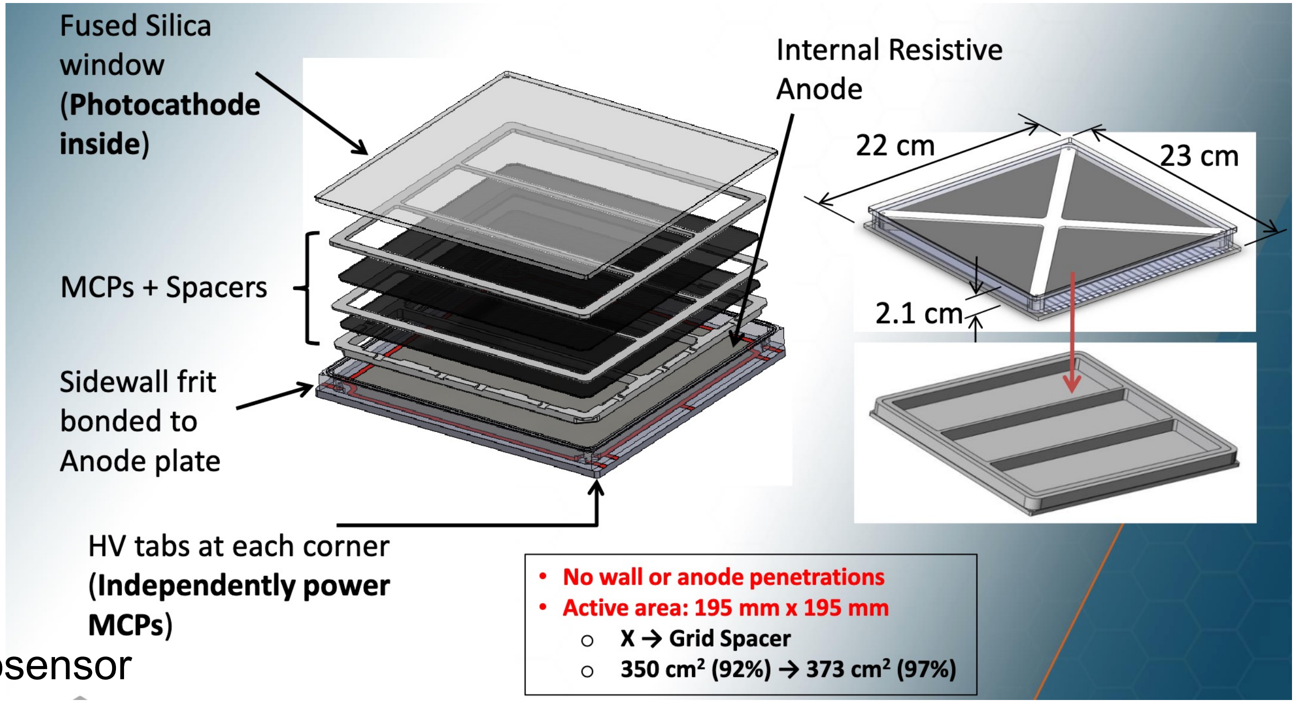
LAPPDs / HRPPDs by Incom Inc.



- *Hollow core* **Glass Capillary Array** (GCA) substrate
  - Borosilicate glass (AKA Pyrex)
    - Little radioactive ^{40}K
  - *No etching necessary! Already hollow*
- **Atomic Layer Deposition** (ALD) is a thin-film deposition technique used to functionalize GCAs
  - **GCA + ALD = MCP**
- Flexible adjustment of film composition and resistivity

Open Area Ratio (OAR) **up to 74%**





- An affordable large area (finely pixelated) vacuum photosensor
- 10x10 cm^2 or 20x20 cm^2 active area
- DC- (Gen I) or capacitively (Gen II) coupled species
- DC-coupled strips or 2D pixellation
- Expected to be (very) cost efficient in mass production
- High enough quantum efficiency and uniform high gain up to ~10^7
- Sub-mm spatial resolution for finely pixelated tiles
- Single-photon timing resolution on a ~50ps level or higher

Gen II variety