

Software Preparation for Commissioning

RIKEN/RBRC
Itaru Nakagawa

Commissioning without beam

1. Apply 100V bias (**HV GUI**). Diagnose any over current channels.
2. Power on a ladder by ladder (**LV GUIs**) and apply 100V bias. Run the calibration. Make sure the results appears in the expected ladder map in the **Calibration Display/Analyzer/Monitor**.
3. Diagnose missing channels and try to recover.
4. Tune the alert range of LV/HV voltage/current control panels (**alert features of LV/HV GUI**).
5. Random trigger noise run (**random external trigger**). Debug any large noise half ladder or channels (**online monitor**).
6. Save dead/hot channels in the database. (**Expert GUI**)
7. Cosmic ray trajectory observation by the **event display** with the **INTT self-trigger** and **standalone DAO**. If the **big-partition** and calorimeter trigger are available, we try to take data with the **calorimeter external trigger**.

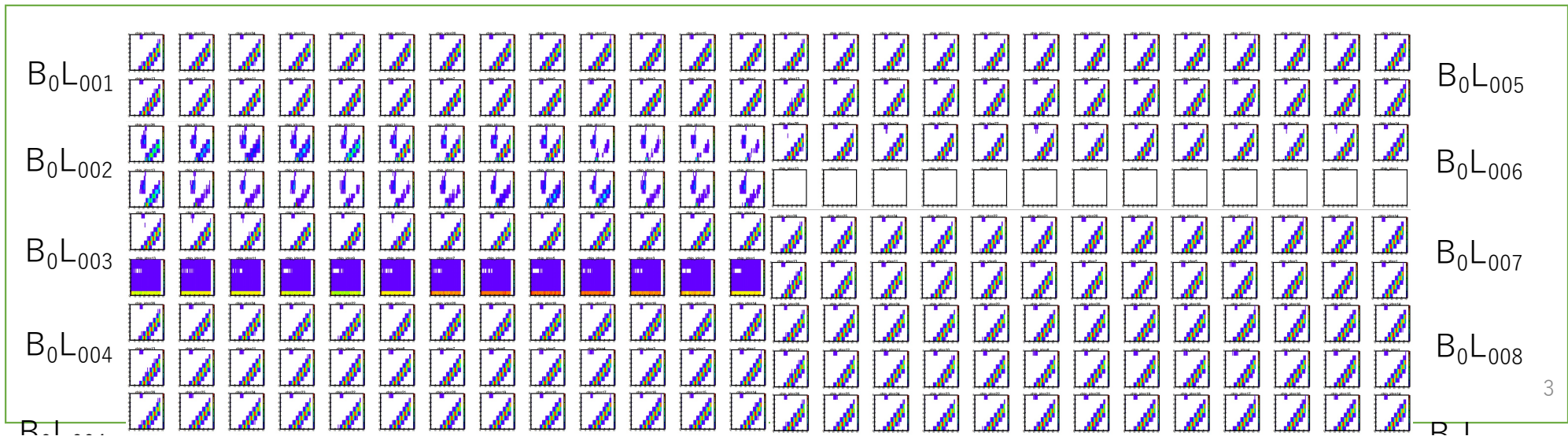


Calibration Display

Misaki Hata



- Should have a calibration results at a glance. At least the results of $\frac{1}{2}$ barrel appears in a single page. Is it possible?
- Perhaps a calibration mode can be implemented to the OnlineMonitor, but #of hits/strip is not sufficient. We definitely need ADC vs. Amplitude 2D plots.
- Any warning capability like the online monitor?

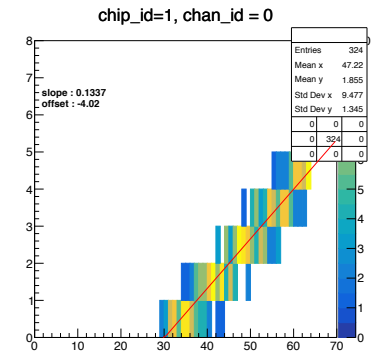


Calibration Result Analyzer

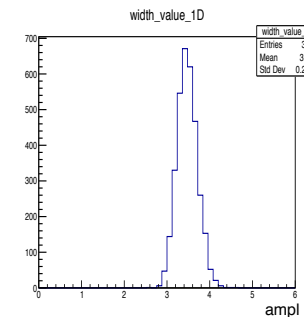
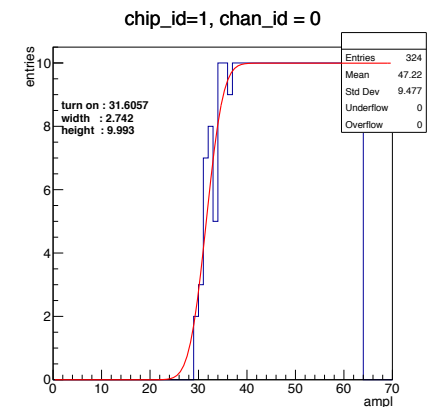
Calibration results are to be simplified into key characters and textualized such as :

- # of entries /chip (half entry, partial data drop to be detected)
- ADC vs. Amp slope
- Thresholds
- Noise levels
- # of bad channels/chip
- These textualized results are to be saved in the calibration database.

The codes developed for the ladder QA can be used. Are these codes in Fun4all?



Fit function : error function

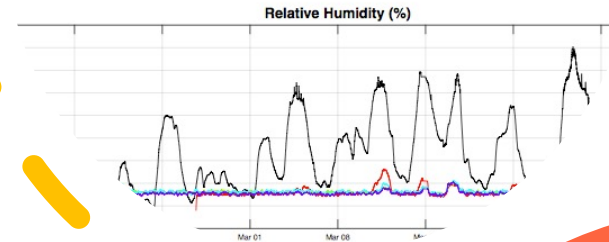
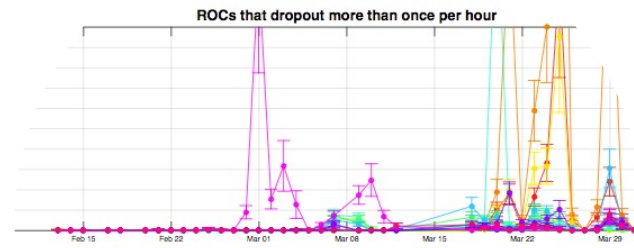


Cheng-Wei's slide
2021/8/11

Calibration Monitor

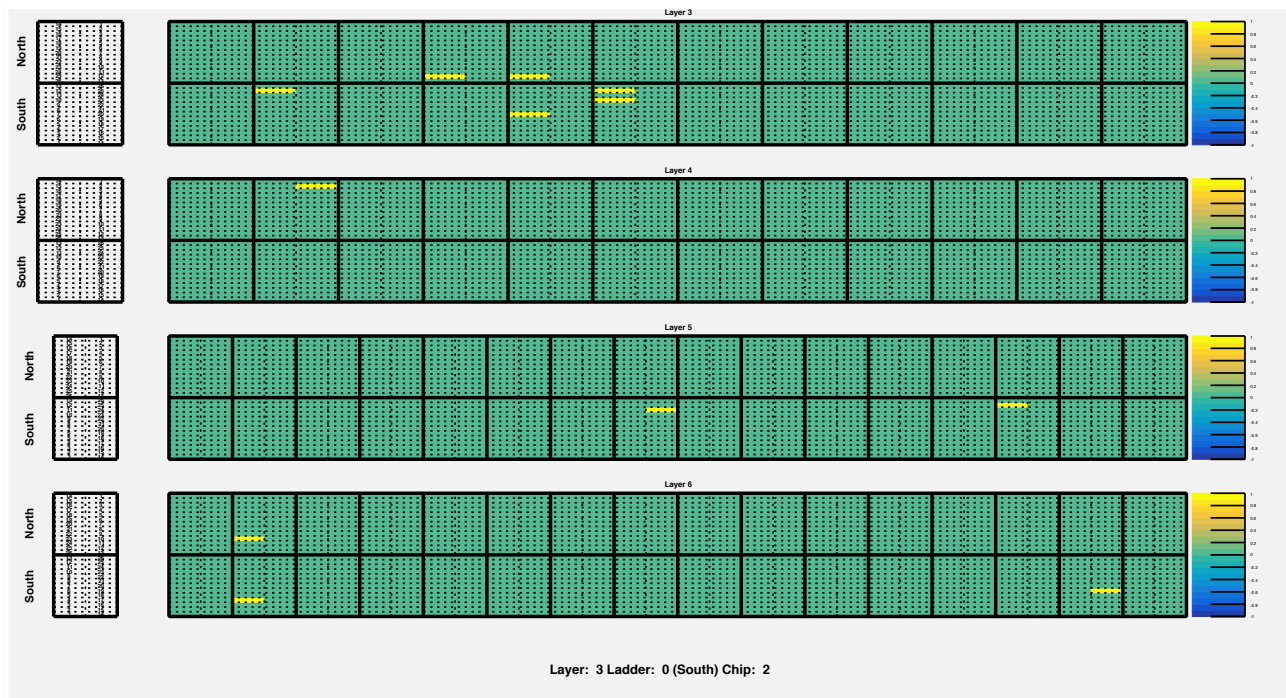
- Calibration run is to be executed regularly a couple of times a day.
- Results are to be monitored by the calibration monitor. The code is to be developed with the same framework with the stability monitor something like

```
%> StabilityMonitor.sh --calib
```



What's New?

Noise rates

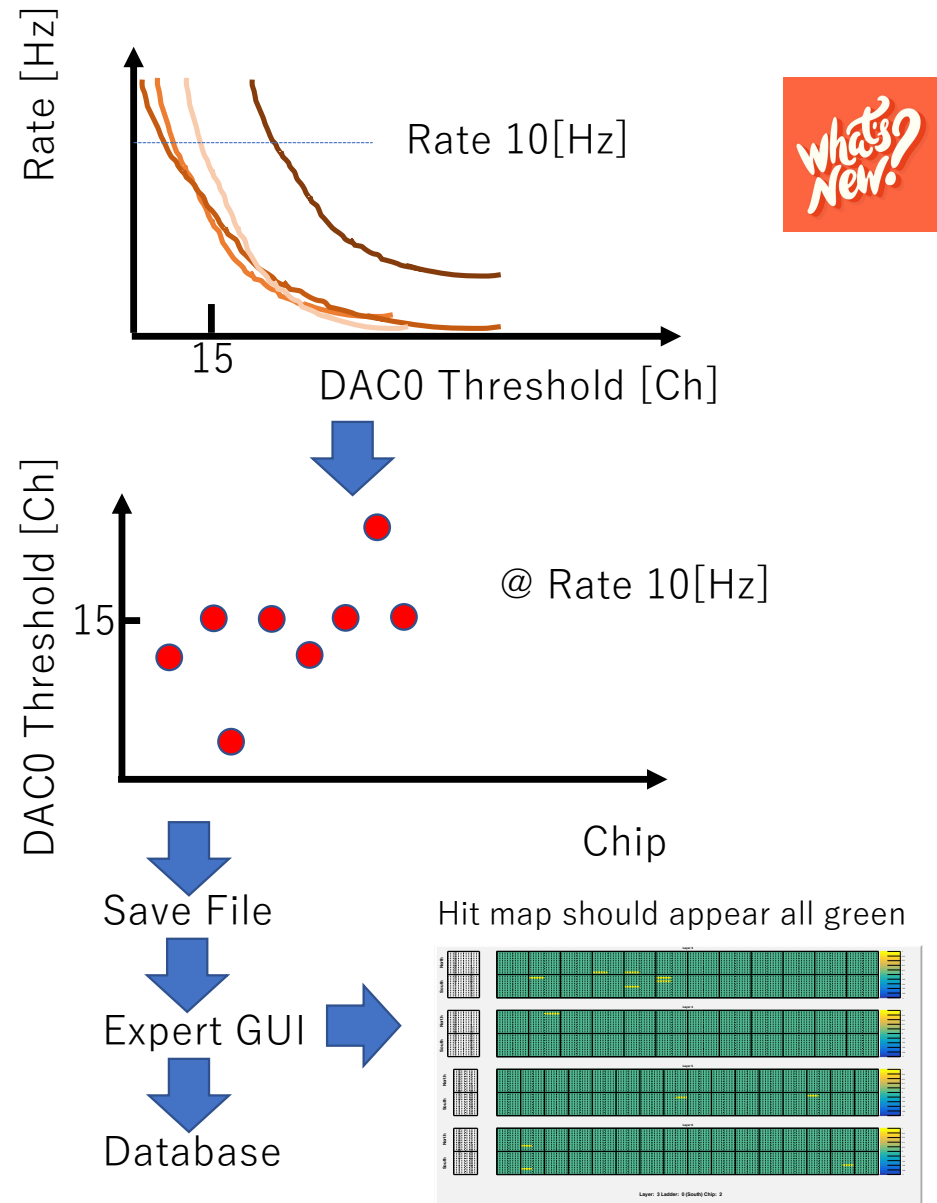


- Data should be taken with a [random external trigger](#).
- Noise rate are to be compared with the [online monitor](#) and check the uniformity of the noise.
- Spot noisy channels and too cold channels and diagnose.

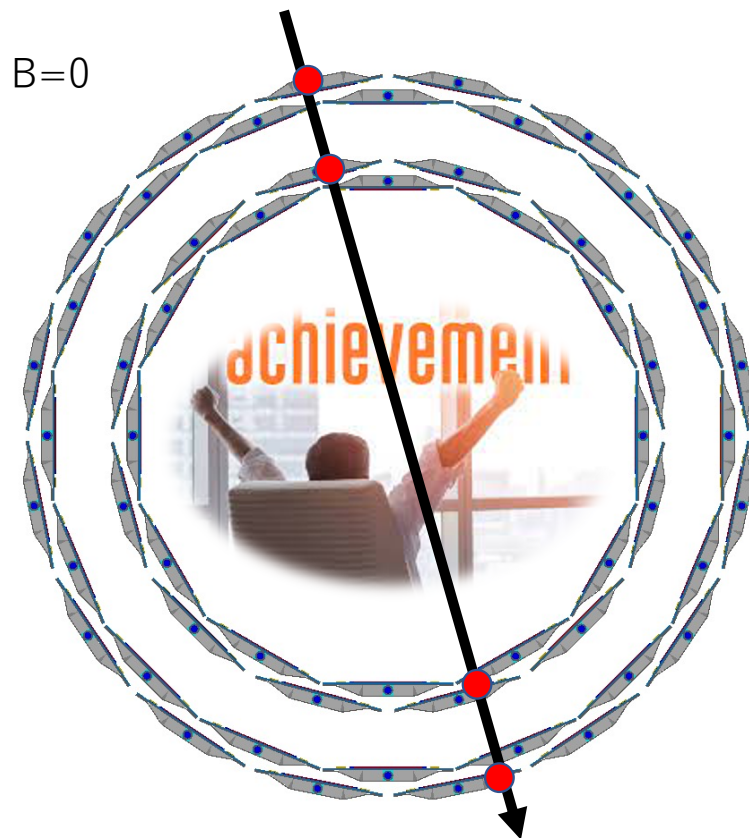
DAC0 Scan

- Scan DAC0 value one-by-one [20, 19, 18, 17, ...] w/ random trigger.
- Optimize the DAC0 threshold for each Chip to give the same given rate. **Save threshold values (52 x 56) in file loadable to Expert GUI.**
- Customize DAC0 threshold setting chip-by-chip (**Expert-GUI**)
- This is the practice for the DAC0 threshold scan with the beam during commissioning. (S/N is also considered w/ beam)

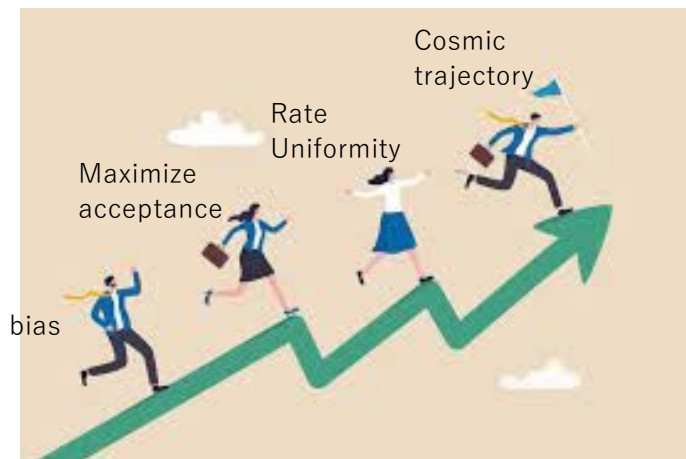
*Additional feature to expert GUI



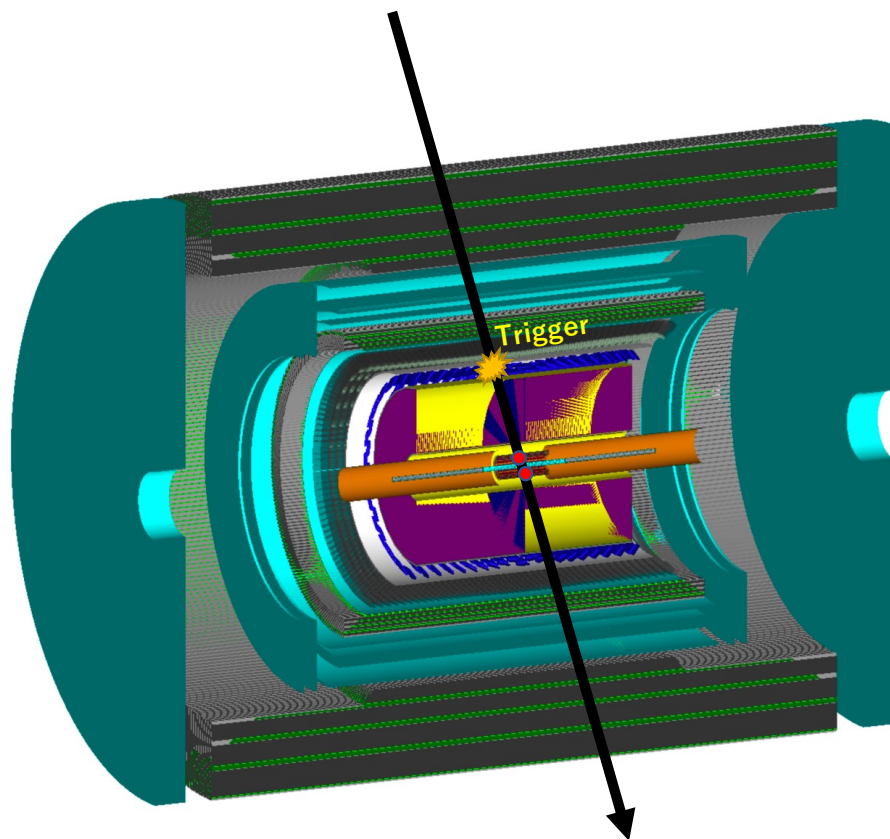
Cosmic Ray Trajectory.



- If the calorimeter trigger becomes available, we may be able to take cosmic data.
- Without the fancy tracking algorithm, we should observe a straight track **by eye** with typical corresponding 4 clusters in each layer using the **event display**.
- The trigger can be the **self trigger** with the INTT standalone, but we may need to set relatively high DAC0 threshold to avoid pile up even after DAC0 threshold optimization.
- The latency should be set around the same setting with source/cosmic rays.



Cosmic Ray Trajectory (Advanced)



- More sophisticated data taking with:
 - Calorimeter external trigger
 - Big partition DAQ? Can be done with the INTT standalone rcdaq?
 - Latency scan with respect to the trigger timing.
 - event display

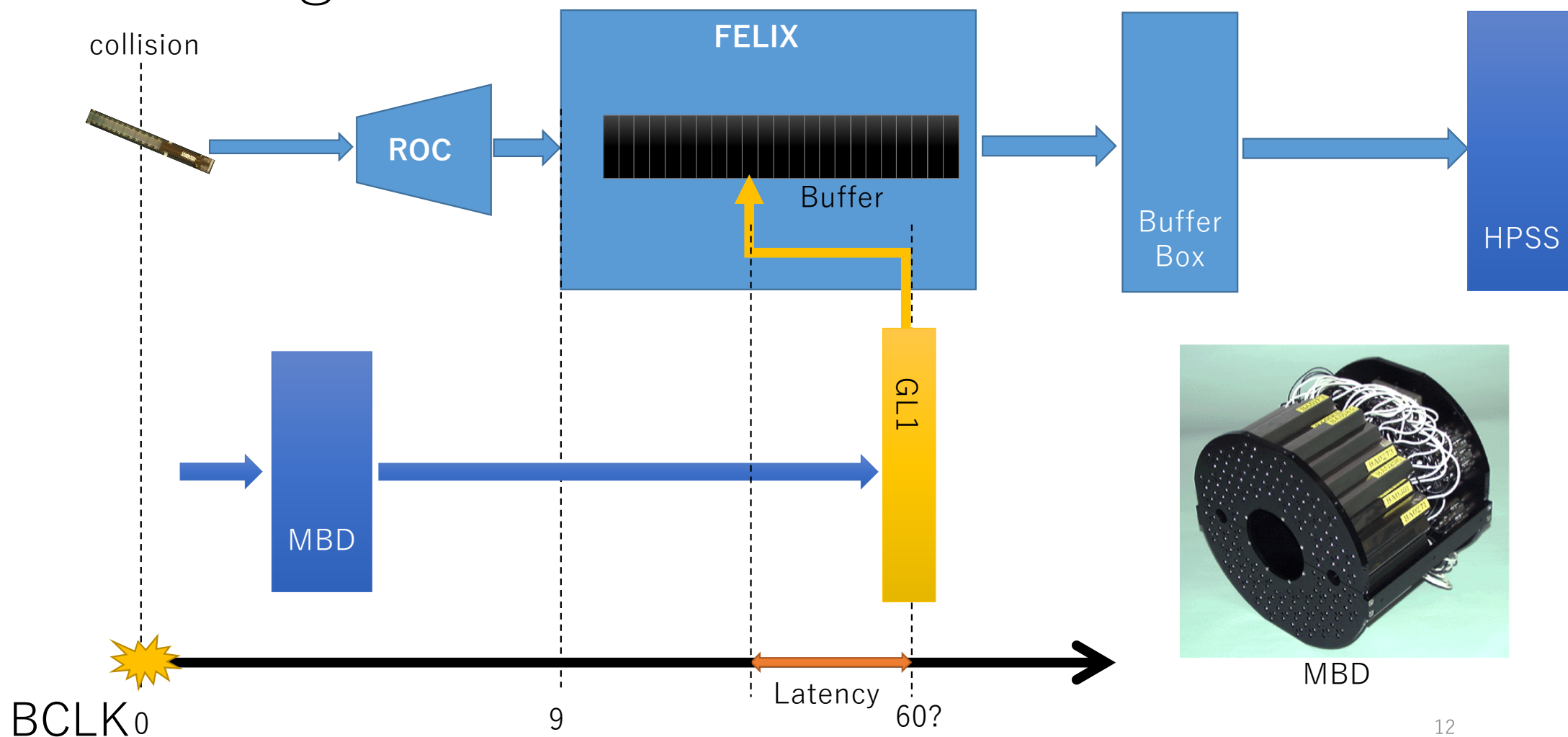


Commissioning with beam

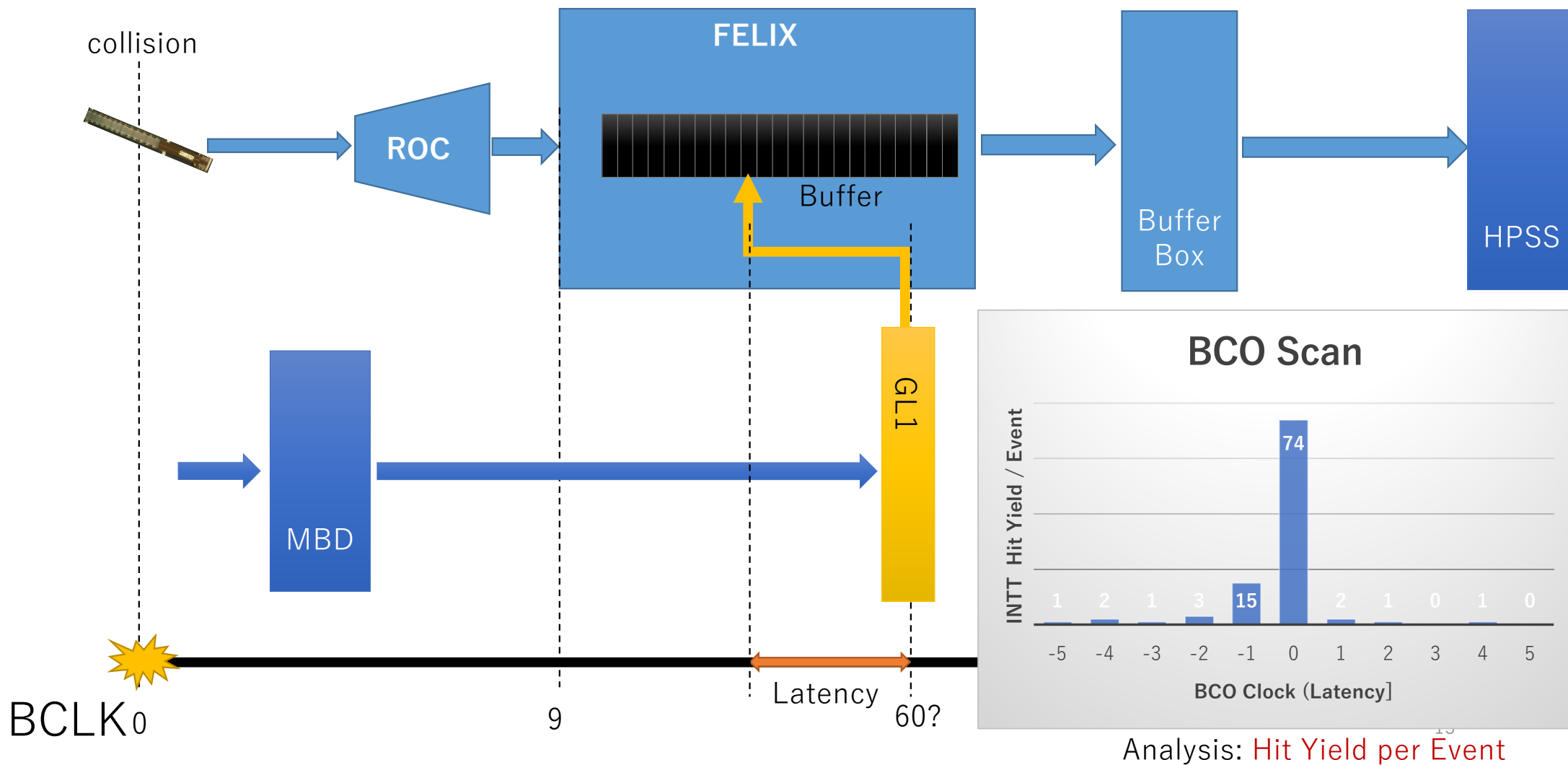
1. BCO Timing Scan (**INTT Hit Yield/Event**).
2. BCO Phase Scan fine tweak the timing with respect to BCO.
3. Mis-cabling check by the geometry (**Event Display**)
4. Diagnose missing channels and try to recover
5. Check yield uniformity (**Online Monitor, Stability Monitor**)
6. Gain matching between ladders or fine tweak noise
7. DAC Scan at HV=100V (**DAC Scan Analyzer**)
8. Bias Voltage Scan (**MIP/MPV Fitter**)
9. DAC0 threshold optimization. S/N evaluation chip by chip.

Timing Tune

Timing Tune



1. BCO Scan



2. BCO Phase Scan

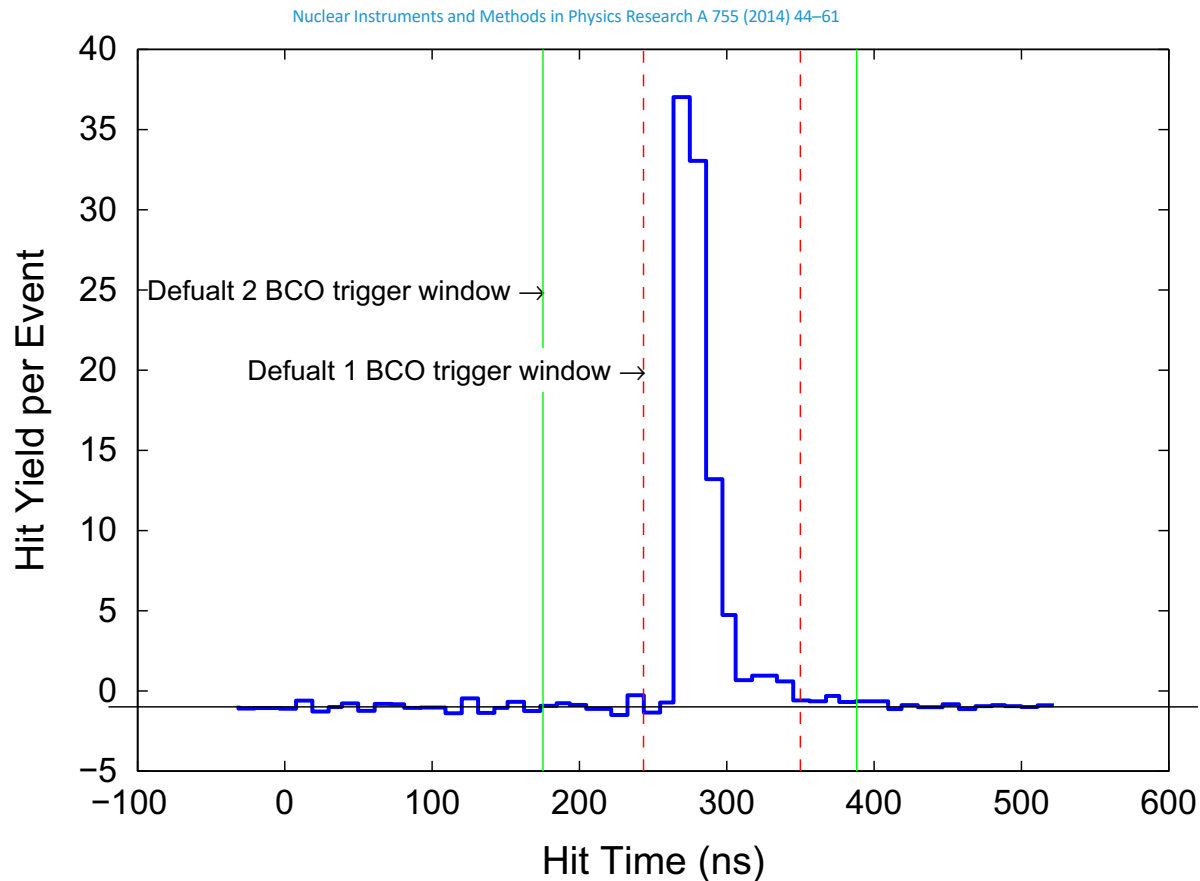


Fig. 32. Timing distribution of the FVTX hits relative to the RHIC beam clock.

6.1. Timing

The distribution in time of FVTX hits is studied relative to the RHIC collision time by comparing the hit rate at different FVTX delay values relative to the RHIC beam clock. The timing distribution for two sectors of wedges in the south arm is shown in Fig. 32. Most hits fall in a window ~ 30 ns wide.

Two standard trigger timing configurations were used during FVTX operation, as shown by the vertical lines in Fig. 32: during relatively low trigger rate running (in heavy ion systems) hits arriving in a time window two RHIC beam clocks (BCO) wide (1 BCO ~ 106 ns) are accepted. In high trigger rate p+p running, a 1 BCO-wide window is used to avoid recording accidental hits from neighboring beam crossings (1 BCO apart).

On 2023/01/12 22:22, Huang, Jin wrote:

That was exactly how it was done and highly recommended for intt too. It took few hours of a special low bunch fill to perform this scan, shifting BCO phase 19-20ns at a time. That appears the only way to set timing for the sub-bco delay
Jin

2. BCO Phase Scan

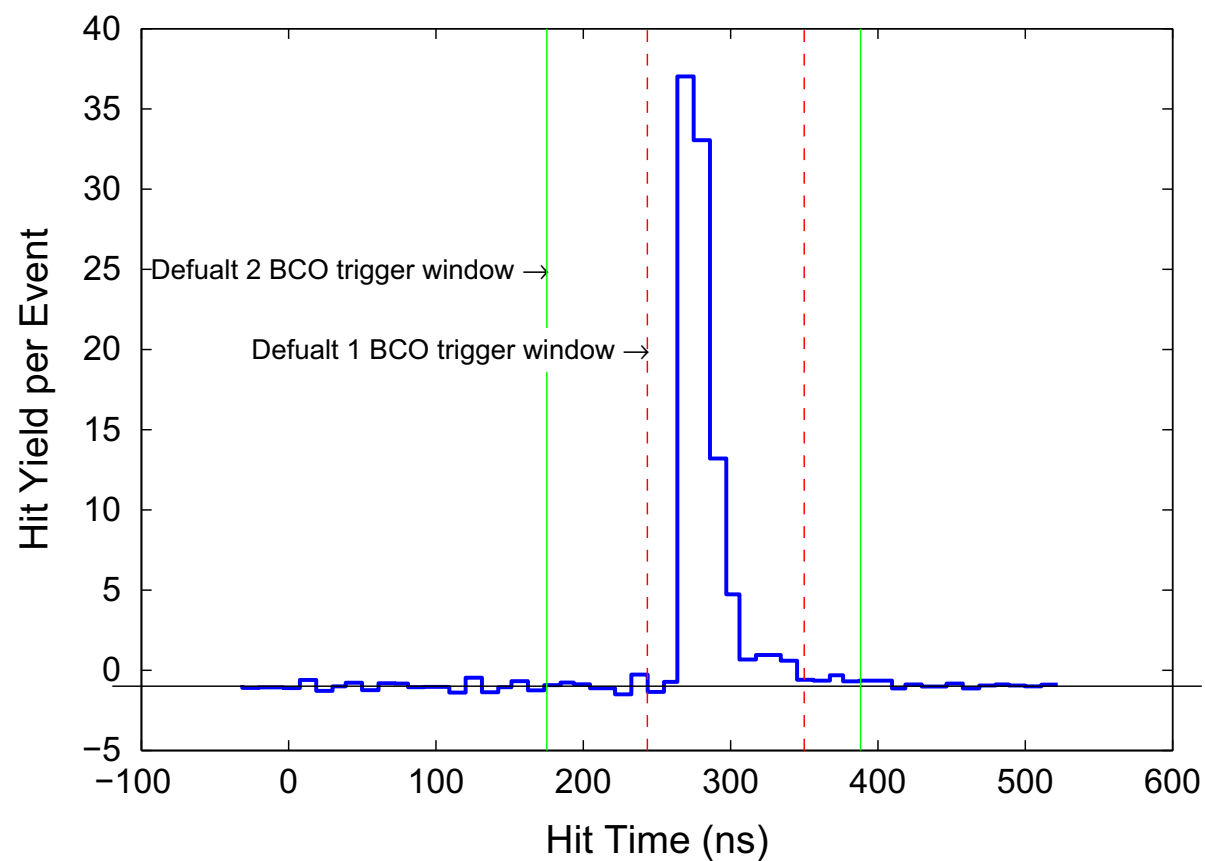
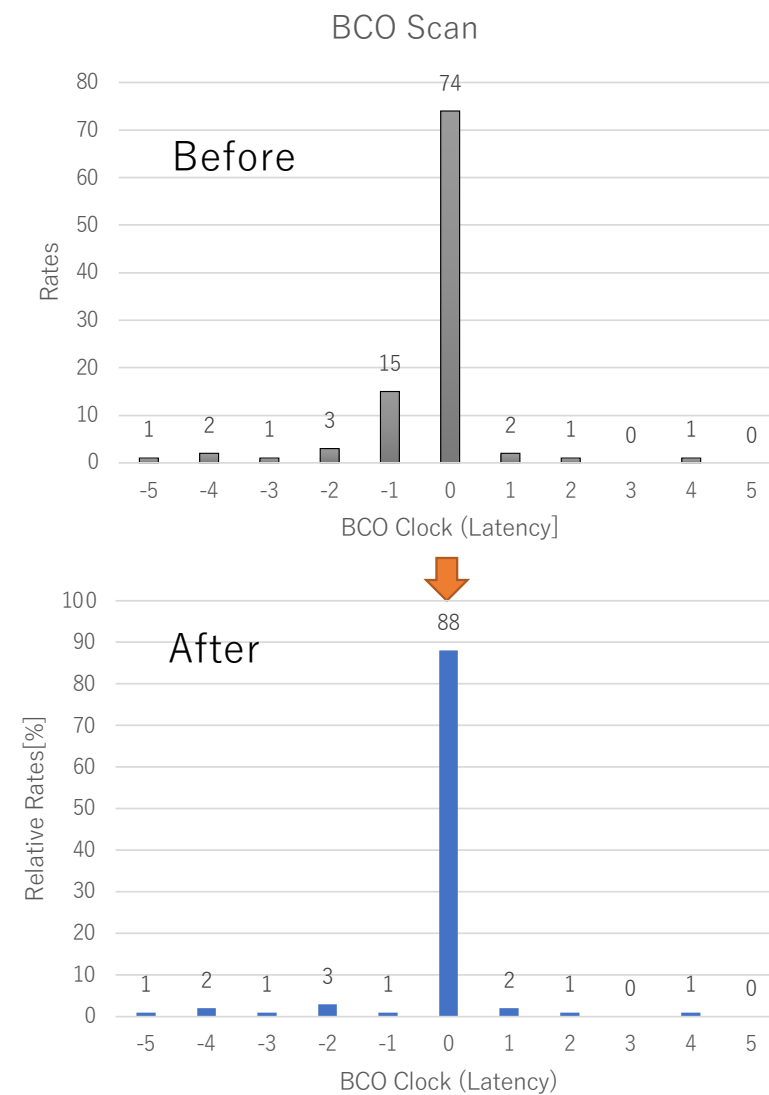
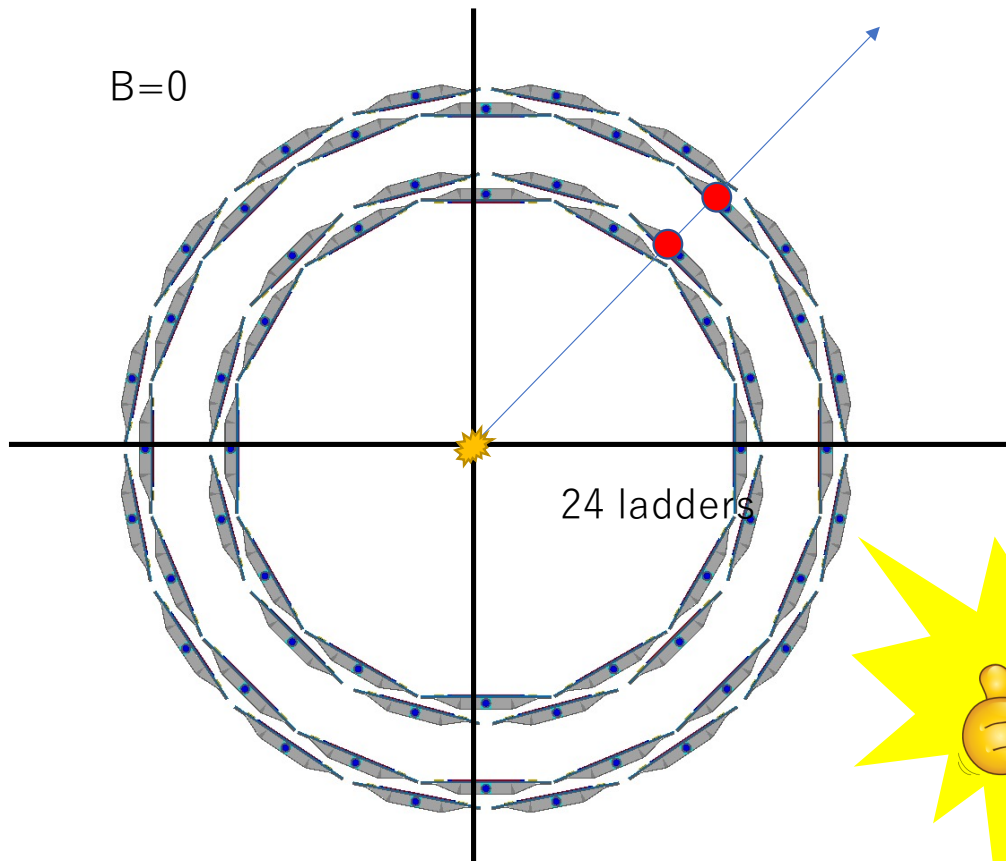


Fig. 32. Timing distribution of the FVTX hits relative to the RHIC beam clock.

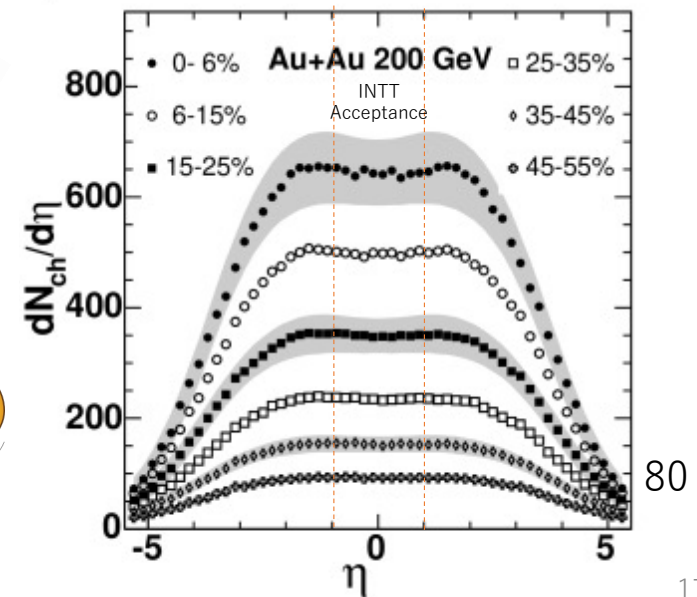
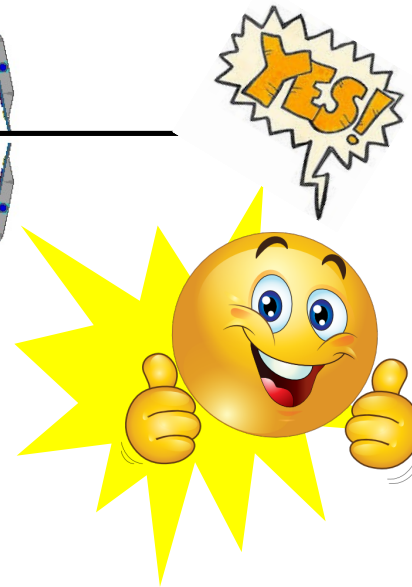


Ladder Geometrical Check

3. Hit Matching

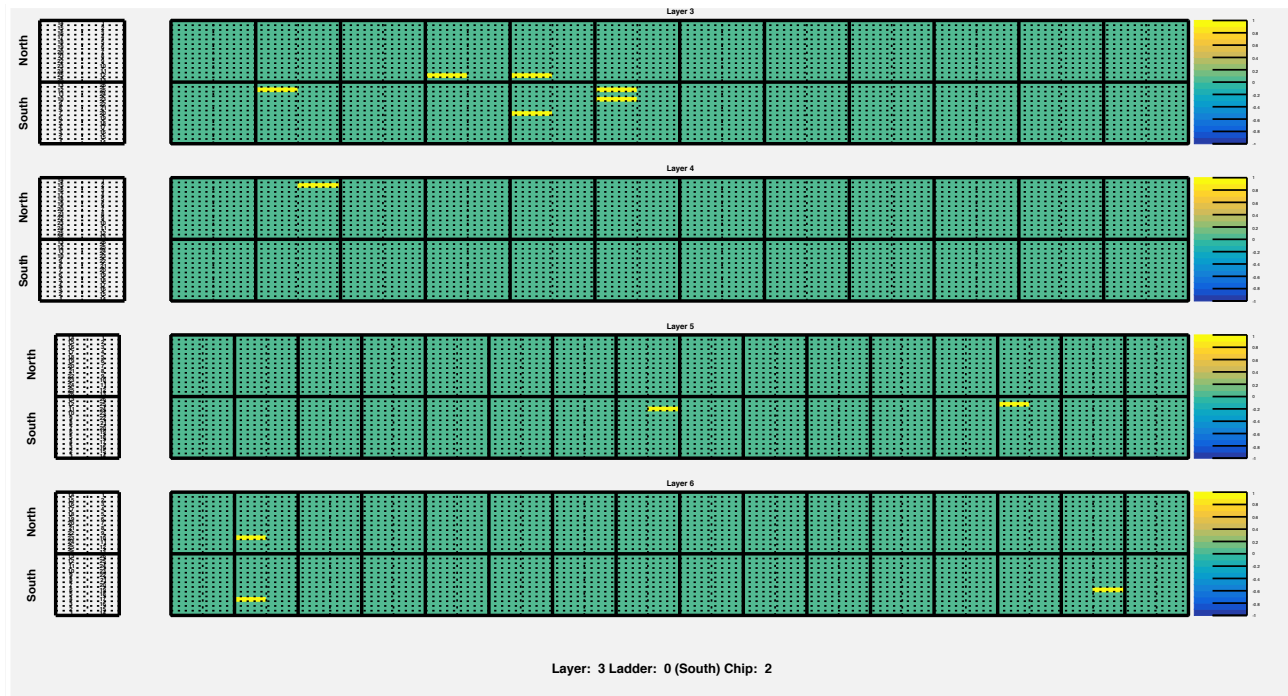


- In early stage of the commissioning, sPHENIX is operated with magnetic field off.
 - Tracks are expected to be straight.
 - At the 45-55% centrality collision, $80/|\eta|$ tracks $\rightarrow$ 4 tracks/half ladder $\rightarrow$ 0.15 hit/chip.
 - Matching hits between L0 and L1 can be identified by eye using the **event display** without fancy tracking algorithm.



Hit Rate Uniformity Check

Hit Rate Uniformity Check



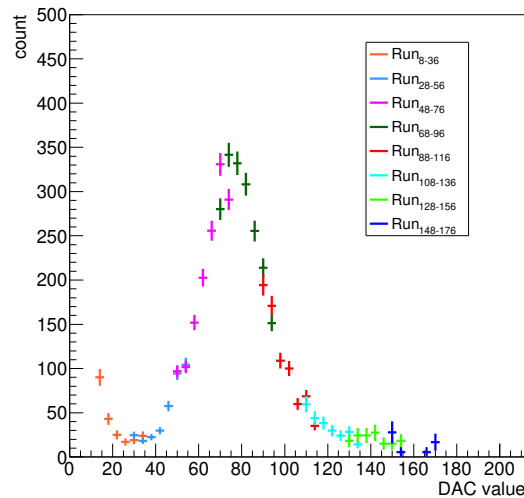
- Definitely need the **online monitor** working.
- Some non—uniformity can be observed by:
 - Bad cable contact
 - Dead channel
 - Hot channel
 - Gain variation
 - ...
- Dead/Hot channel detector is to be implemented.
- This check suppose to be executed periodically after the DAC0 threshold optimization

DAC Scan

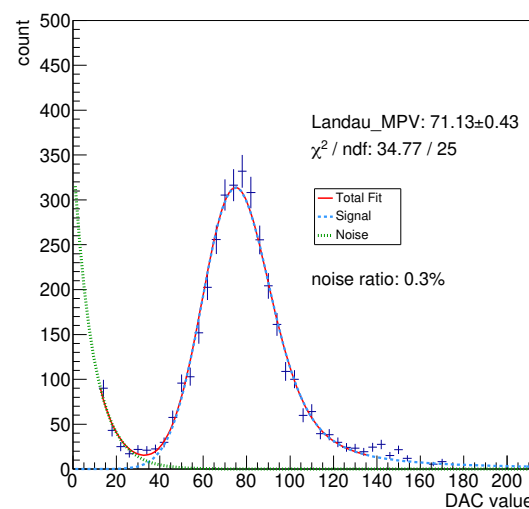
DAC Scan

Scan	1	2	3	4	5	6	7	8
DAC0	8	28	48	68	88	108	128	148
1	12	32	52	72	92	112	132	152
2	16	36	56	76	96	116	136	156
3	20	40	60	80	100	120	140	160
4	24	44	64	84	104	124	144	164
5	28	48	68	88	108	128	148	168
6	32	52	72	92	112	132	152	172
7	36	56	76	96	116	136	156	176

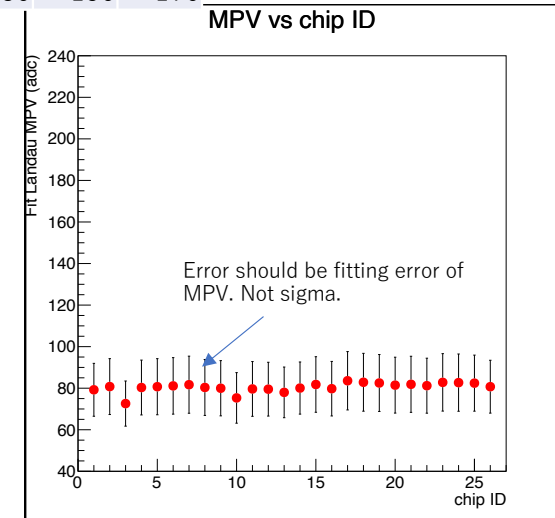
ビームテストと同じ設定で良いか？
オーバーラップ
binは二つ？



- Chip-by-Chip Base
- Clustering (**Optimize offset value**)
- Normalization btwn adjacent runs
- Concatenate all runs



- Fitting with Landau+Gaussian convolution function.



Half ladder by half ladder



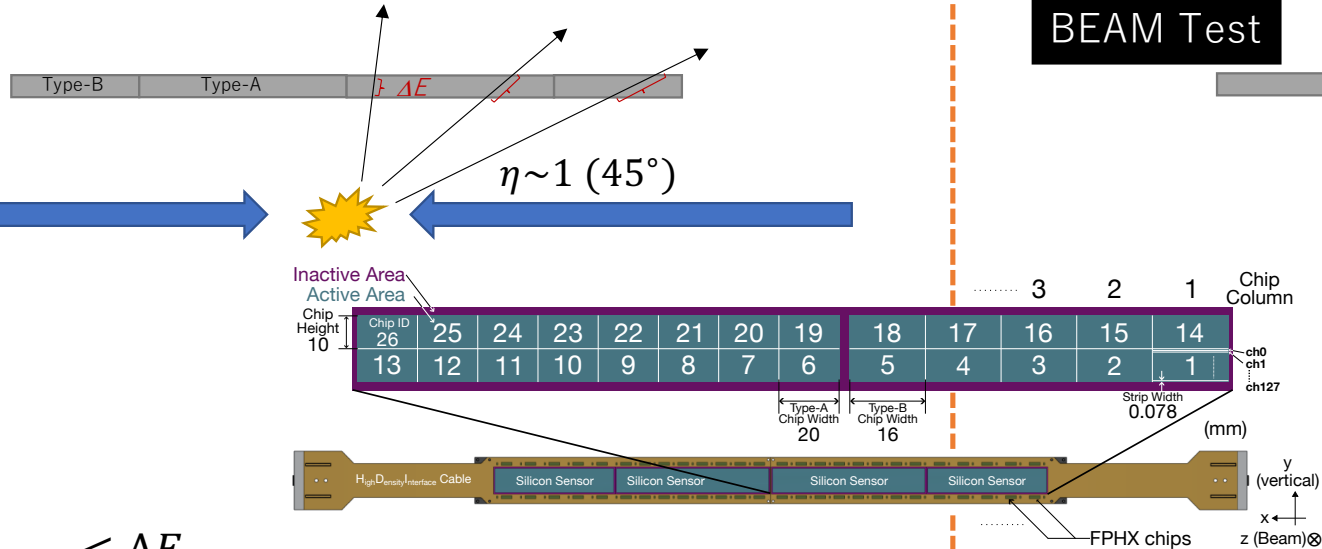
All ladders

Save all fitting parameters:
MPV, Width, ...

How Energy Deposit Looks like in sPHENIX?

DACのオーバーフローが出ちゃうか？

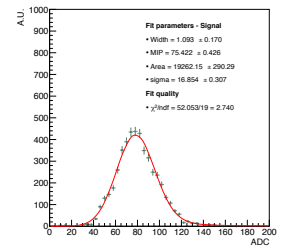
sPHENIX



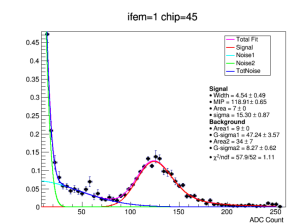
BEAM Test

Cheng-Wei's slide 2022/4/15

Testbeam2021, 50 V
Positron beam, 1 GeV
DAC Scan all 11



Testbeam2019, 100 V
Proton beam, 120 GeV



- $\Delta E_{\text{Type-A}} < \Delta E_{\text{Type-B}}$
- $\Delta E_{\text{chip13}} < \Delta E_{\text{chip12}} < \dots < \Delta E_{\text{chip1}}$
- $\Delta E_{\text{chip1}} \sim \Delta E_{\text{chip13}} \times \sqrt{2} \ (\eta \sim 1)$
- $\Delta E_{\text{chip13}} = \Delta E_{\text{chip26}}$

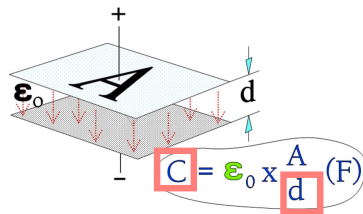
- $\Delta E_{\text{Type-A}} = \Delta E_{\text{Type-B}}$
- $\Delta E_{\text{chip13}} = \Delta E_{\text{chip12}} = \dots = \Delta E_{\text{chip1}}$
- $\Delta E_{\text{chip13}} = \Delta E_{\text{chip26}}$

$\Delta E_{\text{chip13}}^{\text{sPHENIX}} @ 50V \sim \Delta E_{\text{chip13}}^{\text{ELPH2021}} @ 50V, \Delta E_{\text{chip13}}^{\text{sPHENIX}} @ 100V \sim \Delta E_{\text{chip13}}^{\text{FNAL2019}} @ 100V ?$
To be studied by a **simulation** in advance.

Bias Voltage Scan

Bias Voltage Dependence

Cheng-Wei's slide 2022/4/15



$$\boxed{W} = \sqrt{2\epsilon(V + V_{bi})/Ne} = \sqrt{2\rho\mu\epsilon(V + V_{bi})}$$

d

$$\boxed{C} = \sqrt{\frac{\epsilon_0 \epsilon_r}{2\mu\rho|V|}} \cdot A$$

$$\frac{dE/dx \cdot \boxed{d}}{I_0} = \frac{3.87 \cdot 10^6 \text{ eV/cm} \cdot 0.03 \text{ cm}}{3.62 \text{ eV}} \approx \boxed{3.2 \cdot 10^4 \text{ e}^- \text{ h}^+ \text{ -pairs}}$$

Signal

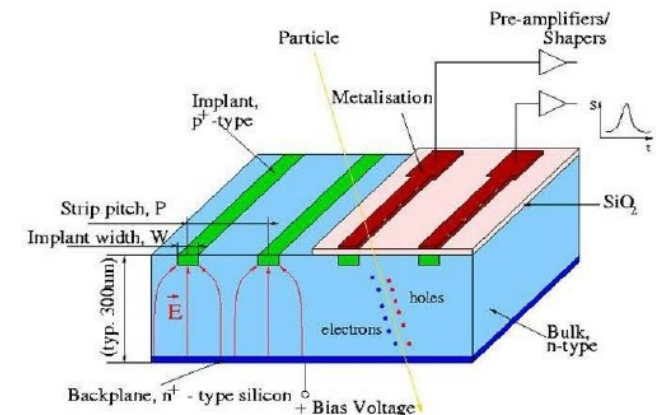
Based on the theory :

$$C \propto \frac{1}{d} \propto \frac{1}{\sqrt{V}} \propto \frac{1}{\text{signal}}$$

C : capacitance
d : the distance of the depletion region
V : supply bias voltage
signal : edep

Itaru's Slide 2022/06/22

Principles of operation



44

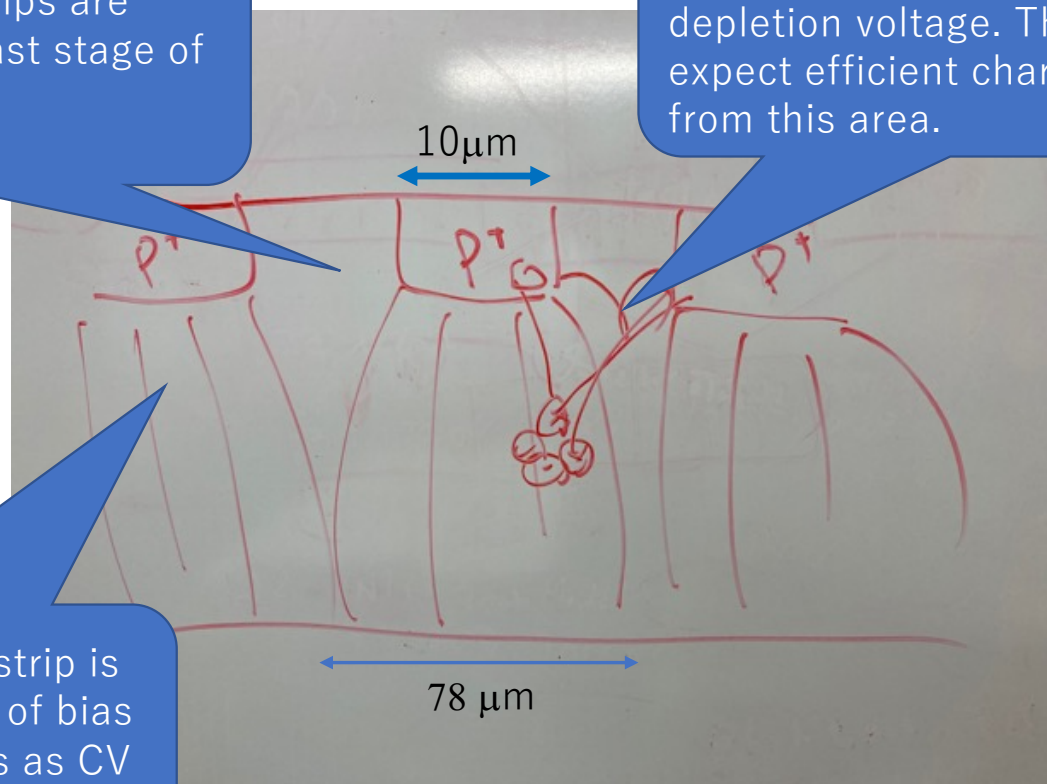
Electric field at non-fully depleted voltage

Electric field between strips are developed towards the last stage of fully depletion voltage.

This area between strips might not be depleted even slightly below the depletion voltage. Thus we cannot expect efficient charge collection from this area.

REALITY

The electric field just below strip is well developed as a function of bias voltage. This directly appears as CV response.

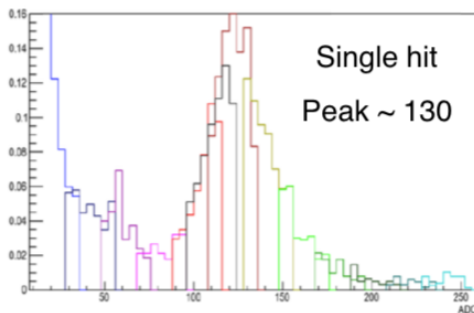


The best way to prove this hypothesis is to see the position dependence of the resolution within the strip width. We'll see a dip in the efficiency distribution around the edge of a strip.

Not sure if this is doable with cosmic ray...

Bias Voltage Scan Plan

- Importance: It is likely we end up with operating $<100V$ due to over current of some silicons.
- We need to know the collecting # of electrons below 100V.

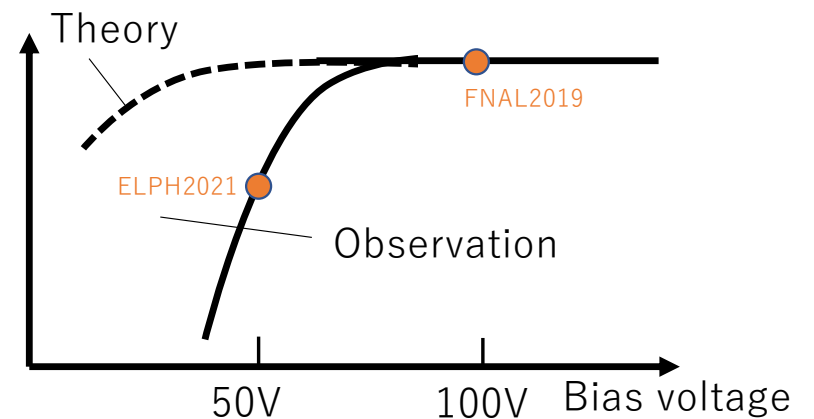


Scan	1	2	3	4	5	6	7	8
DAC0	8	28	48	68	88	108	128	148
1	12	32	52	72	92	112	132	152
2	16	36	56	76	96	116	136	156
3	20	40	60	80	100	120	140	160
4	24	44	64	84	104	124	144	164
5	28	48	68	88	108	128	148	168
6	32	52	72	92	112	132	152	172
7	36	56	76	96	116	136	156	176



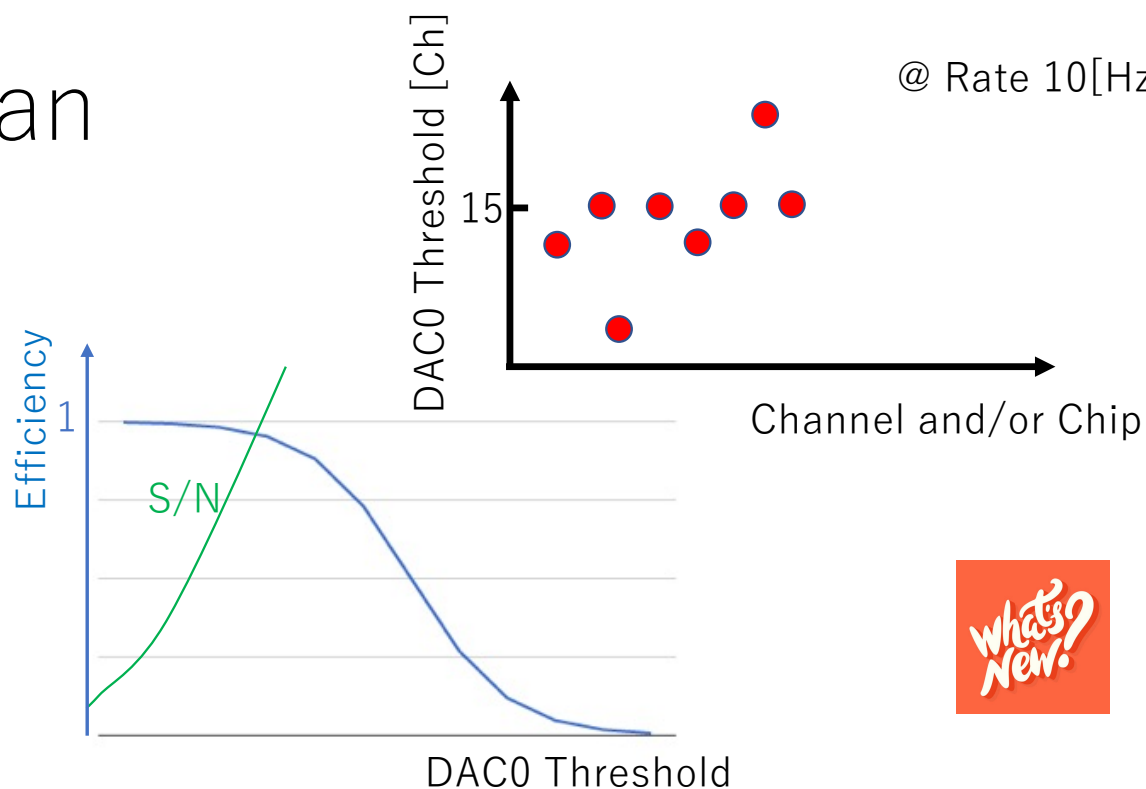
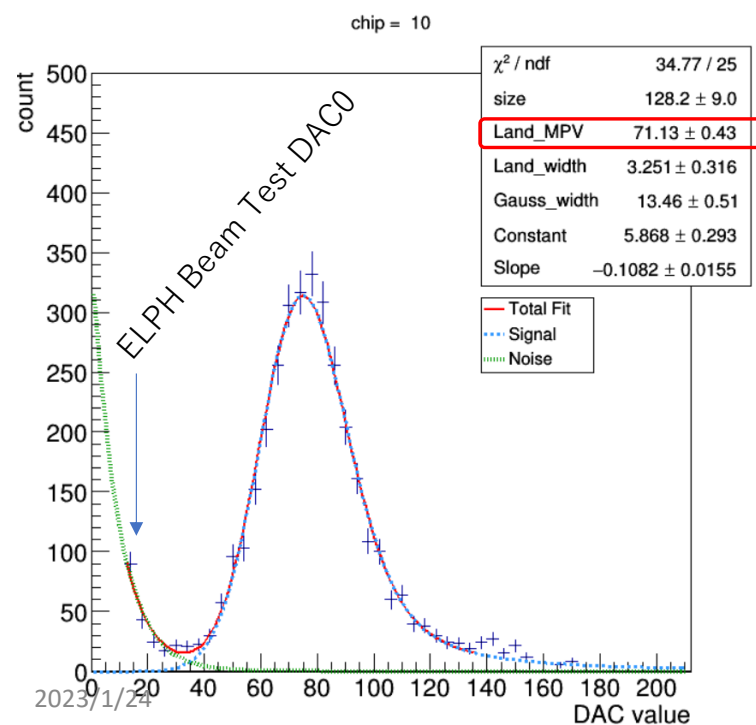
- Scan at 90V, 80V, 70V, 60V, 50V only around MIP region.
- Need immediate semi-online analysis (**DAC Scan code**) if data is satisfactory to cover MPV peak.
- The goal is to make the plot of **MPV vs. Bias voltage**.
- Not sure if we can run a simulation.

MPV vs Bias Voltage



DAC0 Threshold Scan

DAC0 Threshold Scan



DAC0	12	13	14	15	16	17	18
S/N							
Efficiency							

- The final DAC0 threshold is to be determined by the S/N. The philosophy is to keep the signal fraction as high as possible within the tolerable noise rate.

FPHX Operation

- FVTX Operating Condition

ROC: NEO Column: 0 Station: 0

Side 0 Side 1

Side 0 Chip Settings [Editable] Side 0 Controls

Vref	1	1	1	1	1	Vref	1
DAC 0	8	8	8	8	8	DAC 0	8
DAC 1	16	16	16	16	16	DAC 1	16
DAC 2	32	32	32	32	32	DAC 2	32
DAC 3	48	48	48	48	48	DAC 3	48
DAC 4	80	80	80	80	80	DAC 4	80
DAC 5	112	112	112	112	112	DAC 5	112
DAC 6	144	144	144	144	144	DAC 6	144
DAC 7	176	176	176	176	176	DAC 7	176
N1Sel	6	6	6	6	6	N1Sel	6
N2Sel	4	4	4	4	4	N2Sel	4
FB1Sel	4	4	4	4	4	FB1Sel	4
LeakSel	0	0	0	0	0	LeakSel	0
P3Sel	0	0	0	0	0	P3Sel	0
P2Sel	4	4	4	4	4	P2Sel	4
GSel	2	2	2	2	2	GSel	2
BWSel	4	4	4	4	4	BWSel	4
P1Sel	5	5	5	5	5	P1Sel	5
InjSel	0	0	0	0	0	InjSel	0
LVDS Current	7	7	7	7	7	LVDS Current	7
Accept Hits	☒	☒	☒	☒	☒	Accept Hits	☒
Global Inject	☐	☐	☐	☐	☐	Global Inject	☐
Serial Select	0 1	0 1	0 1	0 1	0 1	Serial Select	0 1
	0+1	0+1	0+1	0+1	0+1		0+1
Channel Mask	☐	☐	☐	☐	☐	Channel Mask	☐
	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5		
Revert Changes						Read Chips	
Update EEPROM						Write to Chips	
Wedge FFR							

FPHX Parameters

Name	Description	Default	FVTX	2021 Beam Test
Vref		1	1	1
DAC0		8	8	15
DAC1		16	16	30
DAC2		32	32	60
DAC3		48	48	90
DAC4		80	80	120
DAC5		112	112	150
DAC6		144	144	180
DAC7		176	176	210
N1Sel		6	6	6
N2Sel		4	4	4
FB1Sel		4	4	4
LeakSel		0	0	0
P3Sel		0	0	0
P2Sel		4	4	4
GSel	Gain Select	2	2	2
BWSel	Bandwidth Select	4	4	8
P1Sel		5	5	5
InjSel		0	0	0
LVDS Current [mA]		1	3	2

Reg	Desc	To Chip
*	Wild	0
1	Mask	0
2	Dig Ctrl	5
3	Vref	1
4	DAC0	20
5	DAC1	25
6	DAC2	30
7	DAC3	35
8	DAC4	40
9	DAC5	45
10	DAC6	50
11	DAC7	55
12	N1Sel <3:0>	6
	N2Sel <7:4>	4
13	FB1Sel <3:0>	4
	LeakSel <7:4>	0
14	P3Sel <1:0>	0
	P2Sel <7:4>	4
15	GSel <2:0>	2
	BWSel <7:3>	8
16	P1Sel <2:0>	5
	InjSel <5:3>	0
17	LVDS Current	3

Nevis GUI defaults
(Even from 2013)

4	DAC0	15	
5	DAC1	30	
6	DAC2	60	
7	DAC3	90	
8	DAC4	120	
9	DAC5	150	
10	DAC6	180	
11	DAC7	210	

Nevis GUI Defaults

All / D3 | Mod A0 | Mod B0 | Mod C0 | Mod D0 | Mod A1 | Mod B1 | Mod C1 | Mod D1 | Mod A2 | Mod B2 | Mod C2 | Mod D2 | Mod A3 | Mod B3 | Mod C3

Reg	Desc	To Chip	From Chip	Chip Command				
*	Wild	0		Read	Write	Set255	Reset	Default
1	Mask	0		Read	Write	Set255	Reset	Default
2	Dig Ctrl	5		Read	Write	Set255	Reset	Default
3	Vref	1		Read	Write	Set255	Reset	Default
4	DAC0	20		Read	Write	Set255	Reset	Default
5	DAC1	25		Read	Write	Set255	Reset	Default
6	DAC2	30		Read	Write	Set255	Reset	Default
7	DAC3	35		Read	Write	Set255	Reset	Default
8	DAC4	40		Read	Write	Set255	Reset	Default
9	DAC5	45		Read	Write	Set255	Reset	Default
10	DAC6	50		Read	Write	Set255	Reset	Default
11	DAC7	55		Read	Write	Set255	Reset	Default
12	N1Sel <3:0>	6		Read	Write	Set255	Reset	Default
	N2Sel <7:4>	4						
13	FB1Sel <3:0>	4		Read	Write	Set255	Reset	Default
	LeakSel <7:4>	0						
14	P3Sel <1:0>	0		Read	Write	Set255	Reset	Default
	P2Sel <7:4>	4						
15	GSel <2:0>	2		Read	Write	Set255	Reset	Default
	BWSel <7:3>	8						
16	P1Sel <2:0>	5		Read	Write	Set255	Reset	Default
	InjSel <5:3>	0						
17	LVDS Current	3		Read	Write	Set255	Reset	Default
18	Resets	n/a		Read	Write	Set255	Reset	Default

Chip Control

Display/Modify Configuration for Chip ID 21 Side 15

Channel Mask
[Red = Off, Green = On]

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127

Mask All | Unmask All | Toggle All | Send

Beam mask

Chip Side Enable

0	15	0	1	8	15	0	1	16	15	0	1	24	15	0	1
1	15	0	1	9	15	0	1	17	15	0	1	25	15	0	1
2	15	0	1	10	15	0	1	18	15	0	1	26	15	0	1
3	15	0	1	11	15	0	1	19	15	0	1	27	15	0	1
4	15	0	1	12	15	0	1	20	15	0	1	28	15	0	1
5	15	0	1	13	15	0	1	21	15	0	1	29	15	0	1
6	15	0	1	14	15	0	1	22	15	0	1	30	15	0	1
7	15	0	1	15	15	0	1	23	15	0	1	31	15	0	1

TestStand

☐ Spartan3
 ☐ ROC
 ☒ ROC+FEM
 FEM Addr 15

DB Access

☐ On
 ☒ Off

Global Chip/DAQ Operations

FFR	Enable RO	Latch FPGA	Core Reset	Start DAQ	Check GLINK	test
Init	Disable RO	Calib	JTAG Sync	Stop DAQ	Check FEM	Mask
FO Sync	Set L1	Delay 5	BCO Start	Global Start	Self Trig	DAC
FPGA RST	Er. EEPROM	Write Page	Read Page	Write All	Cosmic Start	Loop

3

DAQ Configuration

DAQ Program

C:/Users/RIKEN_INTT/C Browse

NI DAQ Sample Rate (MHz)

5

Num of events (0==inf)

0

Duration HH:MM:SS (0:00:00==inf)

HH:MM:SS

Print Output

Print Off

FPHX version (for Print)

2

Run Number

Filename

Beam Species

None

Beam Energy

0

Pulser Configuration

Pulse amplitude (10 bits max)

255

Config Amp

Pulse

Num of Pulses

1

Pulse Train

BCOs between pulses

1023

Wedge

0

Module

0

Set Module

Module Enable

Module 15	On	Off	Both	Side 0	Side 1	Module 7	On	Off	Both	Side 0	Side 1
Module 0	On	Off	Both	Side 0	Side 1	Module 8	On	Off	Both	Side 0	Side 1
Module 1	On	Off	Both	Side 0	Side 1	Module 9	On	Off	Both	Side 0	Side 1
Module 2	On	Off	Both	Side 0	Side 1	Module 10	On	Off	Both	Side 0	Side 1
Module 3	On	Off	Both	Side 0	Side 1	Module 11	On	Off	Both	Side 0	Side 1
Module 4	On	Off	Both	Side 0	Side 1	Module 12	On	Off	Both	Side 0	Side 1
Module 5	On	Off	Both	Side 0	Side 1	Module 13	On	Off	Both	Side 0	Side 1
Module 6	On	Off	Both	Side 0	Side 1	Module 14	On	Off	Both	Side 0	Side 1

Manual Packet Send

Packet file to send

Browse

Send

Read

Communications

☒ USB
 ☐ None
 ☐ Ethernet IP Addr 192.168.60.2 Port 9900

Baud Rate

115200

ver7

ROOT

Module ID

6

Calib

External

camac

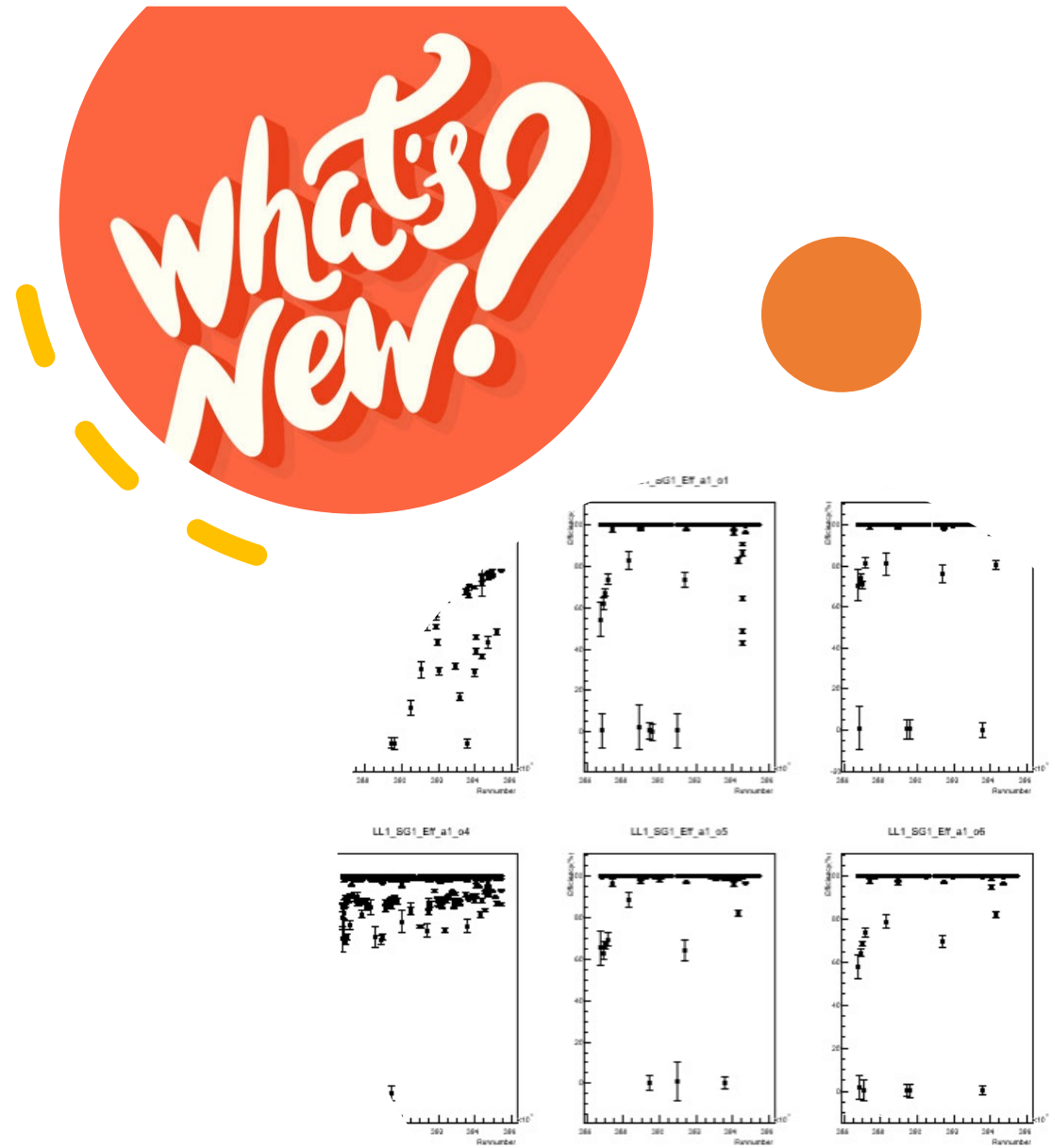
ROOT_trig

Monitoring (Advices from previous discussion)

1. Define online monitor. Develop and test anomaly (dead/hot channel) checker.
2. Establish flushing anomaly checker results to database.

Stability Monitor

- Normalized hit rates/Chip, ADC peak position, S/N, etc. are again, textualized (part of online monitor?) and be saved in the calibration database.
- Then we should develop the stability monitor by plotting above key performance parameters as a function of time.

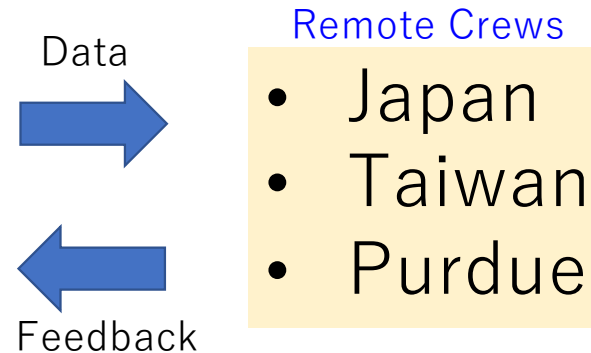


Manpower operation during commissioning

Onsite Crews

- Rachid
- Genki
- Maya
- Itaru : Feb. 20th –
- Cheng-Wei : March 2nd -
- Joseph : Middle of Feb –
- Jaein : March 1st -
- Else?

Hardware debugging, data taking,
change setting, logging incidents,...



Analysis



- Once we have a beam, the data taking is 24 hours.
- As long as we have a plan, we'll continue data taking with the INTT standalone DAQ independently from other subsystem data taking.
- The hall access will be coordinated with other subsystems.
- We will be blind immediately without the analysis code and cannot move forward!

Summary

- Various analyses and display codes are required for each measurement in commissioning. **Need to prepare all necessary codes in advance!!**
- Depending on the results, the INTT operating parameters are determined and the next measurement is made, so results are required immediately. Compared to single ladder analysis, the number of channels and the amount of data are overwhelmingly large.
- Data analysis is not an amount that can be handled on-site. Need feedback from remote analysis crews.
- Since we cannot have every INTT team members to be on-site, the commissioning program is designed to analyze the data remotely and provide feedback to the on-site.
- Volunteers are always welcome!

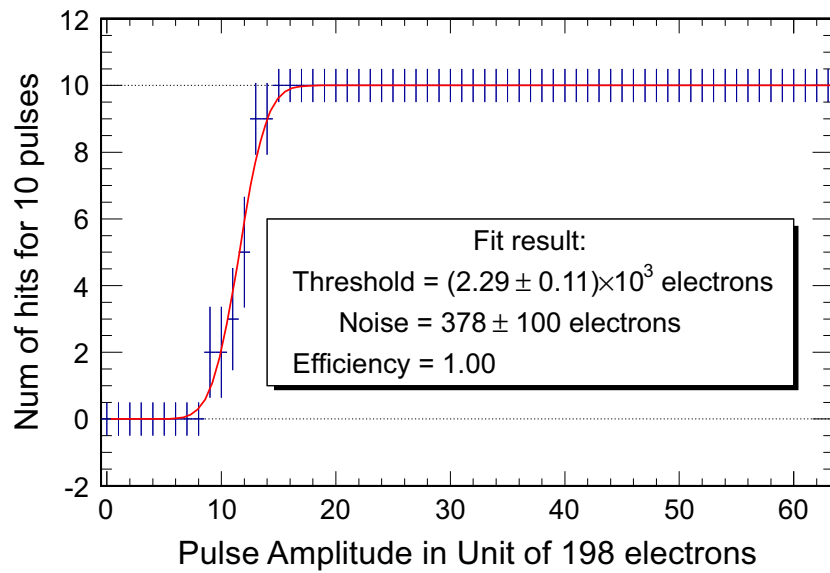


Fig. 35. Typical calibration data for a single channel (data points), fit with a normal cumulative distribution function.

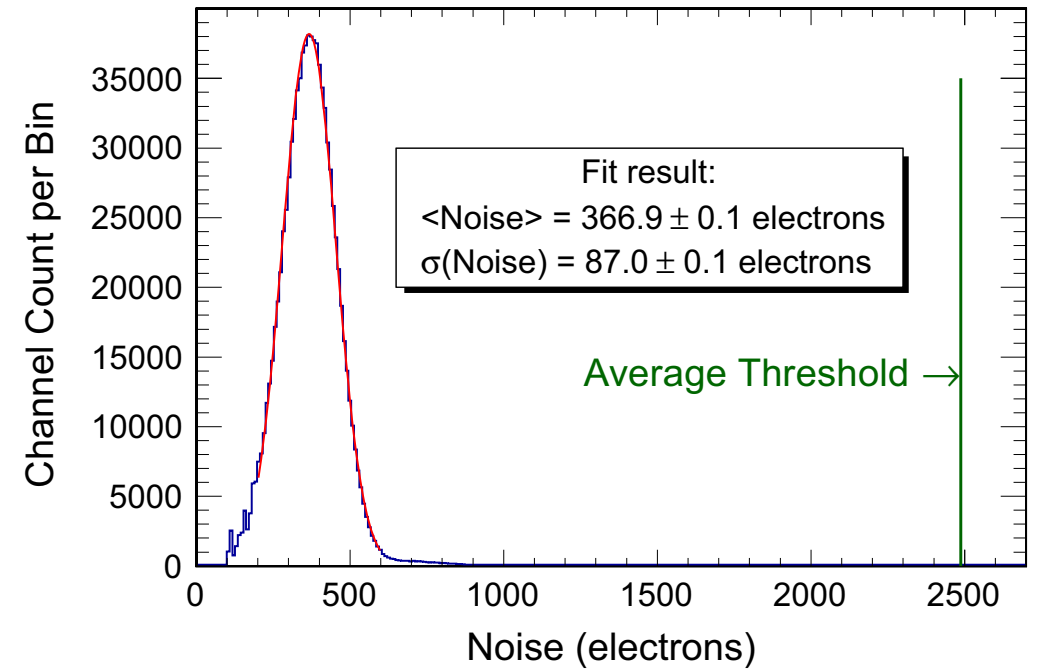


Fig. 36. Histogram of the noise parameter, σ , for all channels under operating conditions, in a typical calibration run. A Gaussian distribution fit to the data gives a mean noise level of 367 electrons. The nominal discriminator threshold at ~ 2500 electrons is shown by the vertical line.