

Update on ePIC powering and associated services estimates

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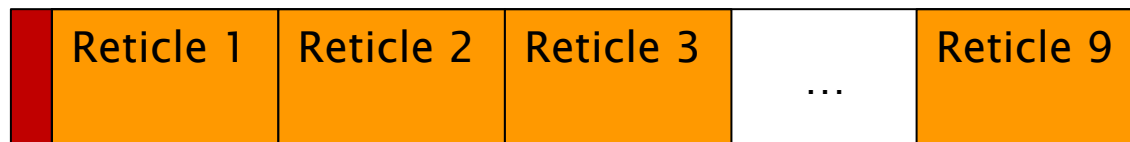
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Supporting material

- EIC SC ePIC SVT baseline configuration v0.0.
 - Released on 7 November 2022 as a starting point for eRD104/111/113 work.
 - <https://indico.bnl.gov/event/17713/>
- First version of services estimate, discussed with the project.
 - https://brookhavenlab.sharepoint.com/:b:/s/eRHIC/bnl&slac/experimental%20equipment/ETpXbQLIIGRFhUpan91DhtgBsRnBFDDW_DC11rRhzy0FQ?e=fLldcg
- Initial ideas on serial powering presented on 30 January 2023 at the EIC SC general meeting.
 - <https://indico.bnl.gov/event/18202/>
- Remember: the trick to design a low mass powering scheme is to **transmit power at low current and high voltage.**

Sensor design (quick reminder)

- The ePIC sensor will be a MAPS sensor in 65 nm technology.
 - A MAPS sensor contains sensor and readout chip functionality in one piece of silicon.
- Each sensor will be made of a row of stitched reticles plus one periphery.
 - Each reticle is identical and contains sensor and electronics functionality.
 - The reticles are electrically stitched along the length to form the pixel matrix.
 - Currently, for the ePIC SVT we foresee sensors made of rows of up to 9 reticles.
 - At one end of the stitched row, there is the periphery containing circuits for data transmission, power distribution, biasing, etc.



- Each sensor needs:
 - **Low voltage** (1.2V) to power the electronics.
 - **Bias voltage** (4-6V) to deplete the sensor substrate.

Sensor LV power estimate

- Initial ITS3 sensor specifications give 20 mW/cm^2 .
 - This number is given in the ITS3 Letter of Intent CERN-LHCC-2019-018 / LHCC-I-034 (01/12/2019).
 - We understand this to include the periphery and to be for 1×9 stitched reticles.
- Note that this power density is not uniform across the sensor.
 - The pixel matrix will consume very little power compared to the periphery.
- Size of a 1×9 sensor = $\sim 53 \text{ cm}^2$.
 - Reticle width = 18.85 mm, length = 30 mm.
 - Periphery width = 18.85 mm, length = 10 mm.
- **Power per sensor = $\sim 1 \text{ W}$.**
 - As most power is consumed in the periphery, the current assumption is that the power does not scale with the number of reticles.
- **Sensor voltage = 1.2 V.**
 - Defined by the technology node.
- **Sensor current = $1 \text{ W} / 1.2 \text{ V} = \sim 0.85 \text{ A}$.**

LV power cables count

- The initial conservative estimate assumed direct powering, with cables for analogue and digital power, plus return.
- Discussion with the project highlighted the need to make an estimate based on a more realistic powering scheme.
- The initial estimate is thus updated considering a serial powering scheme.
- Based on the initial SP concept presented in January, serial powering chains for the **sagitta layers** are assumed to be made of:
 - **Two** sensors in L3.
 - **Four** sensors in L4.
- An initial serial powering configuration still needs to be worked out for the **disks**. For now, let's assume **chains of 3 sensors**.

LV power cables count

- For the **vertex layers**, it is prudent to assume **smaller chains (2 sensors)** for the time being, while evaluation of scheme robustness and redundancy progress.
 - Longer chains increase the risk of losing a significant portion of the layer if case of problems on one sensor.
- **Each SP chain will get one cable + return delivering the total current for one sensor, 0.85 A.**
 - The split between analogue and digital current, and voltage generation, will be done on the sensor by the Shunt-LDO regulator(s).

LV power cables count

- Number of cables carrying 0.85 A.

	L0, L1, L2	L3, L4	BWD disks	FWD disks
LV	34	256	216	216
LV return	34	256	216	216

- Previous estimate

	L0, L1, L2	L3, L4	BWD disks	FWD disks
LV digital	68	824	648	648
LV analogue	68	824	648	648
LV return	68	824	648	648

- Remember that
 - L0, L1, L2 (vertex layers) services come out in the hadron direction.
 - L3, L4 services come out on both sides (half on each side).

LV power count

- In the previous estimate we had also done a different calculation of number of sensors to **account for the uncertainty on the yield**. We had assumed **sensors made of an average of four reticles**.
 - In discussion with the project we decided not to use this one.
- In this case, the number of cables carrying 0.85 A is

	L0, L1, L2	L3, L4	BWD disks	FWD disks
LV	77	498	367	367
LV return	77	498	367	367

- Previous estimate

	L0, L1, L2	L3, L4	BWD disks	FWD disks
LV digital	153	1542	1100	1100
LV analogue	153	1542	1100	1100
LV return	153	1542	1100	1100

LV power cable cross section

- Cables should be assumed to be **aluminium** not copper.
- Not sure how to define the cable cross section.
 - Check ATLAS and CMS schemes; **discuss with project engineers.**
- Total V_{drop} on cables constrained by:
 - Current source output voltage capability \rightarrow unknown.
 - Allowed power density, i.e. heat \rightarrow unknown.

Serial powering basics

- As the modules are powered with a constant current, V_{drop} is not constrained as in a voltage based powering scheme.
 - It can in principle be chosen only depending on the output voltage capability of the current source and of the allowed power density (i.e. cooling capability).
- Higher V_{drop} can be allowed in the active area of the detector to reduce the material budget of the cables.
 - Outside the detector the voltage drop can be reduced to lower the power losses.
- With respect to voltage based powering schemes (incl. DC-DC), serial powering allows more flexibility in the optimization of material and power efficiency.

The diagram illustrates two power distribution schemes. The top diagram, labeled 'Direct powering', shows a current source I connected to a resistor RnI^2 and a series of modules (Mod 1, Mod 2, ..., Mod n). The bottom diagram, labeled 'Serial powering', shows a current source I connected to a resistor RI^2 and a series of regulators (Regulator) connected to modules (Mod 1, Mod 2, ..., Mod n).

L. Gonella | ePIC SVT powering | EIC SC meeting - 19 Dec 2022

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Sensor bias voltage

- The sensor bias voltage will be around 4 – 6 V.
- The current for sensor bias is very low → **cables with small cross section.**
- For now we assume that **each sensor will receive the sensor bias independently**, with its own set a cables (bias + return).
- **Alternative sensor bias schemes** will be looked into but require **R&D** to find possible solutions.
 - As each sensor in the chain has a different ground, it is not possible to have group of sensors sharing the same HV line + return.
 - This only works for sensors where there the headroom between operational voltage and breakdown is larger then the total voltage drop in the chain.
 - i.e. planar sensors biased with 100s V.
 - This is not the case for MAPS.
 - Check ATLAS and CMS schemes, especially for 3D sensors.

DC-DC conversion

- Power is transmitted at low current and high voltage only until the DC-DC converter → Unless the converter is placed close to the sensor, we will get the full current in active area (i.e. high material).
- The converters are too much material to be placed close to the sensors. Putting them further away, on the support cone, only partially solves the material problem (i.e. upstream of the converter).
 - And could add spots of high material in front of other detectors.
- **This option is currently not considered for the ePIC SVT** (i.e. not followed up in the eRD104 R&D).
 - Also note that ATLAS and CMS did not use this scheme for their upgraded pixel detectors at the HL-LHC because of material.
 - DC-DC conversion is used in the ATLAS and CMS strip detectors (lower power, further from IP), and it is placed on the module.

Reminder of the known unknowns

- The **reticle size** is assumed to be 18.85 mm x 30 mm, but it is not the final size yet.
 - The reticle size will be better defined during the ITS3 ER2 design, i.e. some time this year.
- The **stitching yield** is still unknown. Depending on the result, we might have more, shorter sensors.
 - Yield estimates should be known some time this year.
- The **sensor LV power** is an estimate and will certainly change (possibly **increase**).
- The overall **SVT layout** might still change, especially in the BWD/FWD regions.
- **SP chains could be longer**. To be further assessed as SP scheme details are worked out and redundancy options understood and implemented, and in collaboration with the project as routing space and needs evolve.
- **Formal establishment of the collaboration with ITS3** is fundamental to work on any powering scheme for ePIC.

Shunt-LDO configuration per sensor

- As discussed in January, we would like to use the **Shunt-LDO regulator**, that has been developed specifically for SP by ATLAS and CMS.
- The sensor will have **multiple power domains** to allow switching off parts of one reticle to improve yield of large area stitched sensors.
- Different regulator configurations are possible. First ideas are:
 - One Shunt-LDO regulator per power domain.
 - One Shunt-LDO plus one switch for power domain.
- Shunt-LDO specifications are being worked on for a first prototype design in 65nm.
- A discussion with RD53 Shunt-LDO designer planned for next week.

Conclusion

- Work on serial powering proceeds on various aspects:
 - Sensor power consumption estimate defined.
 - Regulator specifications being drafted for different configurations on the sensor.
 - Design of bandgap circuit for Shunt-LDO ongoing.
 - LV cables number updated with respect to initial estimate.
- Next steps:
 - Discuss Shunt-LDO regulator design with RD53 designer.
 - Finalise, review and approve prototype Shunt-LDO specifications to start design.
 - Define initial SP concept for disks.
 - Discuss LV cable cross section with project engineers.
 - Brainstorming on sensor bias options.
 - Look into ATLAS and CMS SP schemes.

Back up
