EICROC/HGCROC evaluation for HPPD/MCP status and plans

F. Bouyjou, E. Delagnes, JJ Dormard, F. Dulucq, M. Firlej, T. Fiutowski, J. Gonzalez, F. Guilloux, M. Idzik, C. de La Taille, J. Moron, D. Marchand, C. Munoz, M. Morenas, N. Seguin-Moreau, L. Serin, K. Swientek, D. Thienpont

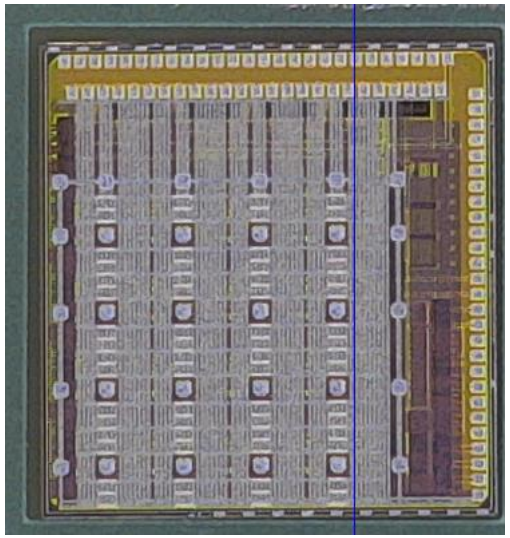
6 mar 2023

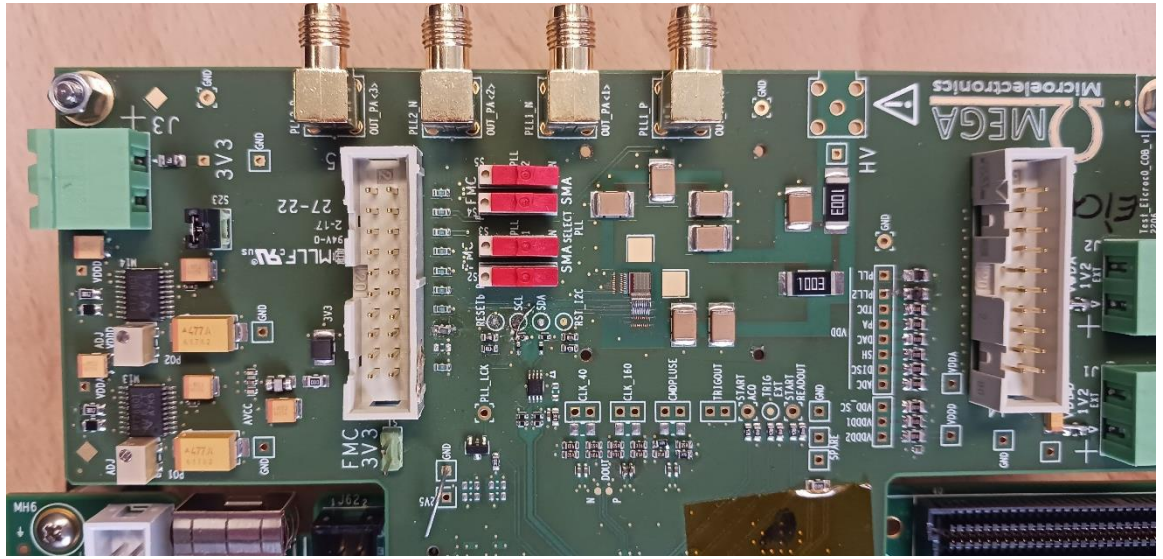
outline

- OMEGA Chips for timing measurements @EIC
  - EICROC0 : 16ch AC LGAD readout derived from ATLAS ALTIROC
  - HGCROC3 : 72ch Si diode readout with timing capability used by CMS HGCAL
- Comparison EICROC/HGCROC for HRPPD
- Next steps for EICROC/HGCROC
- Conclusion

EICROC0 overview

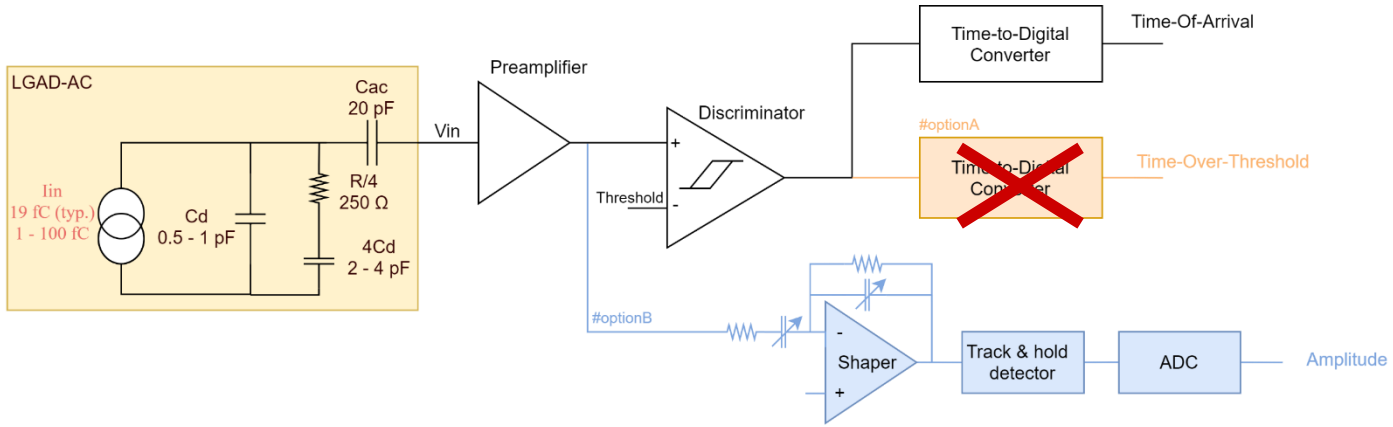
- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 um pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now under test at IJCLAB and OMEGA.

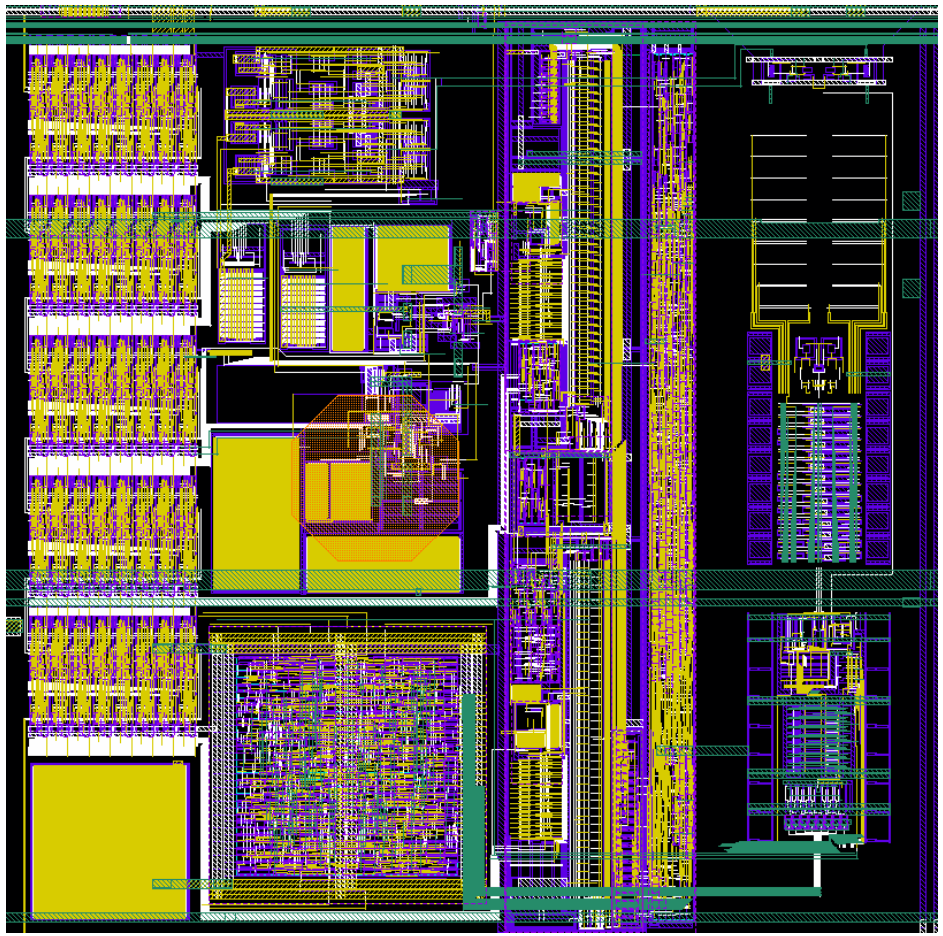




EICROC0 : one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes

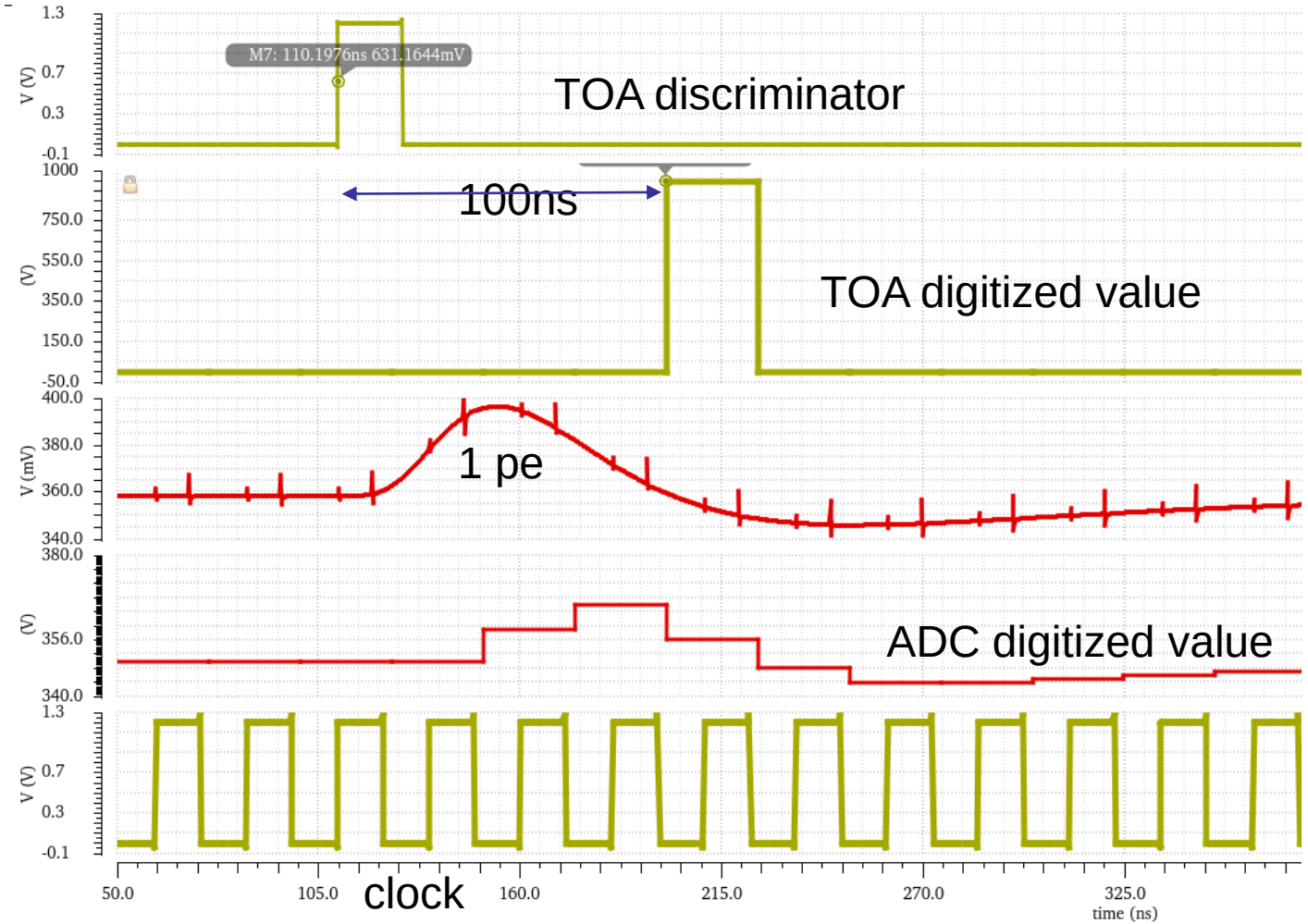




Slow control | PA +discri | TOA TDC | 8b 40M ADC

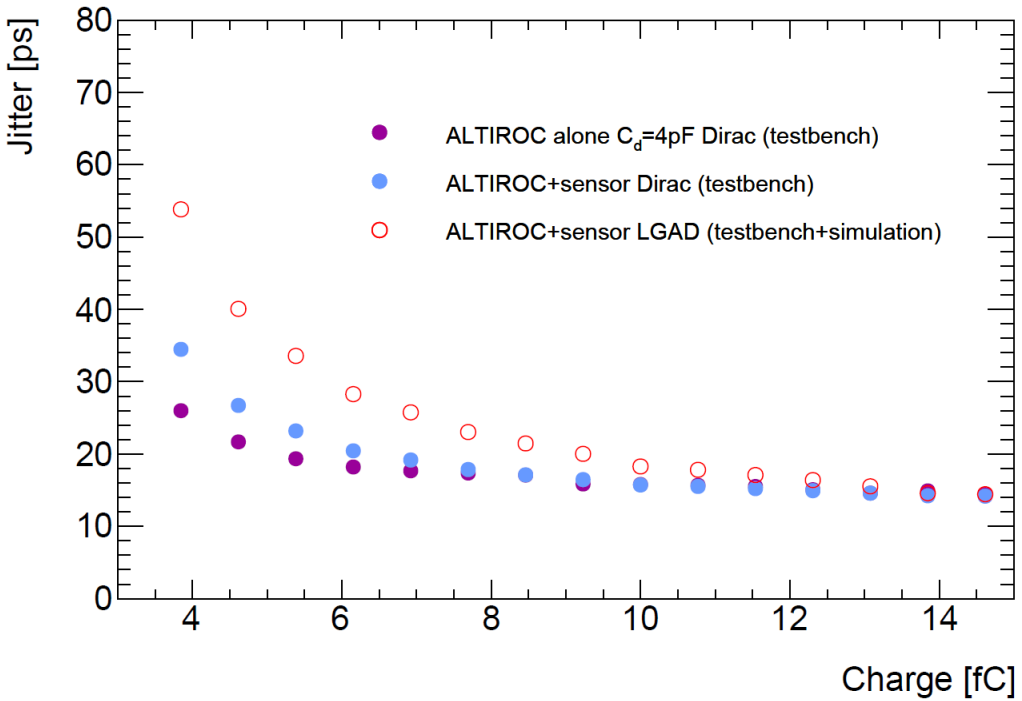
Simulated waveforms

- Illustration from another (similar) chip (HKROC)



expected performance (derived from ALTIROC1 HGTD)

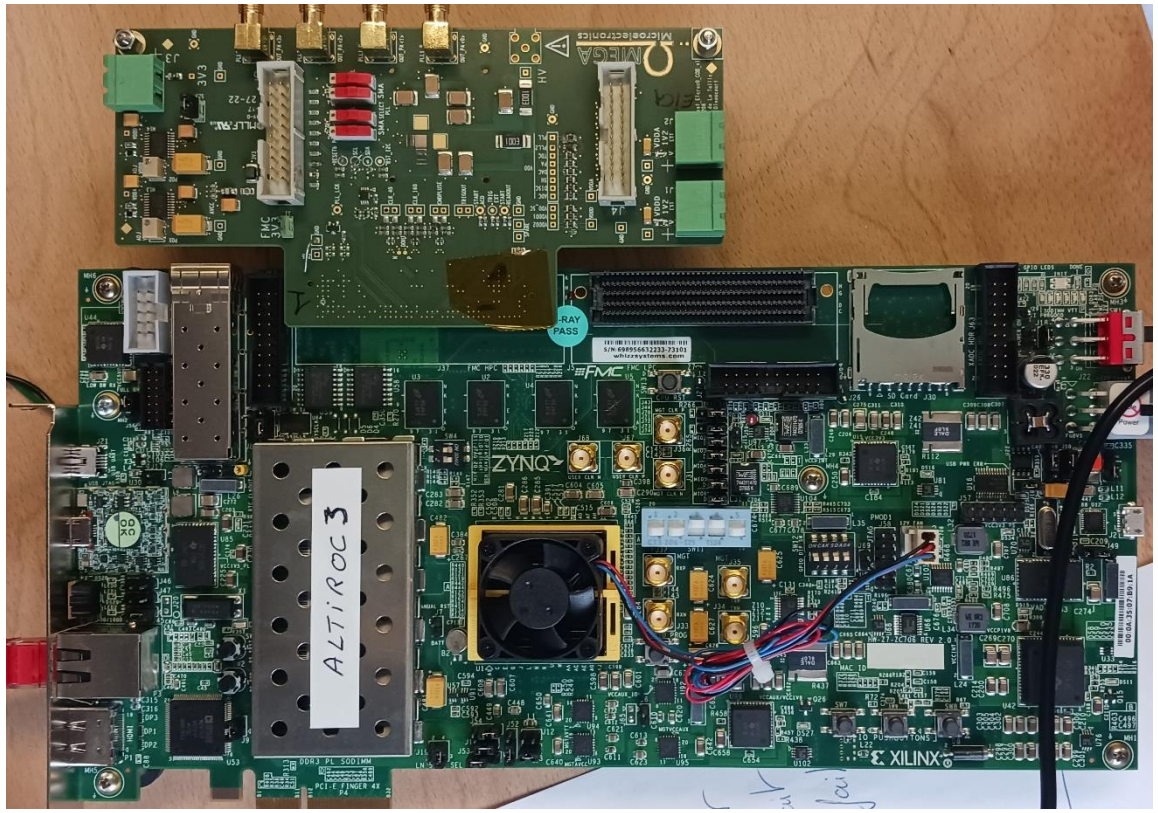
- Altiroc1 prototypes since 2018 , 25 channels (Preamp + discri + TOA and TDC TDS + SRAM) to validate front-end since 2017
  - TDC performance validated
  - TOA jitter performance validated
  - TOT performance : validated with ASIC alone, but still some concern when connected to sensor + HV connection
  - Phase shifter & PLL performance validated
- Altiroc1 bump bonded onto sensors: Very useful to understand system an integration issues

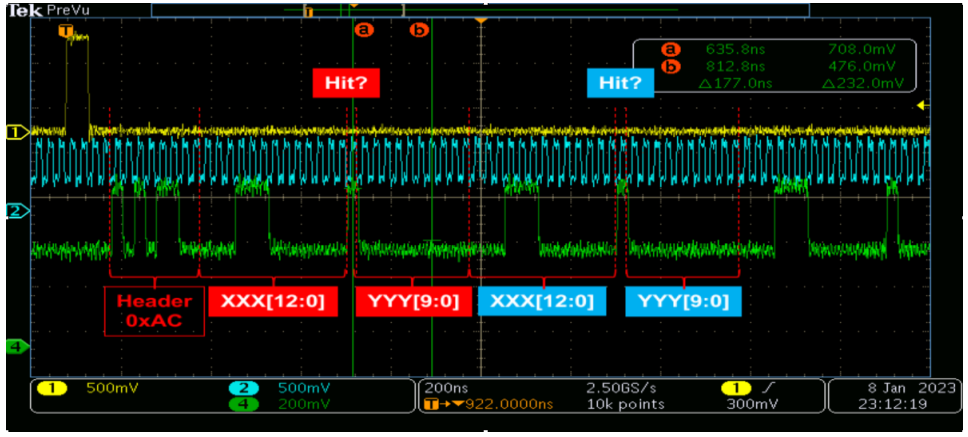


< 20 ps for Q > 6 fC dominated by clock/TDC/calib command
< 40 ps at Q=4 fC start to be dominated by noise

EICROC0 status

- Testboard up and running
  - Firmware and software from IJCLAB
  - Configuration OK
  - Lost a bit of time to send the testpulse…
  - Preamp, discri signals observed
  - Data coming out as expected
  - Still trying to find time to understand the data…





HGCROC3 overview

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

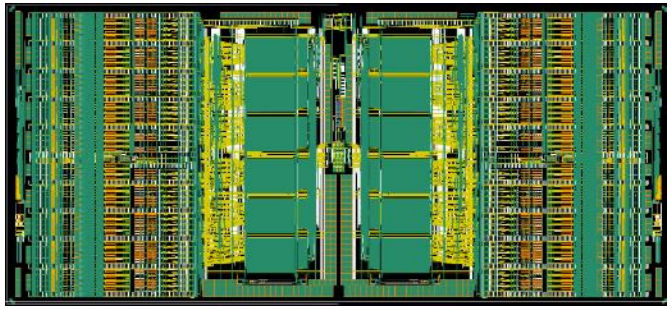
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

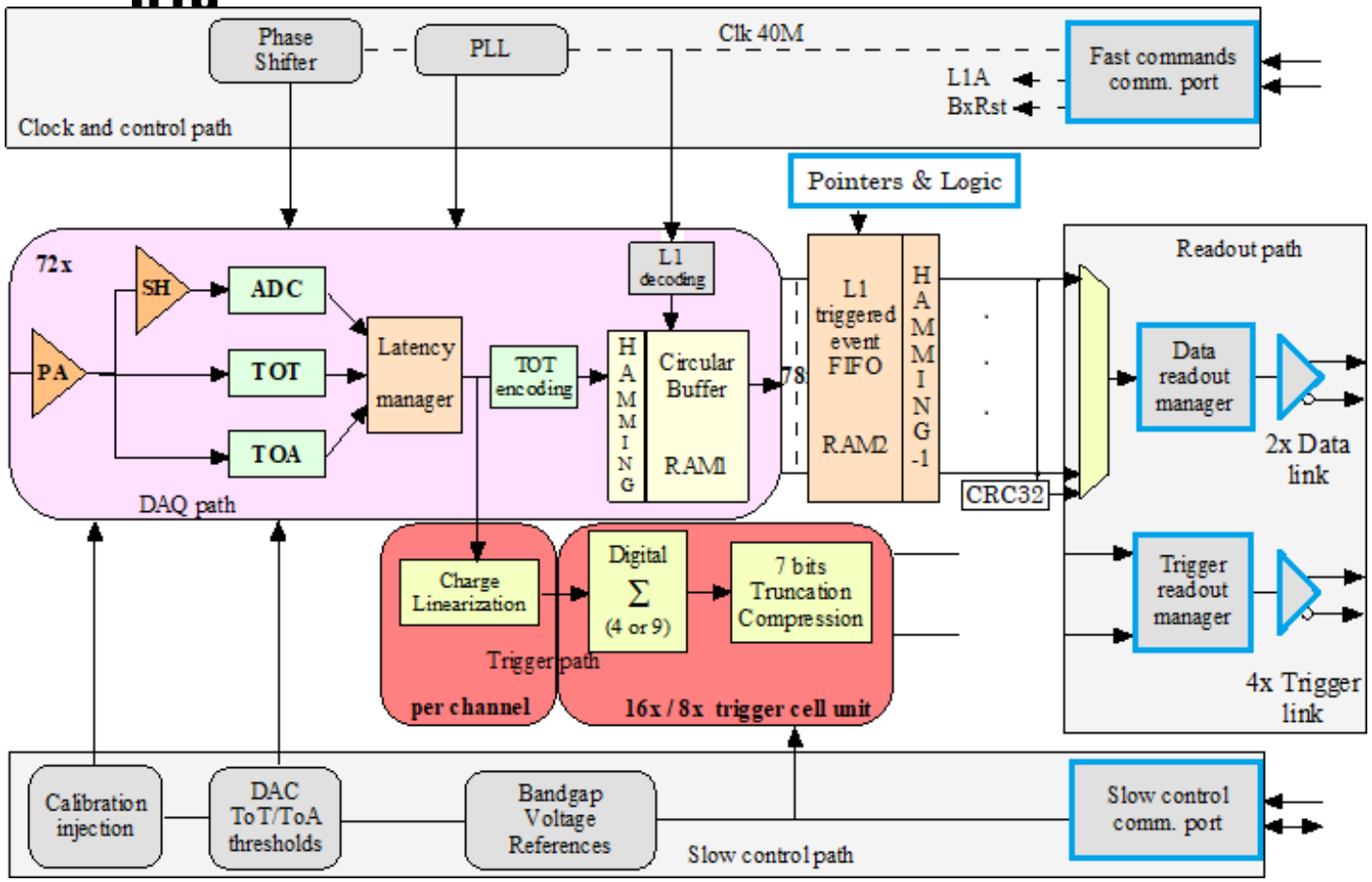
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain





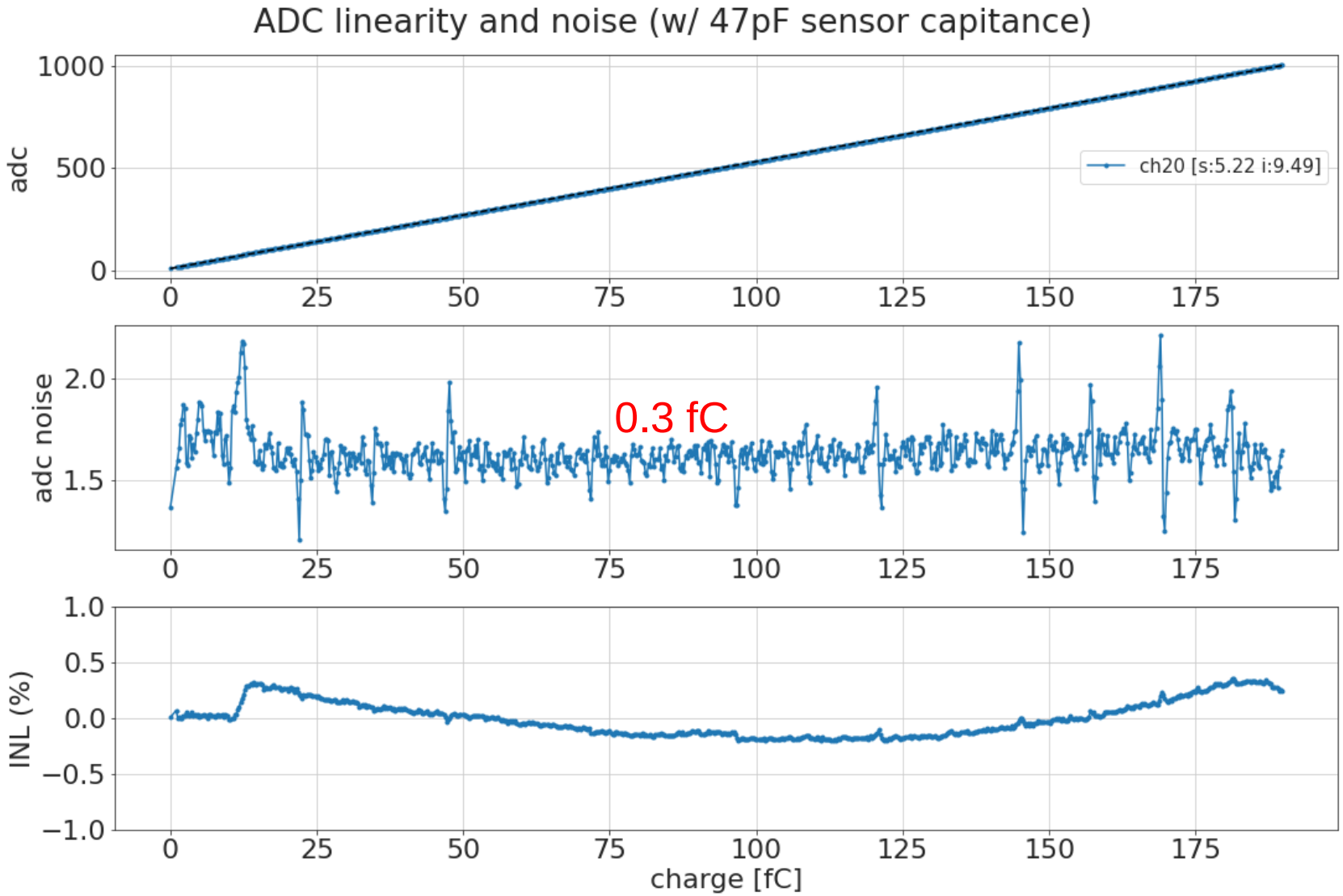
ROCv3: Charge measurements (ADC range)

- Injection and readout with the full readout chain enabled
- Internal injection with calibration DAC (low 1,5 fC offset)
- ADC noise ~0.3 fC resolution

(1.6 ADCu)

- Good linearity within +/- 0.5%

1.6 fC (~1 MIP) linearity for the typical gain

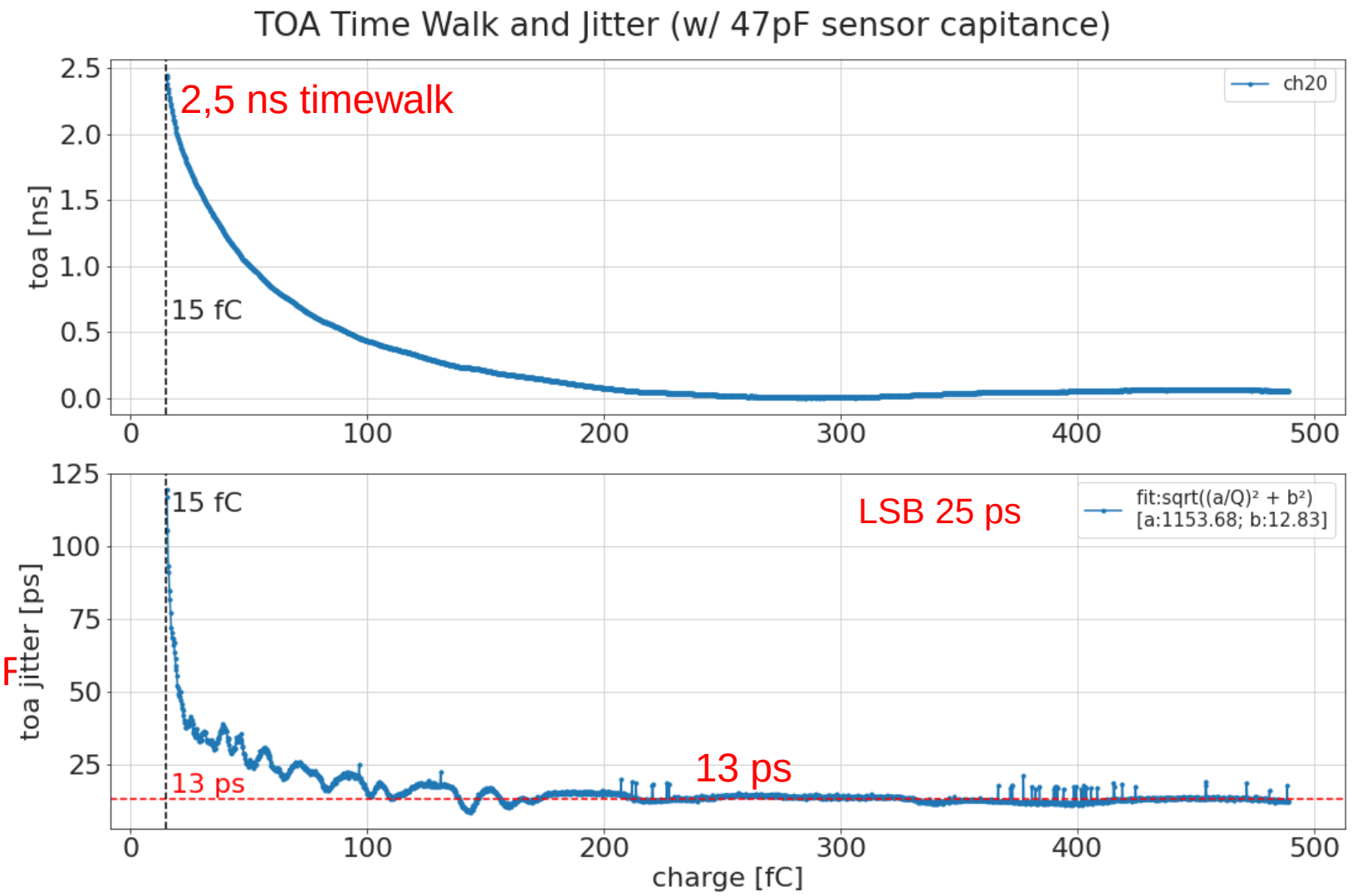


ROCv3: Timing measurements (TOA)

- The TDC has been improved to properly reconstruct the timing (also new layout) and to cope with outliers
- Minimum threshold set to 15 fC

(20 fC for ROCv2)

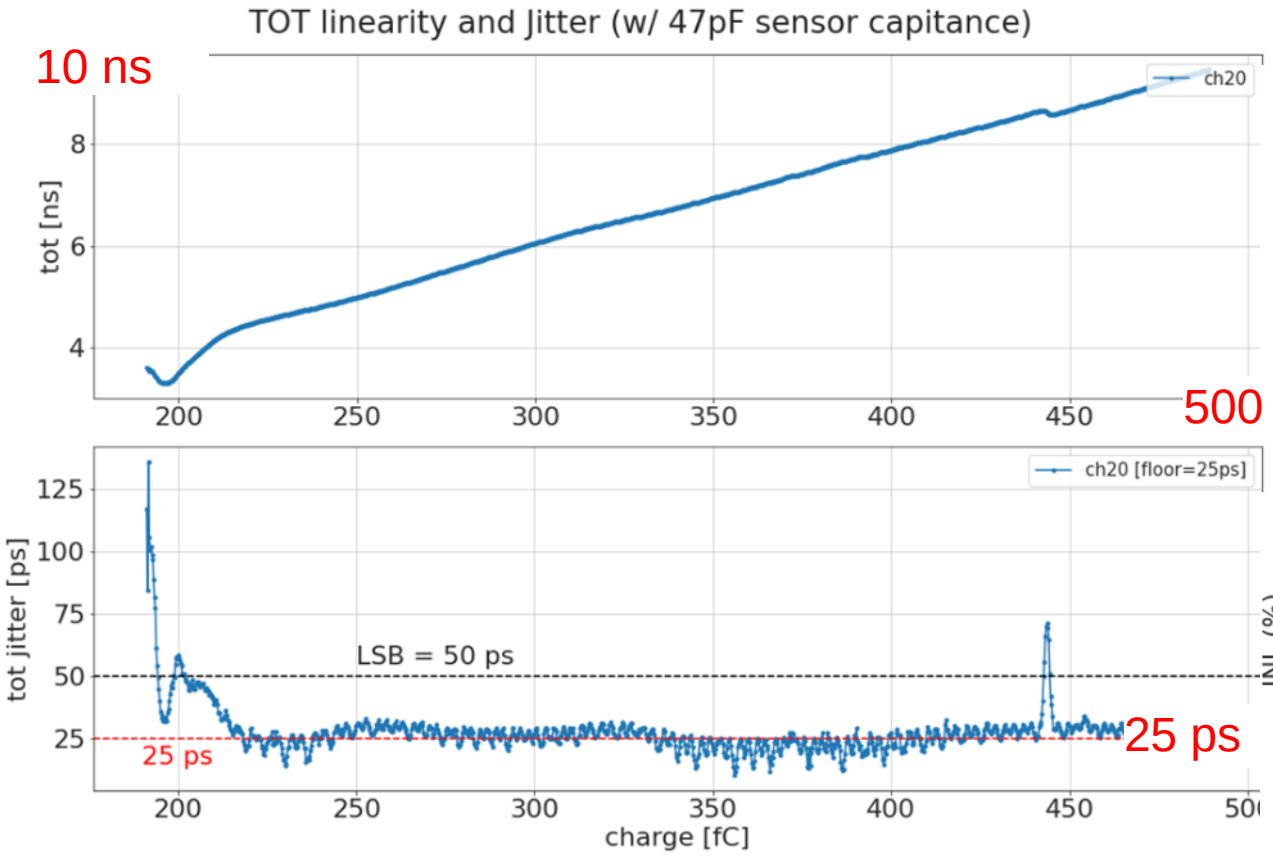
- The measured jitter floor is about 13 ps (25 ps for ROCv2)
- Should be even better with Cd=5-10pF
  - To be measured for HRPPD

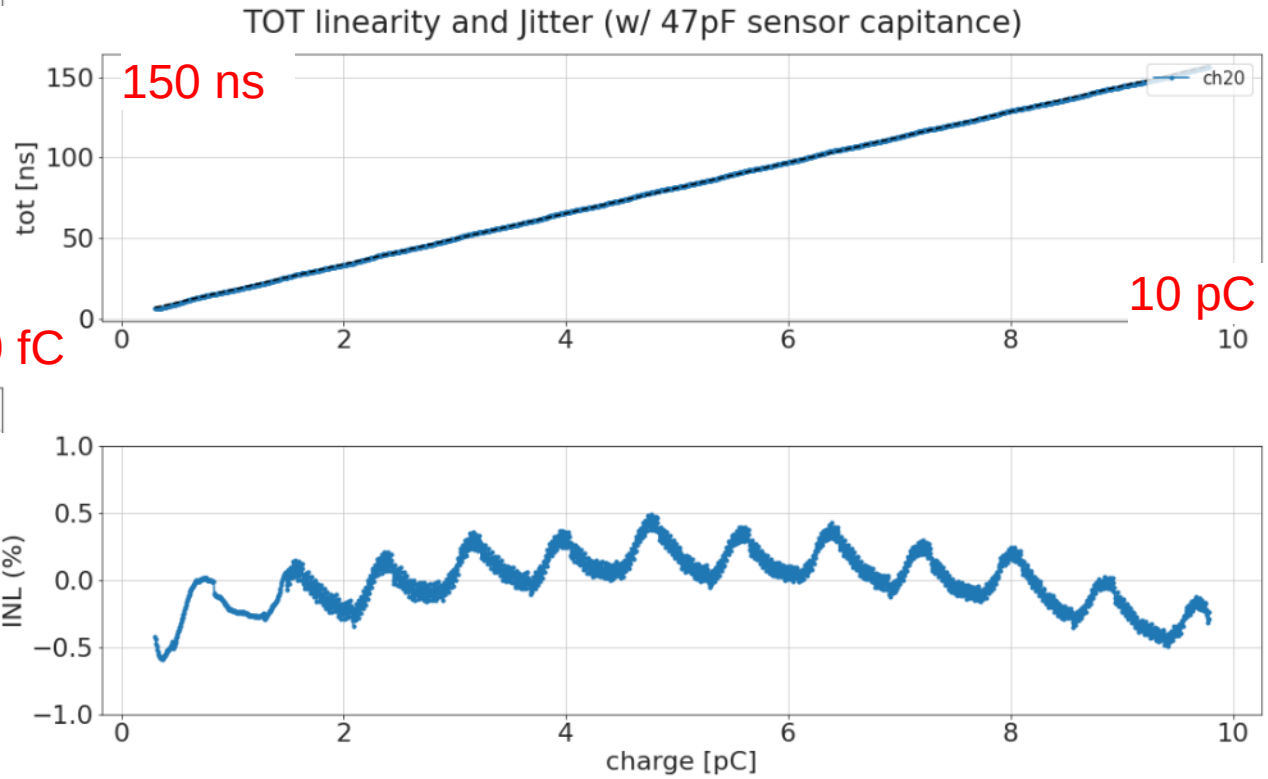


ROCv3: Time over Threshold measuremenst (TOT)

Charge measurement from TOT when preamplifier saturates (max 200 ns)

- 160 fC to 10 pC (for the typical preamplifier gain) with 12-bits TDC (LSB 50ps)
- Linearity < 1% linearity to be confirmed (2% in ROCv2)
- Resolution around 25 ps (50 ps in ROCv2)





Compared performance

HGCROC3 (2020)

- 72 channels fpBGA
- Sensor : Si Cd~50 pF
- Dyn range 0.3 fC to 10 pC
- Noise : 0.3 fC @ Cd=50 pF tp=20 ns
- TOA Min threshold ~20 fC
- Time walk ~2 ns (Cd=50 pF)
- Jitter ~1.5ns/Q(fC) (Cd=50 pF)
- Pd = 15 mW/ch

EICROC0 (2022)

Not yet measured, values fm ALTIROC

- 16 channels COB
- Sensor : AC LGAD Cd~1 pF
- Dyn range 0.3 fC to 100 fC
- Noise : 0.3 fC
- TOA Min threshold ~4 fC (Cd=4 pF)
- Time walk ~0.7 ns (Cd=4 pF)
- Jitter ~100 ps/Q(fC) (Cd=4 pF)
- Pd = 3 mW/ch

Next steps

- EICROC1 : larger chip to study floorplanning and EIC backend
  - Probably with variants of columns to study different low-power front-end and digitization
  - Target 1 mW/ch (lower power ADC)
  - Study clock adaptation to EIC (100 MHz input)
  - Size tbd (probably 8x4 or 16x4) unlikely to have final size 16x16 before end 2024

- HGCROC4 (4EIC!) : adapt to EIC R/O and DAQ
  - Possibly slower shaping and ADC to reduce power : target ~5 mW/ch
  - EIC clock 100 MHz
  - Auto-trigger

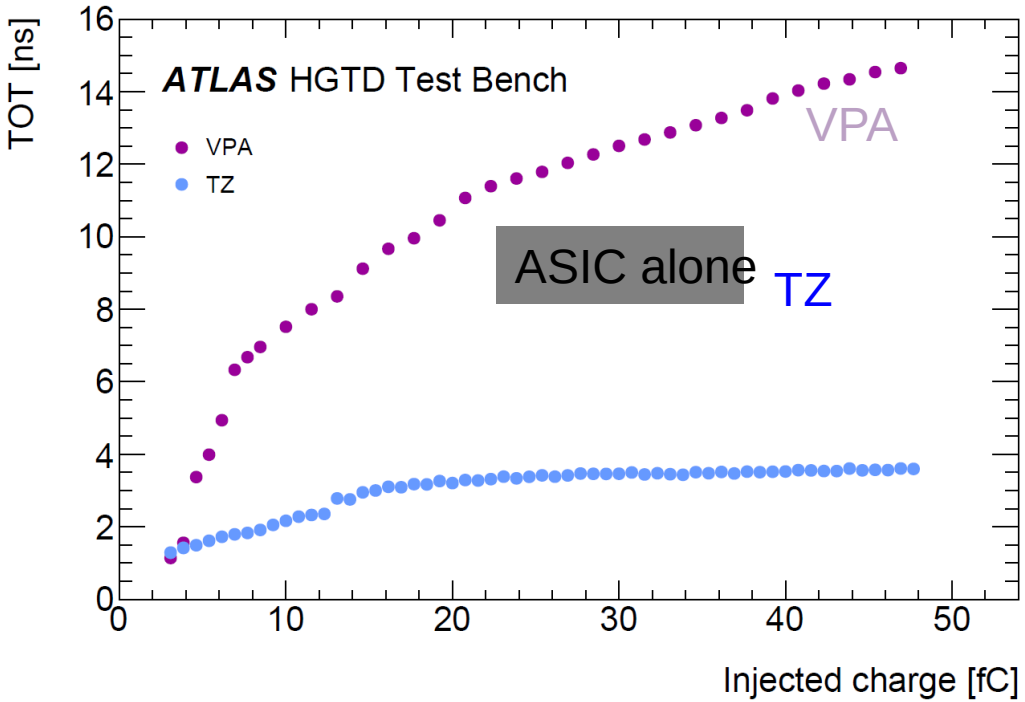
Conclusion

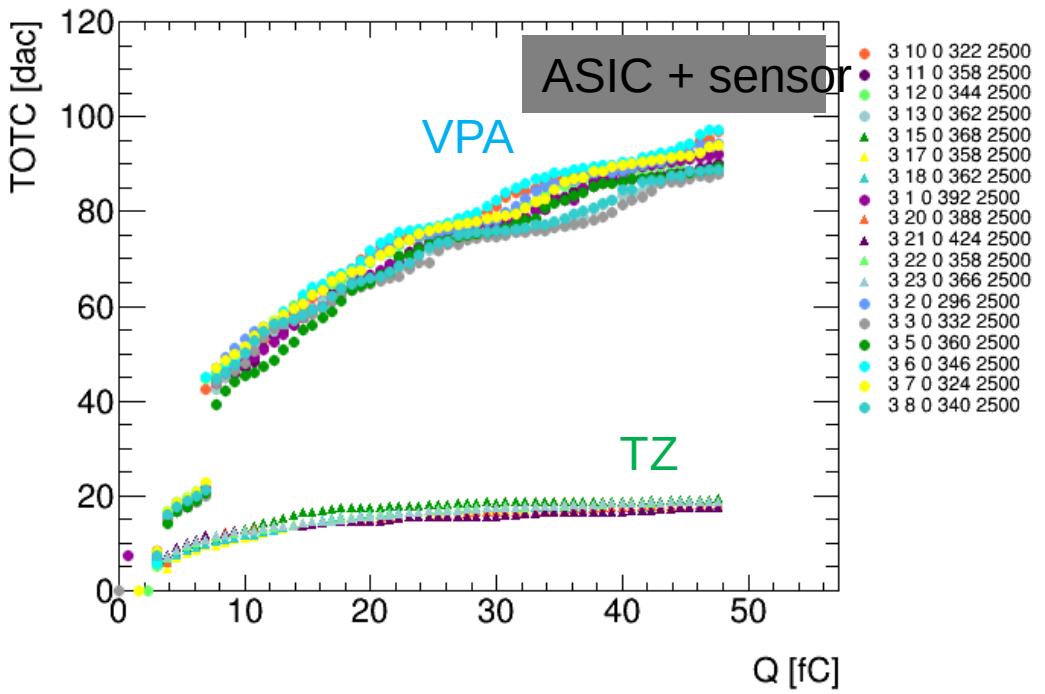
- For HRPPD, we would recommend to start from the mature HGCROC to evaluate the performance at system level
  - Min threshold 15-20 fC, jitter 10 ps, LD BGA package easy to fit on PCB
- EICROC2 16x16 channels not foreseen before 2024
  - EICROC0 still waiting to be characterized because of heavy workload on CMS HGCAL prod
  - Lower threshold, jitter and power, but bump pitch of 500um may be complicated for PCB ?
- Studies scheduled in 2023 to migrate the backend to EIC specs on EICROC and/or HGCROC

Backup

Altiroc1, TOT and time walk validation

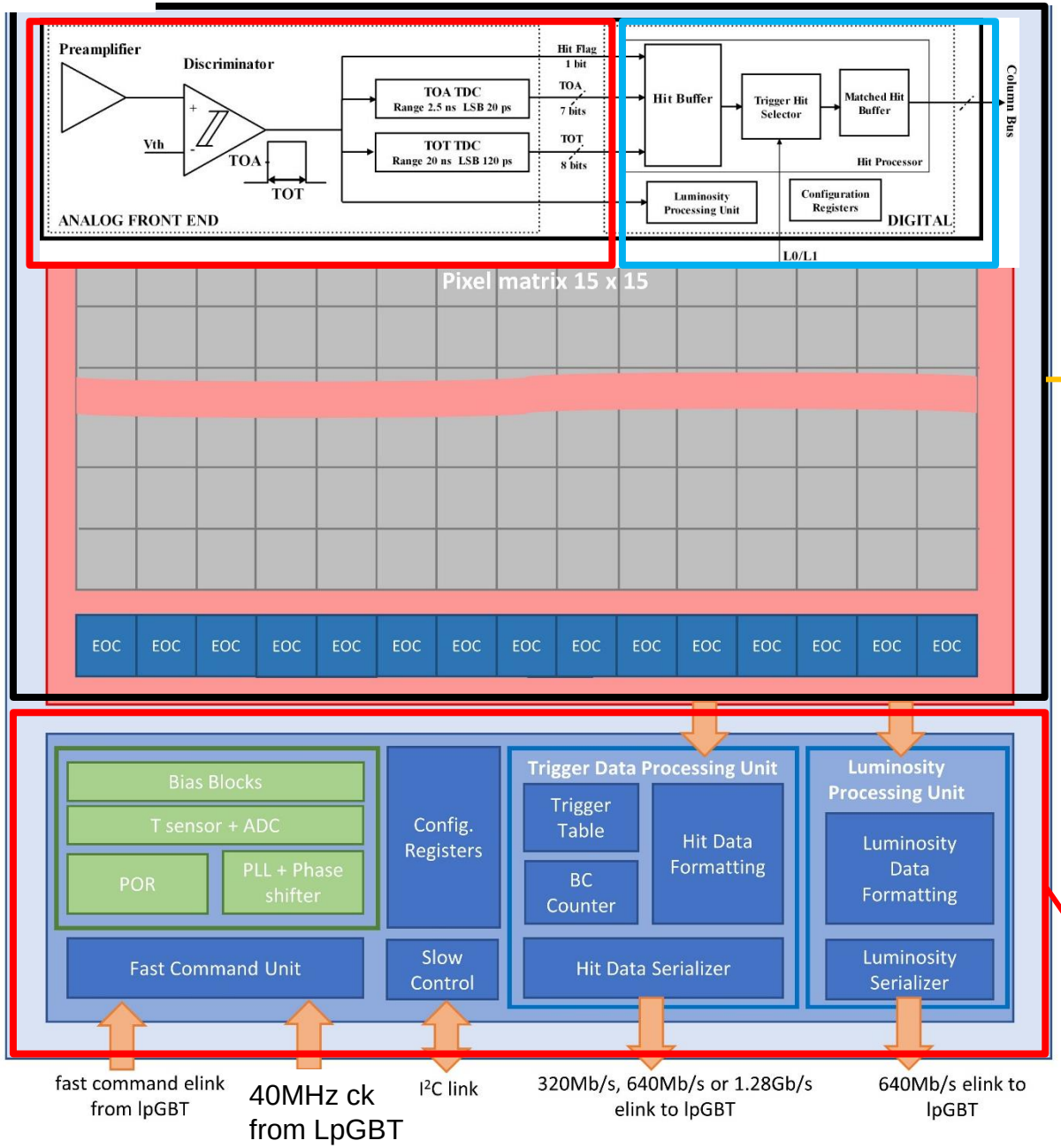
Jitter performance was ok on test bench (see TDR) but no testbeam in 2020 for validation with particles
TOT issue has been further investigated on test bench :

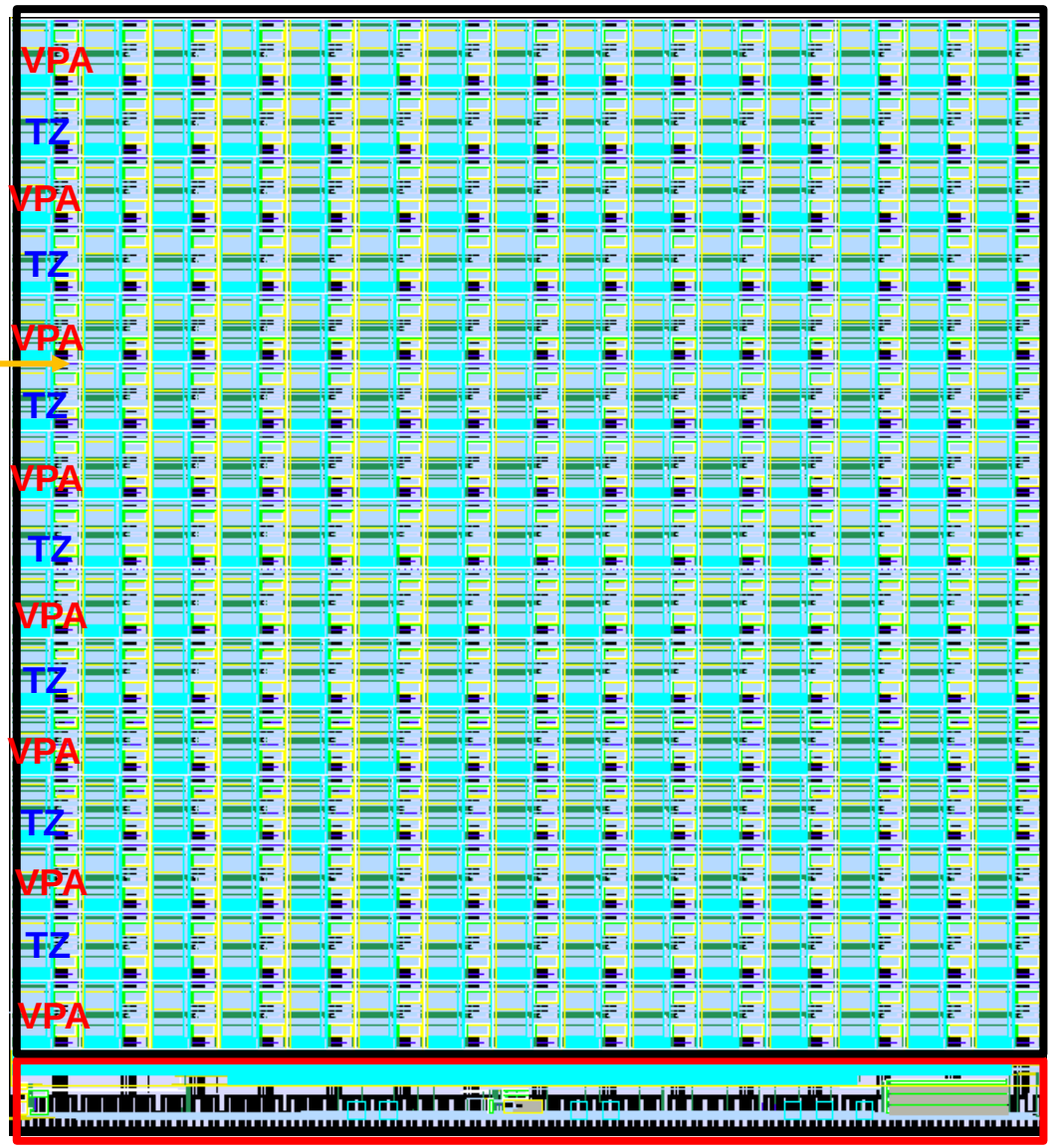




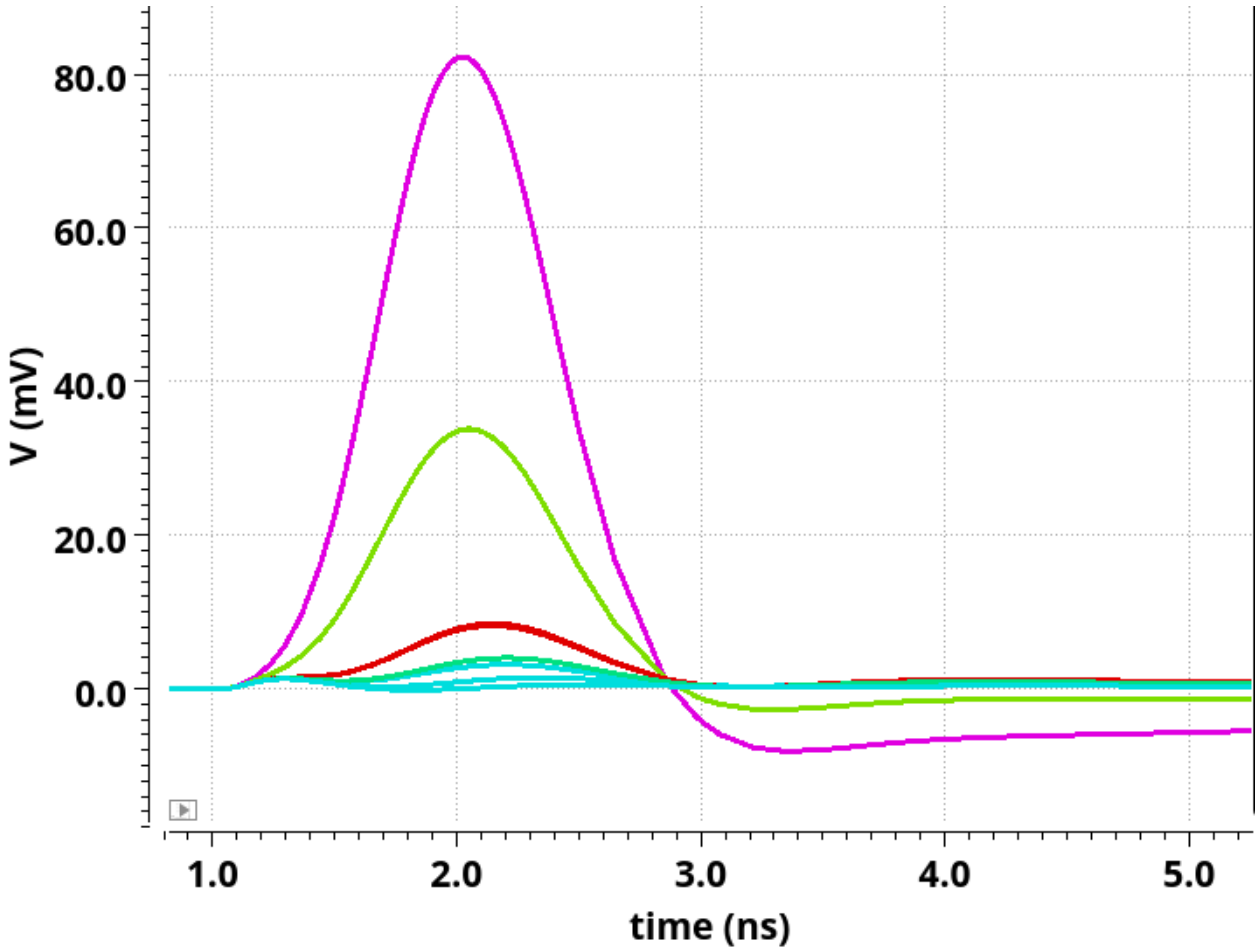
TOT behaviour fine when ASIC alone. It shows small kinks but can be used for time-walk correction
Discontinuities appear when ASIC bump bonded to sensor **AND** Bias Voltage wire-bonded….
Better behavior using Transimpedance preamp (TZ) instead of Voltage preamps (VPA)
=> integration of both preamps types in Altiroc2

Altiroc2 full size ASIC

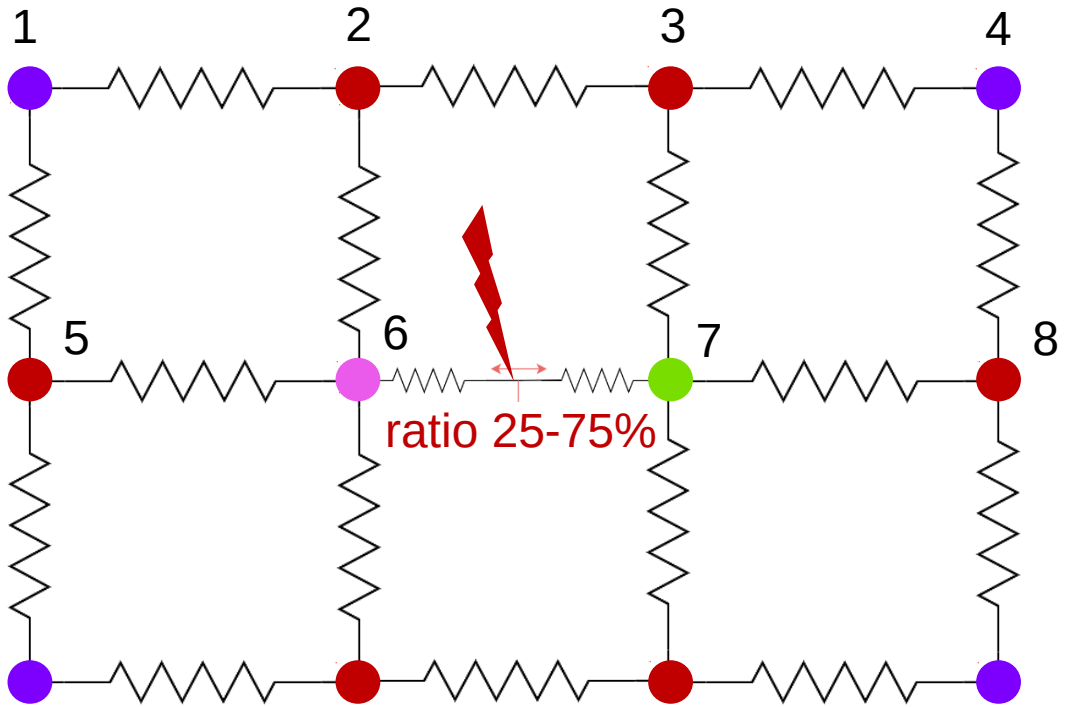




Preamplifier output signal with 25-75%

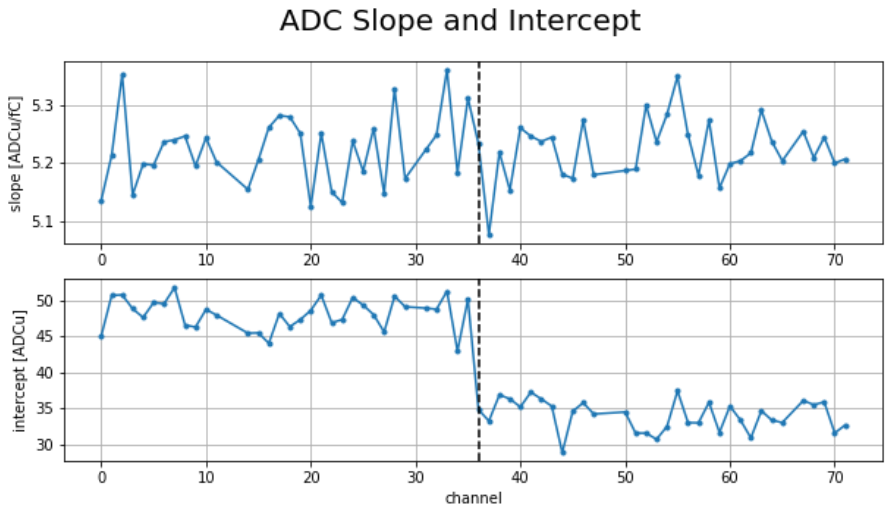


When charge deposition (19 fC) at distance ratio 25-75%

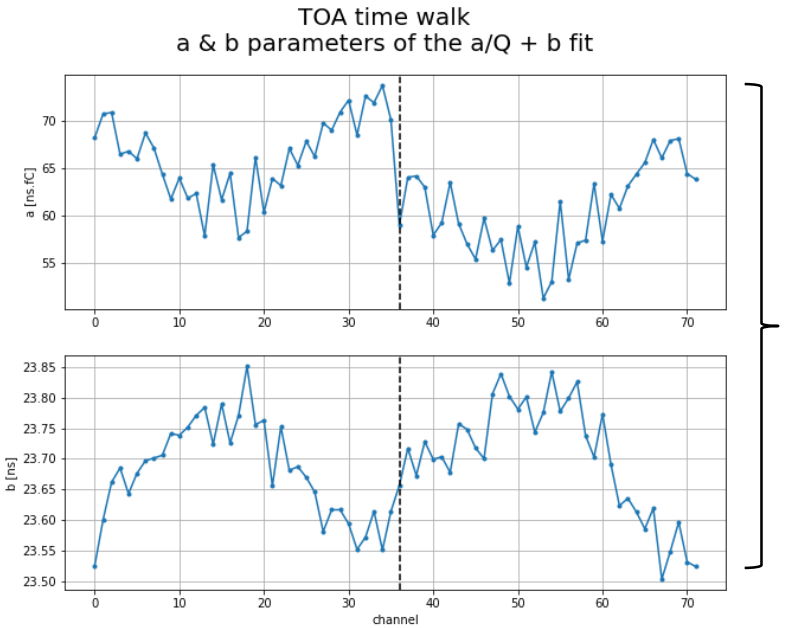


$R_{sheet} = 1\ kOhm$

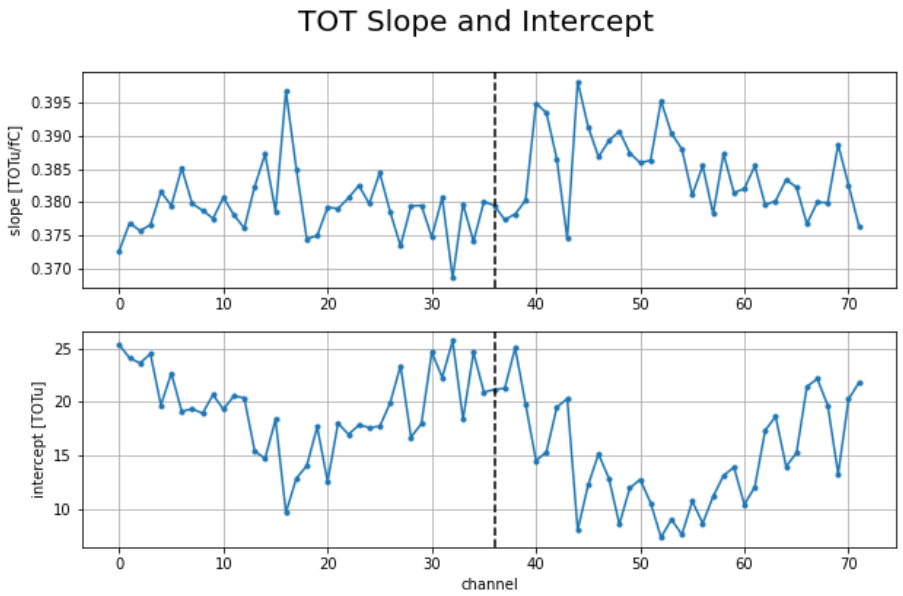
Uniformity



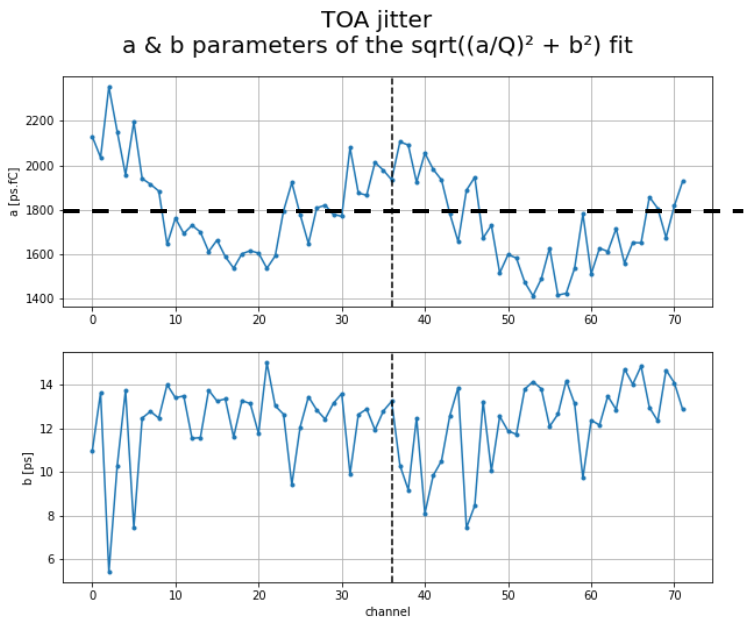
5.2 ADCu / ch
(+/- 2%)



Clock distribution from the middle of each half visible on the time walk distribution



0.38 TOTu / ch
(+/- 3 %)

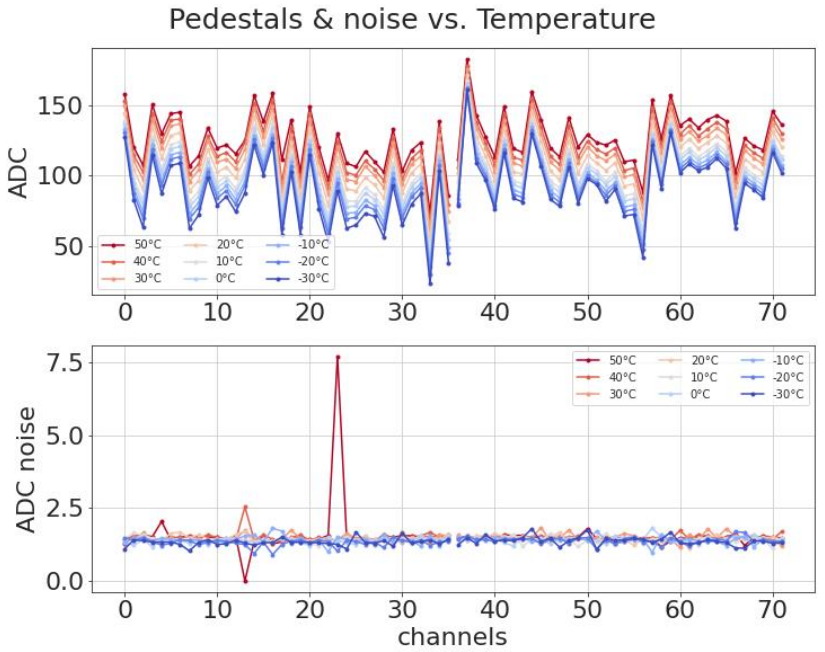


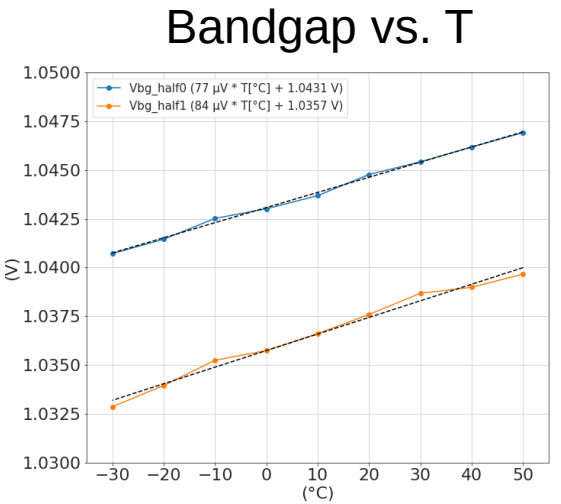
1.8 ns / Q(fC)

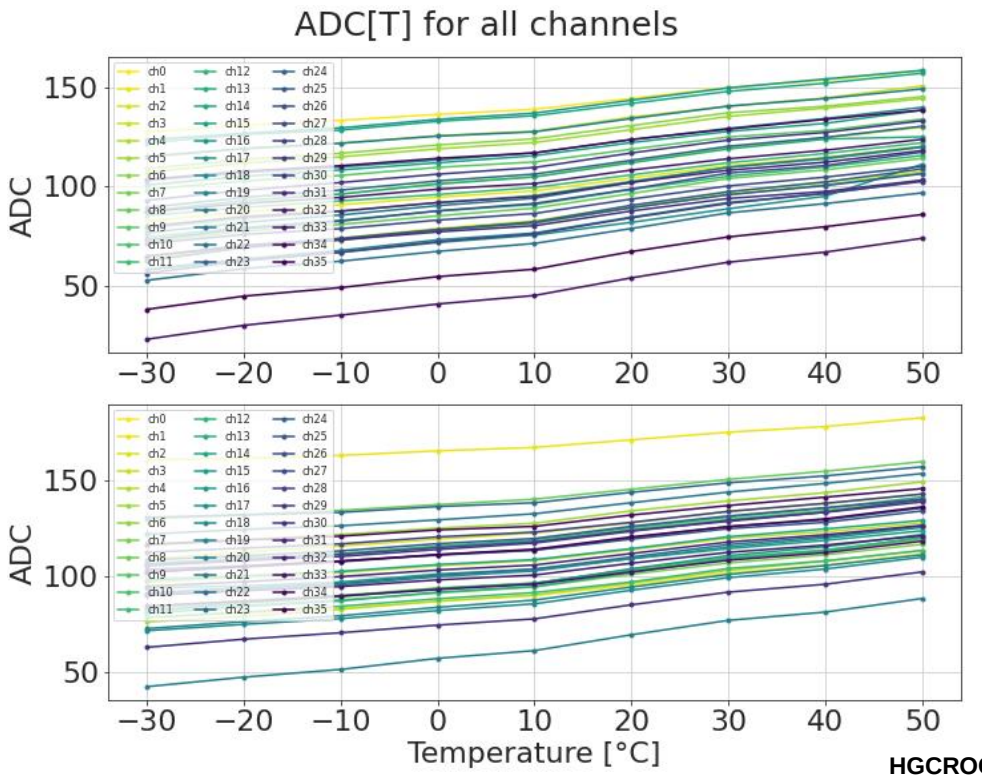
13 ps rms

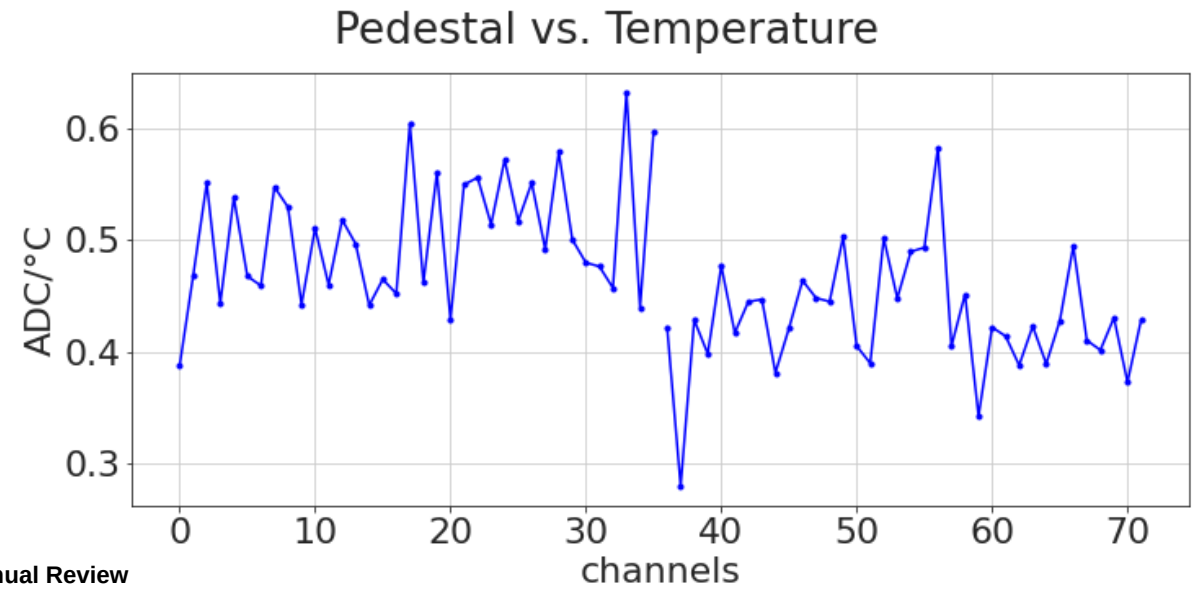
Temperature sensitivity

- Bandgap
  - 80 µV / °C
- Pedestals
  - + 0.5 ADCu/°C



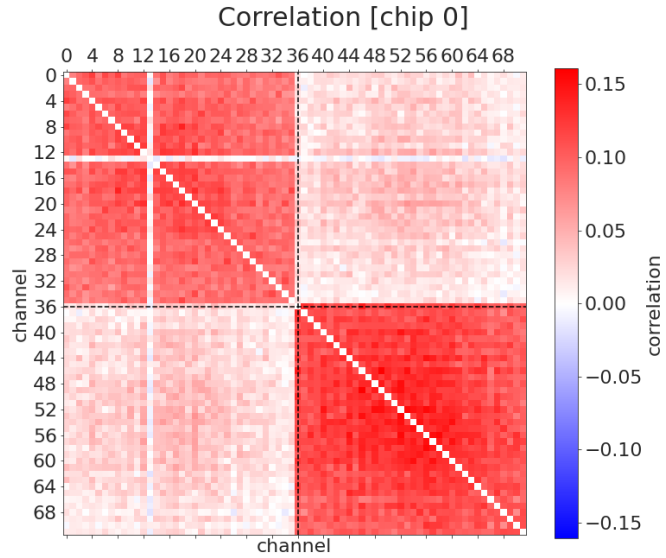




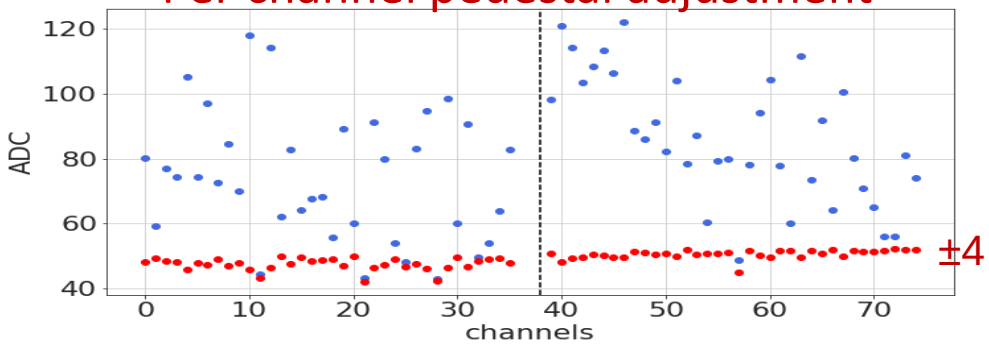


ROCv3: Noise and pedestal measurements

- Measured noise with 47 pF input cap = 0.3 fC (~ 2000 electrons) (0.7 nV / √Hz)
- Very low correlated noise contribution: max 0.15
  - Comparable with HGCROC2 even if the digital activity was doubled
- ADC pedestal adjustment done manually with local 6b DAC

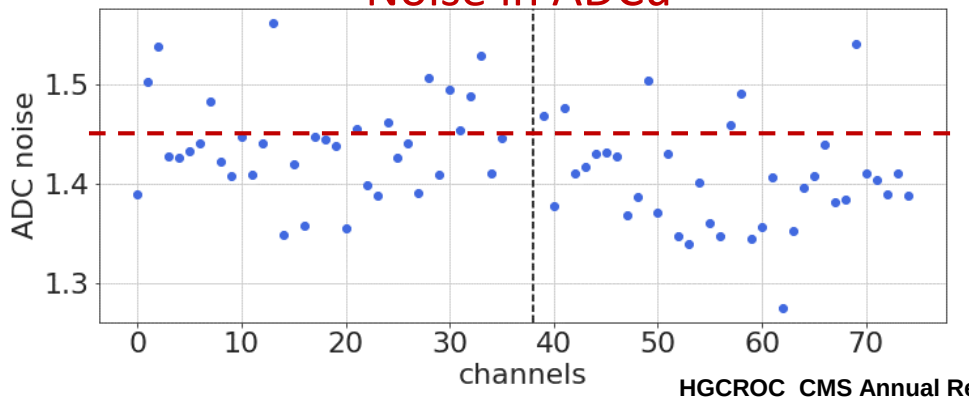


Per channel pedestal adjustment



±4 ADCu

Noise in ADCu



~0.3 fC

Full chip (72 channels)