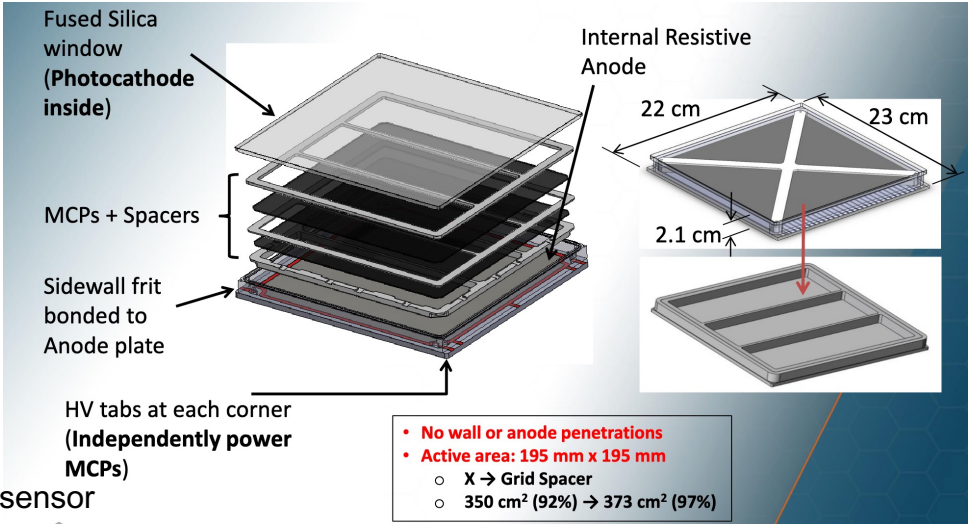
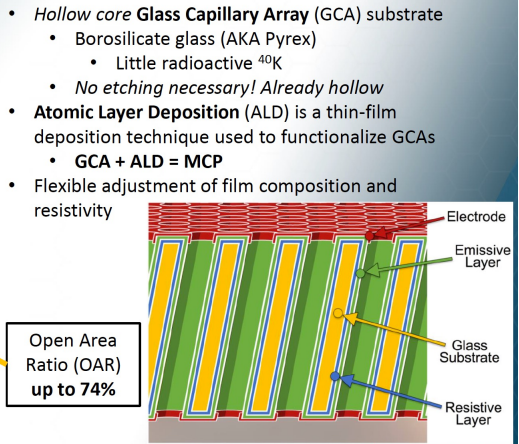
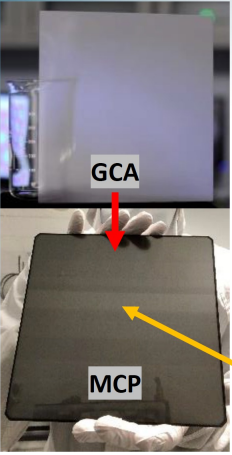


Proximity focusing RICH with HRPPD sensors (and EICROC ASICs?) for the EIC e-endcap

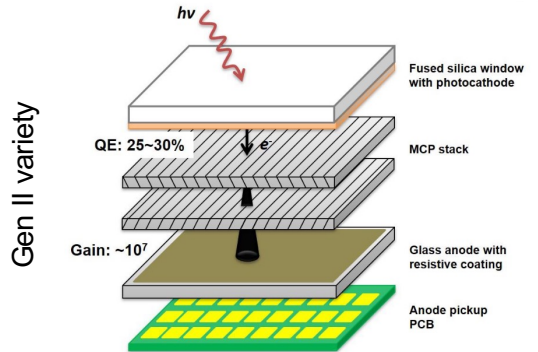
Alexander Kiselev (BNL)

Ad hoc meeting with detector and electronics experts, March 6, 2023

LAPPDs / HRPPDs by Incom Inc.



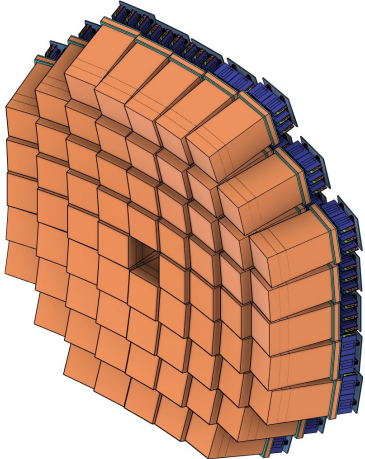
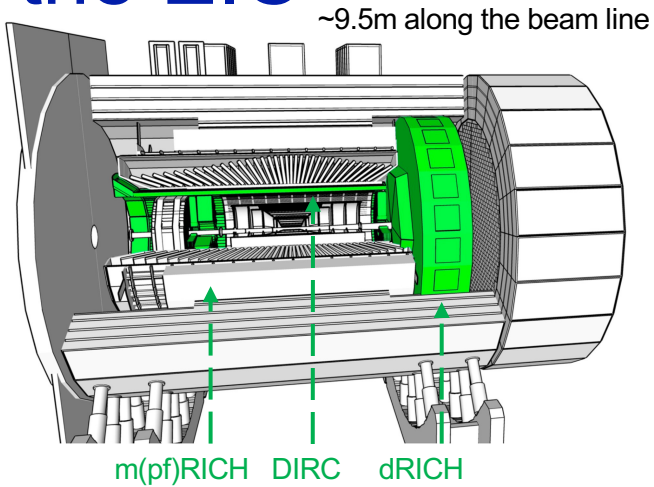
- An affordable large area (finely pixelated) vacuum photosensor
- 10x10 cm² or 20x20 cm² active area
- DC- (Gen I) or capacitively (Gen II) coupled species
- DC-coupled strips or 2D pixellation
- Expected to be (very) cost efficient in mass production
- High enough quantum efficiency and uniform high gain up to $\sim 10^7$
- Sub-mm spatial resolution for finely pixelated tiles
- Single-photon timing resolution on a $\sim 50\text{ps}$ level or higher



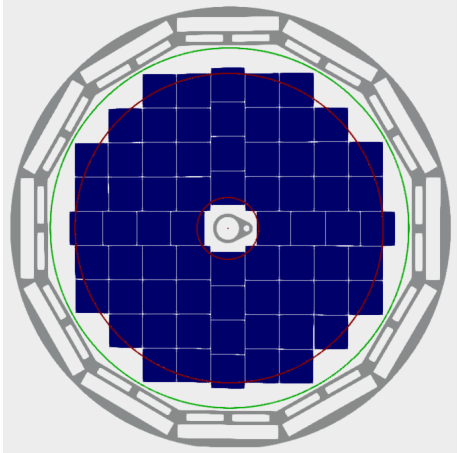
Possible LAPPD applications for the EIC

- mRICH / pfRICH: low dark noise, ToF capability (vs SiPMs)
- DIRC: expected to be more cost-efficient (vs other MCP-PMTs)
- dRICH: problematic, because of the magnetic field orientation

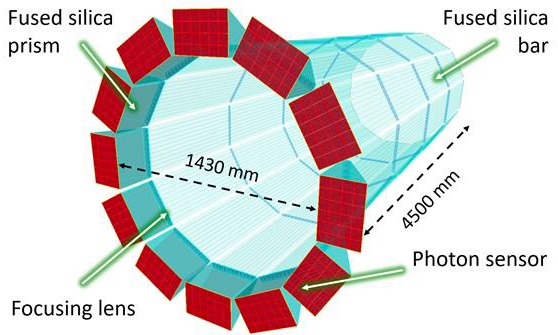
mRICH / pfRICH	either DC-coupled or Gen II, 10cm formfactor
DIRC	DC-coupled, 10cm



mRICH: 68 HRPPDs total

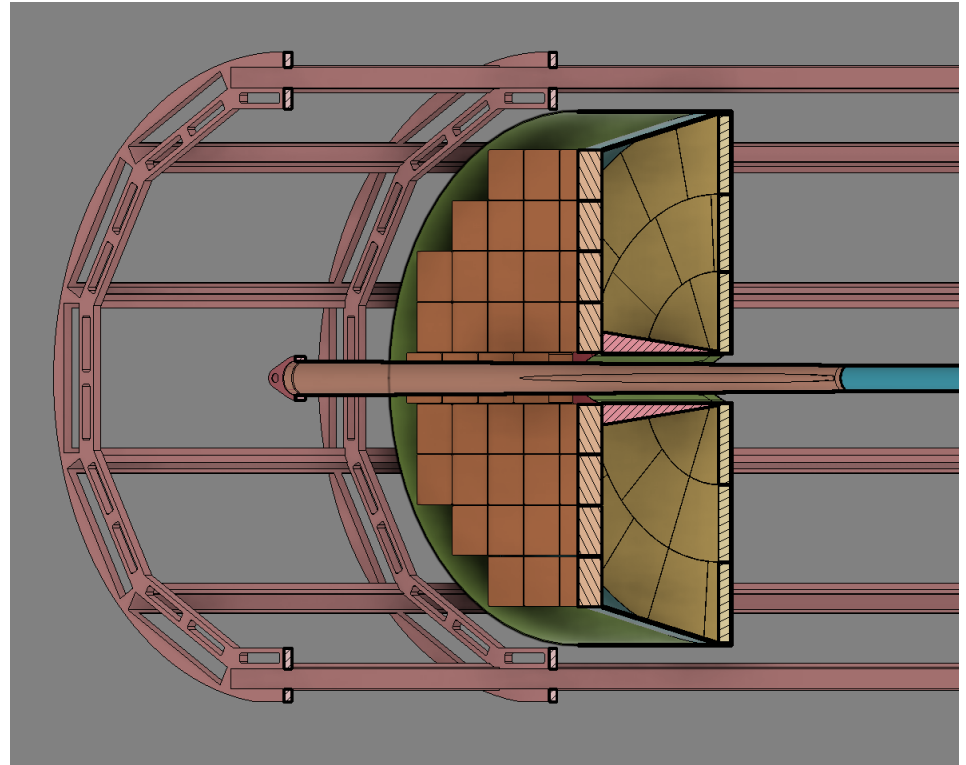
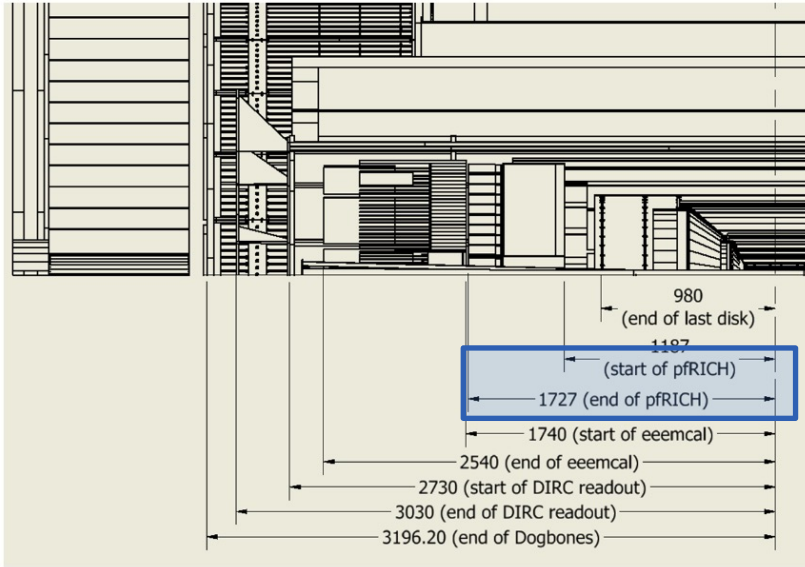


pfRICH sensor plane: 68 HRPPDs total



DIRC: $12 \times 3 \times 2 = 72$ HRPPDs total

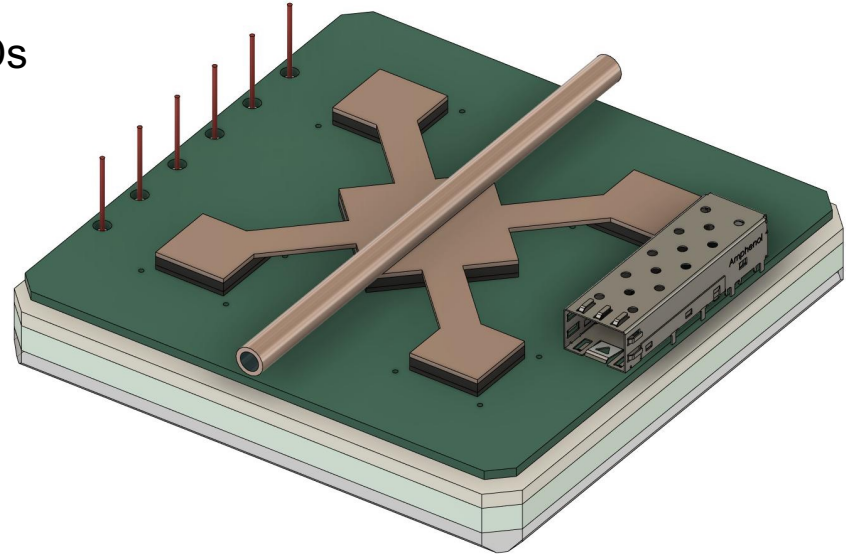
Boundary conditions in the ePIC e-endcap



Inner radius	Mimic beam pipe flange
Outer radius	643 mm
Total length	541.5 mm

HRPPD photosensors & FEE

- A flat sensor wall with 68 12cm x 12cm HRPPDs
- 108mm x 108mm sensitive area
- Pixellation: 32x32 -> 1024 pads per sensor
- FEE: assume four 256ch EICROC chips per sensor; 50mm of space reserved overall
- ASIC bump-bonded to the PCB
- Can afford water cooling if needed
- There will be NO FPGA on board (but copper uplinks to an RDO located nearby)



Requirements to ASIC

- Operating gain: *variable*, up to $\sim 10^7$
- Expected single photon timing resolution $\sim 50\text{ps}$
- Pad capacitance $< 10\text{pF}$, most likely can be made below 5pF
- Leading edge $< 1\text{ns}$
- Noise level (DCR) $\sim 1\text{kHz}/\text{cm}^2$

HRPPD-to-ASIC interface

- Agreed to proceed with the Samtec compression interposers as a lead option

COMPRESSION HARDWARE

ULTRA LOW PROFILE SYSTEMS FOR Z-RAY® INTERPOSERS

- Designed for Z-Ray®, the lowest profile, most flexible high-density micro interposer in the industry (ZA8 and ZA1 Series)
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- Ultra low profile
- Reduces risk of damage to the interposer
- ZSO Series for single compression with solder balls
- ZHSI and ZD Series for dual compression interposers



Provides alignment

Protects solder ball joints when compressed

ZSO

ZD

ZHSI

Provides alignment and compression

