OAK RIDGE National Laboratory

# Synergy between HGCROC and EICROC

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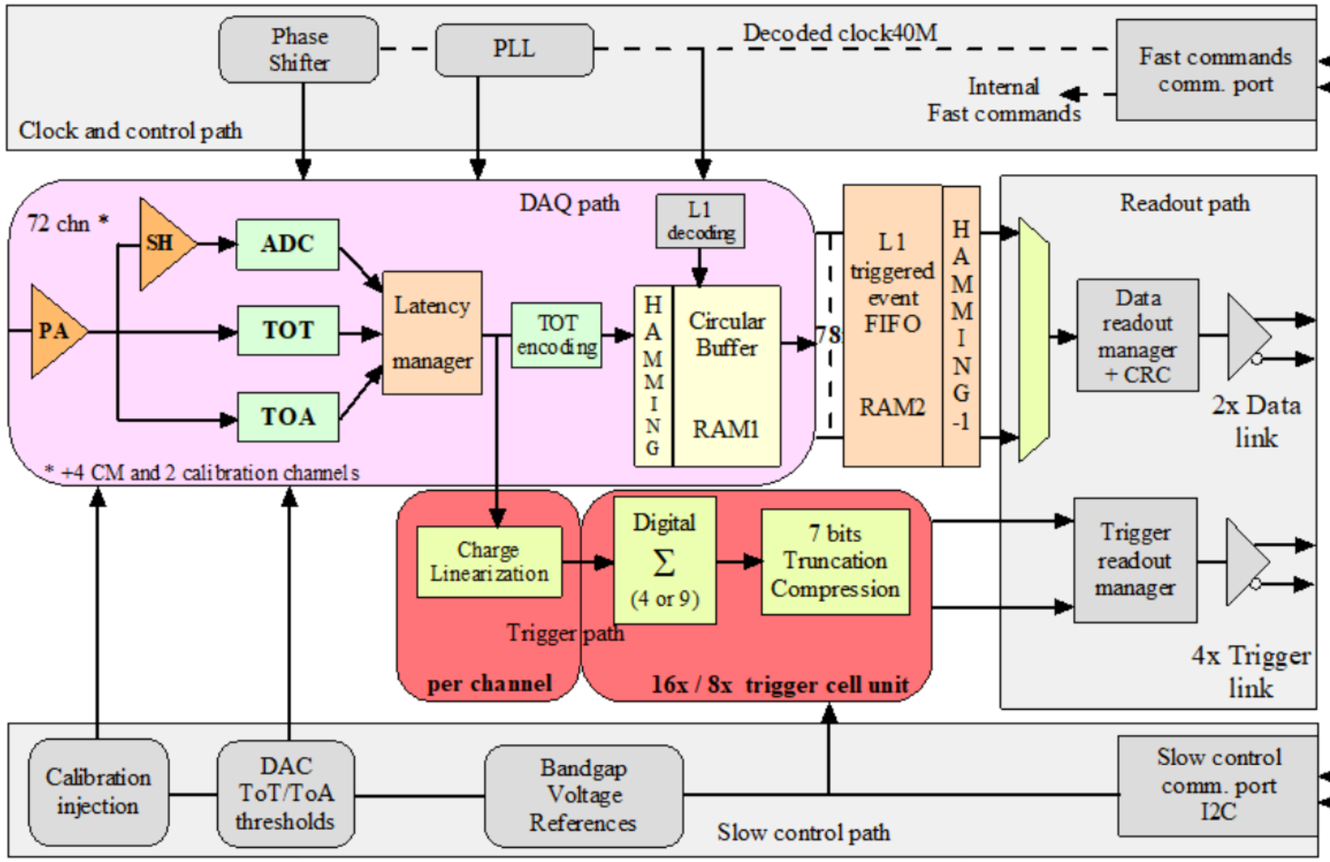
(ORNL)

ORNL is managed by UT-Battelle LLC for the US Department of Energy

# HGCROC architecture




**Existing ASIC for CMS, ALICE detectors**

**Overall chip divided in two symmetrical parts:**

- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

**Measurements:**

- Charge:
  - **ADC peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution**
  - TDC: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - **Time of arrival, 10 bits (25ps)**

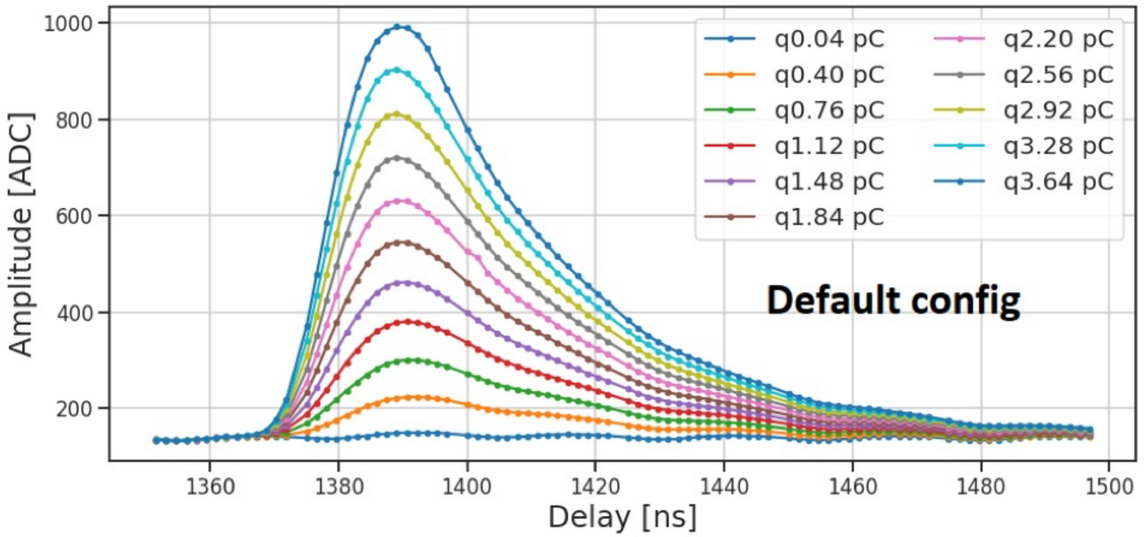
**Data flow:**

- DAQ path:
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- **Trigger path:**
  - **Sum of 4 or 9 channels, linearization, compression to 7bits**
  - **4 x 1.28 Gbps links**

Control:

- Fast commands, **40MHz and 320MHz clock**
- I2C for slow control

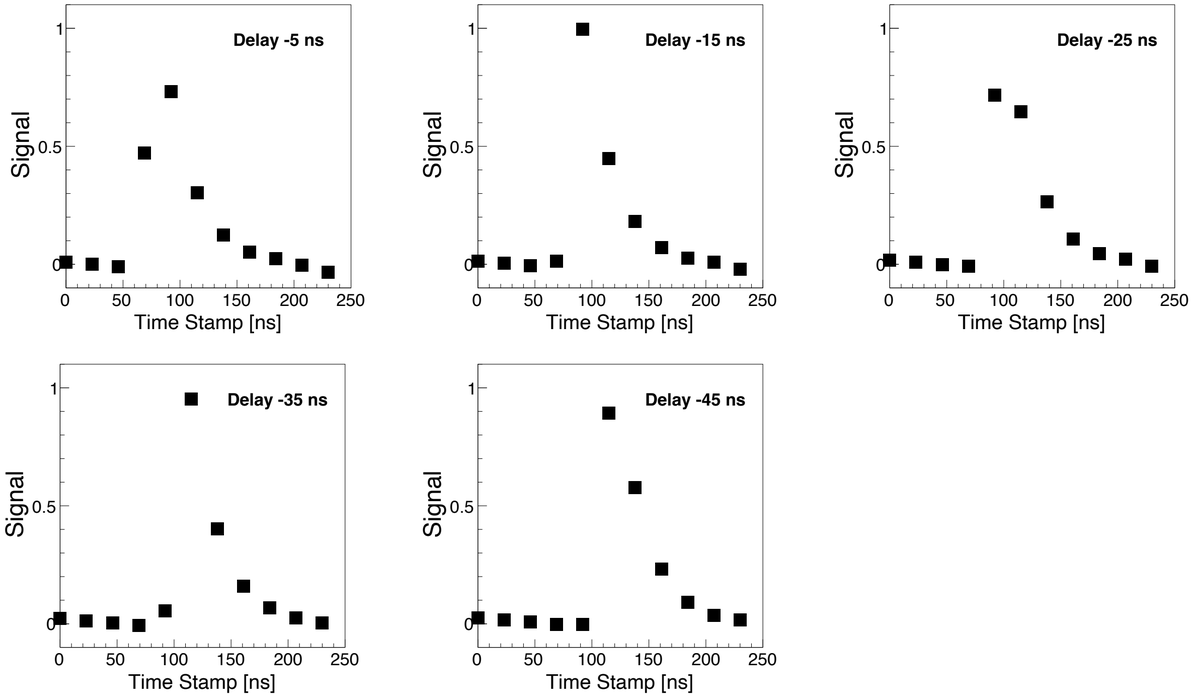
# HGCROC for EIC use




**Signal from the shapers:**

- SiPM response of the H2GCROCv3 (from CMS)
- Default configuration used

Can it be used with the EIC 100 MHz clock?

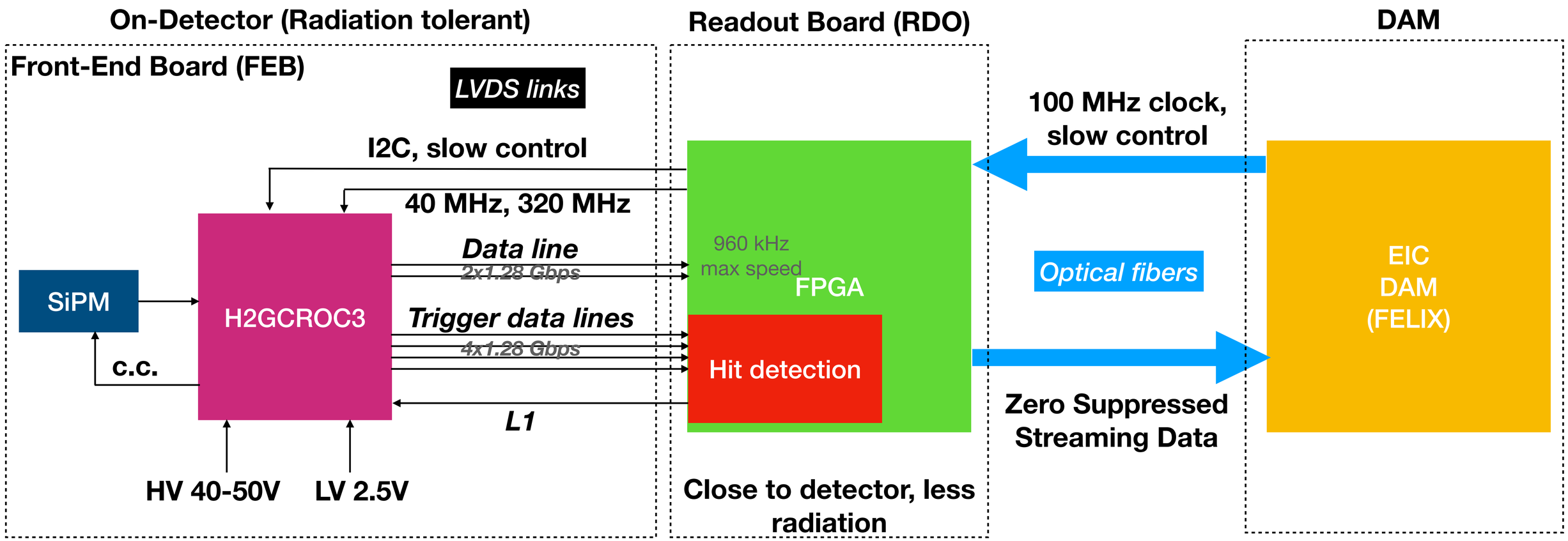



**There are 5 different phases of the signal sampled with the 40 MHz clock:**

- The new version of the H2GCROCv3 can read out multiple consecutive bunch crossings
- For good signal reconstruction, we plan to save 3 (or 4) samples for each signal
- Total: 3 ADC, 3 TOA and 3 TOT values, 32bitx3 words for each physics signal

We can reconstruct the phases (using TOA) and the shower shape (ADC+TOT template fit) for the EIC 100 MHz clock

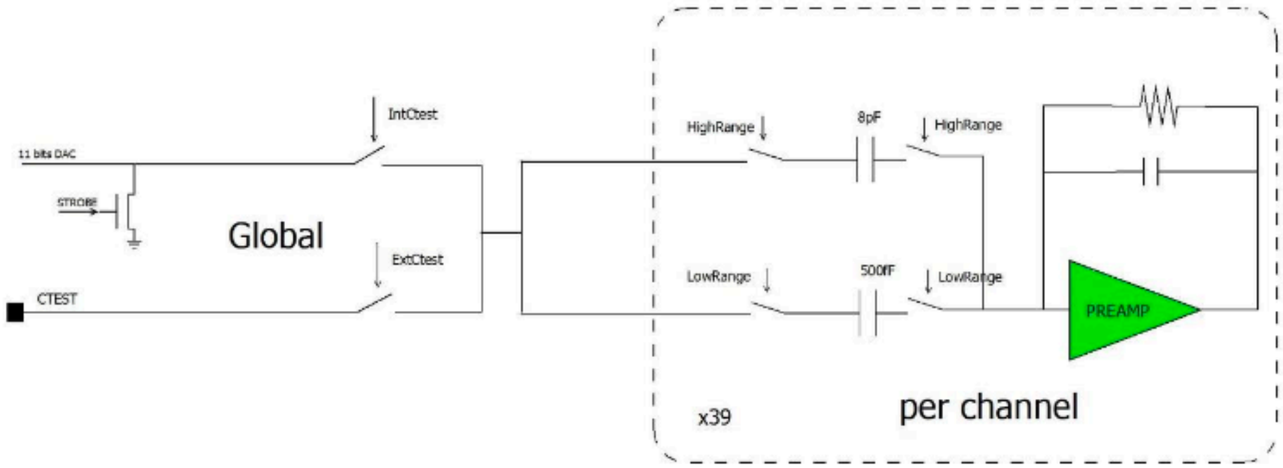
# LFHCAL hierarchy




**Data propagation from the detector to the EPIC DAQ system:**

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

# Internal calibration




**Internal Calibration circuit implemented in the HGCROC:**

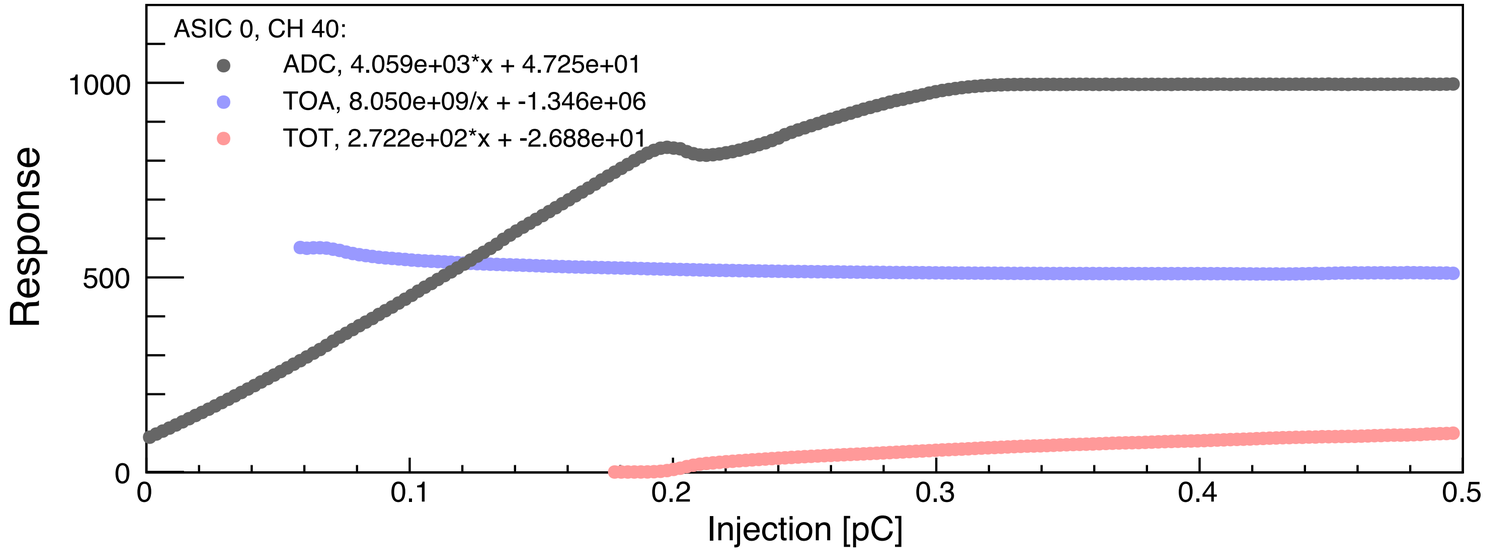
- Almost the full dynamic range. Reference voltage 0-1V:
  - 0.5 pF Low Range: 0 - 0.5 pC
  - 8 pF High Range: 0- 8 pC

Calibration circuit injection value of 11-bit:
*Can be used to identify the thresholds for TOA and TOT, check linearity, etc.*

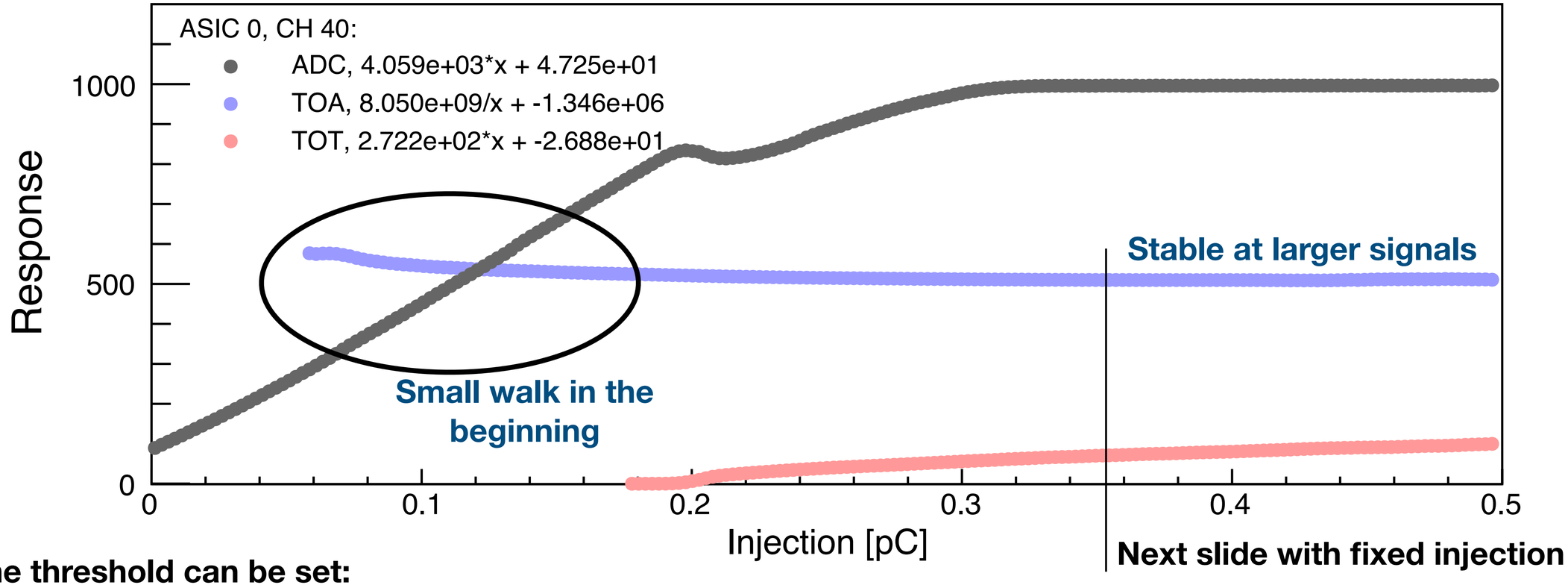
**Dynamic range of the HGCROC:**

- Real data from the v2 chip
- Silicon variant
- ADC set to saturate around 850:
  - Small dip in the ADC happens when the TOT circuit comes online
  - TOT values are shown only to 100 (out of the 4095 range)
  - TOA have a small walk from threshold to 0.18 fC, then it is stable

*We are currently working on the same data for the HGCROC chip*



# Zoom-in to the timing




**The threshold can be set:**

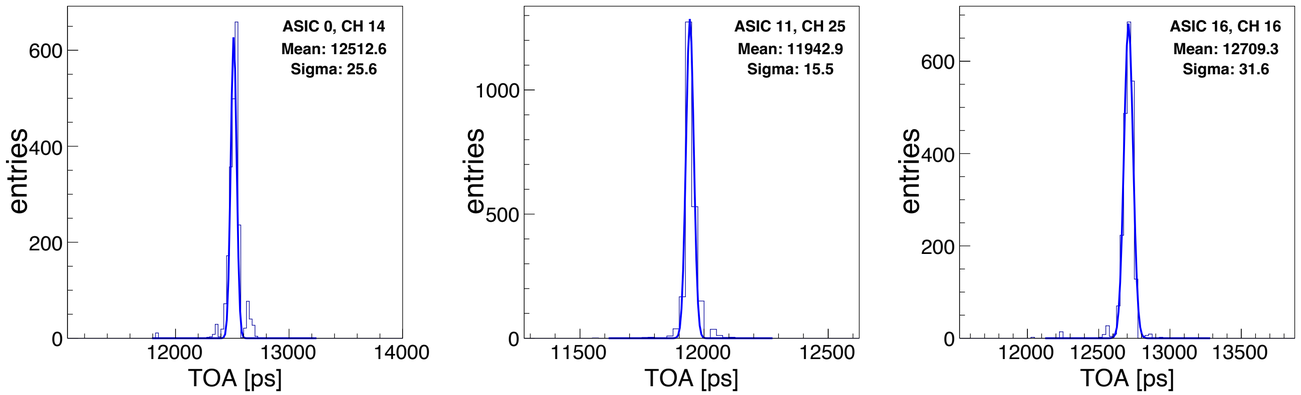
- One global value for 36 Channels (half of the chip)
- Individual channel-by-channel (36 parameters)

Walk is minimal, can be adjusted with the ADC

**EICROC0 design:**

- TZ Preamplifiers from ALTIROC
- TDC from HGCROC (CMS, CEA/Irfu/DEDIP)
- 8 bit ADC for time-walk correction (AGH Krakow, adapted from HGCROC)

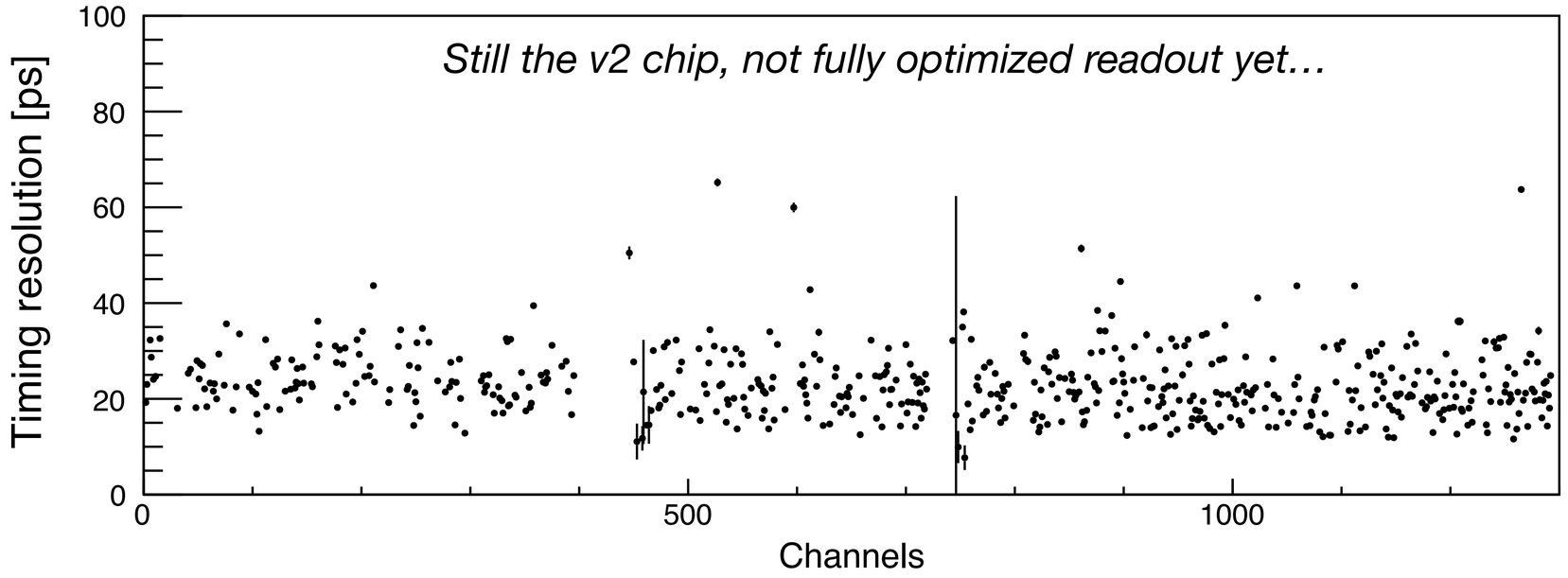
# At fixed injection value (in the stable region)



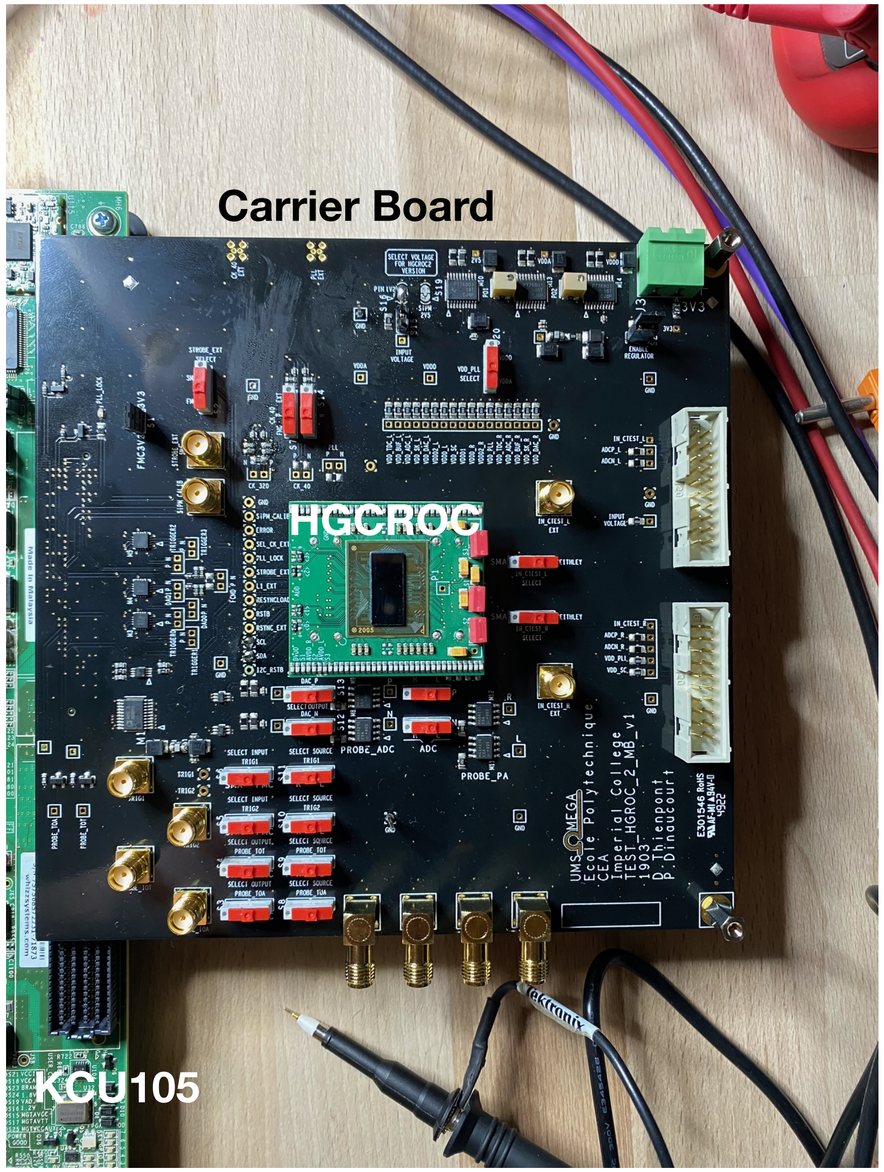

**Some examples of the TOA timing distribution**

**Resolution extracted from 18 ASICs in series:**

- Run by a Xilinx Ultrascale FPGA
- 18 in series (from 30cm to 10cm distance from FPGA-ASIC)
- Extracted the timing resolution where I could: 15-35 ps in general



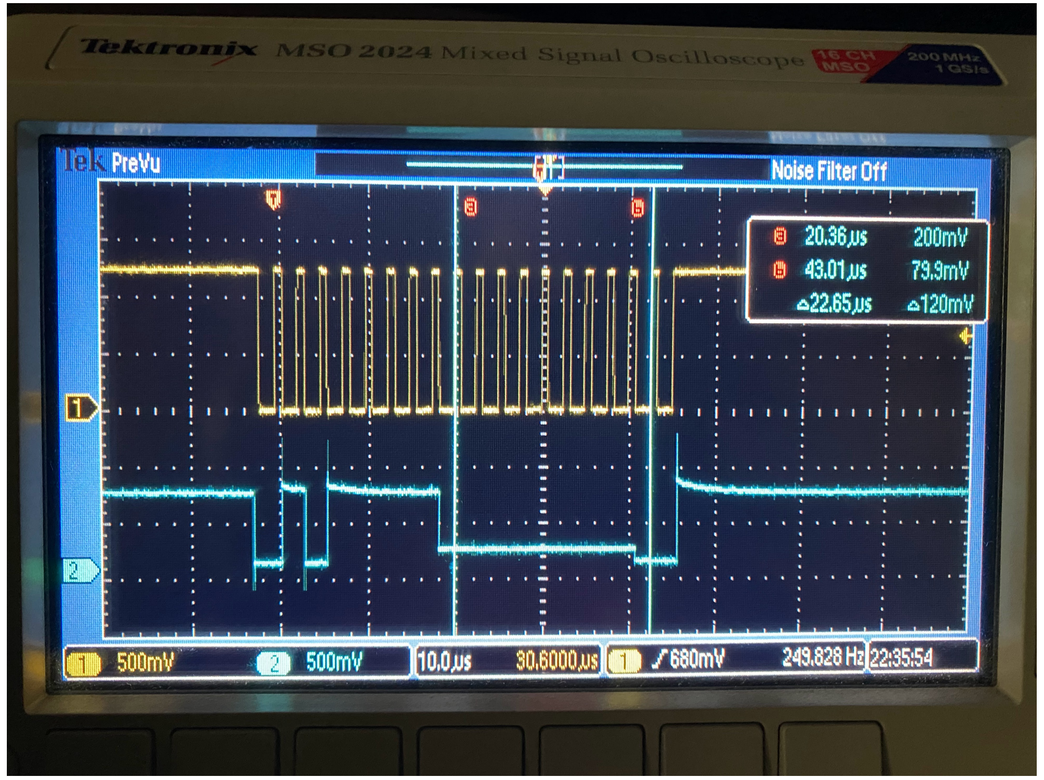
# Starting to test HGCROC3 with testing board




**Testing the HGCROC feasibility for the EIC use:**

- Carrier board (ordered 5 of them, delivery under progress from CERN)
- Mezzanine board with HGCROC (ordered 5 of them for testing, delivery 4-5 weeks)

Firmware on the KCU105 evaluation board is done by Omega. We are currently updating, upgrading the readout code.



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# Our plan for the FY2023

**Milestones:**

1. **HGCROC basic tests: April 2023:**
   - Already started, trying to figure out the setups with the HGCROC
   - All documents are available from Omega, I shared it with some interested people from the Call Groups, I can share it here too
2. **Start of tests of HGCROC with SiPM: May 2023**
   - We also have a parasitic test beam in June at CERN for first real tests
   - Comparison with the CAEN units (only ADC, there is no timing there)
3. **Prototype PCB: September 2023**
   - We can produce one non-test board setup
   - We have a possibility to have a parasitic testbeam in CERN again
4. **Start of on-detector prototype PCB: October 2023**
   - Here we probably wanted 1-2, but we can add more (72ch/board)
   - **It is probably here where we could start to think to produce something for pfRICH**
5. **Firmware development: December 2023**
6. **Beam tests: December 2023**
   - Dedicated for the LFHCAL module

# Backups

# Possible use of ECON-D in LFHCal

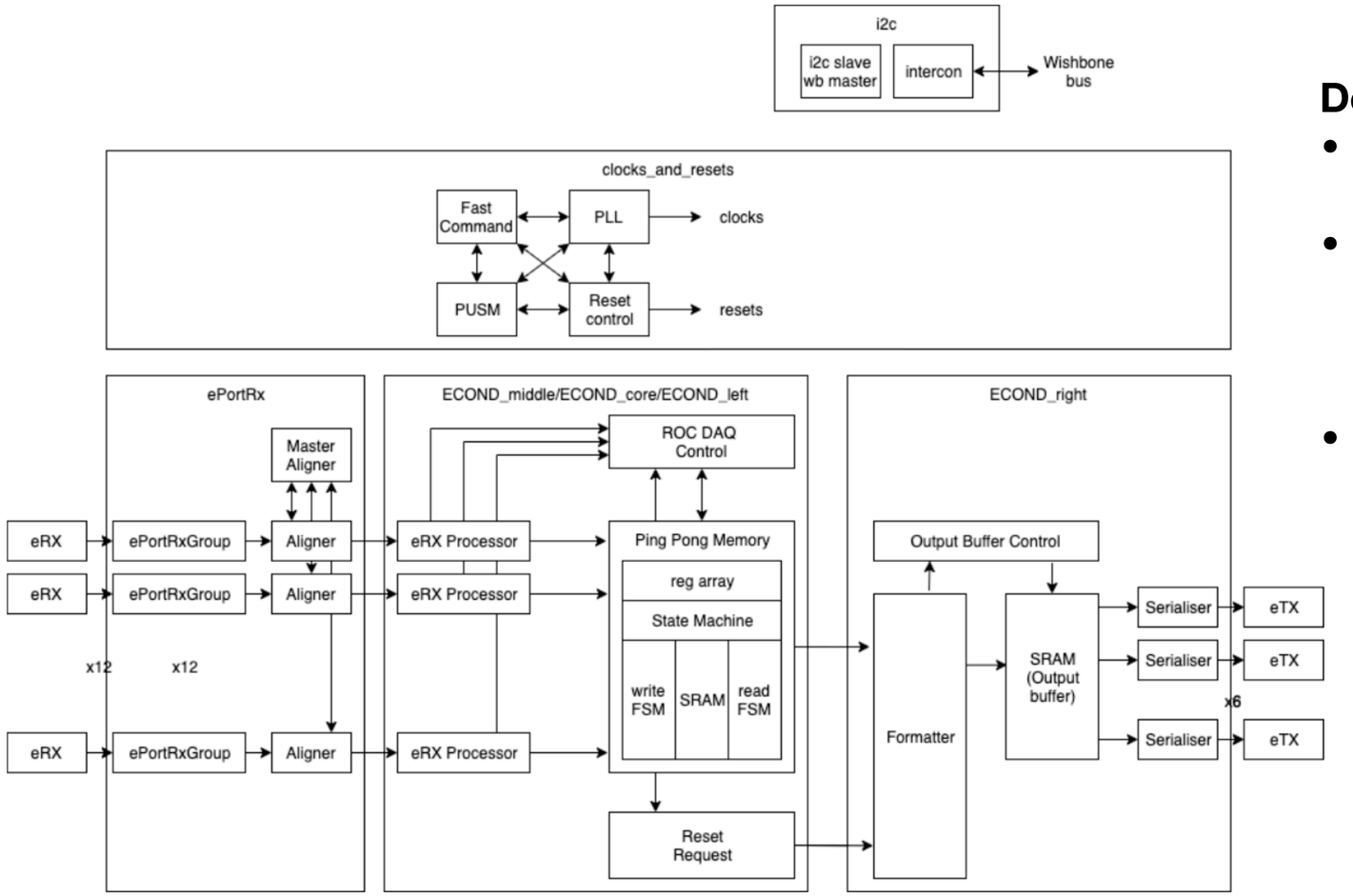



Figure 3 ECON-D Functional Block Diagram

**Developed for CMS HGCal in Fermilab:**

- First submission in March, we want 5-10 of them for testing at least
- Only “functionality” is zero suppression. In principle 12 lines in, 1-6 lines out (depends on the occupancy, how much zero suppressed data we need to ship out)
- Very radiation tolerant, would reduce a lot of cabling, services

**This is just a thought:**
**If we keep the same data format in EICROC, can this be used (maybe with modification)?**

# Possible use of ECON-T in LFHCal

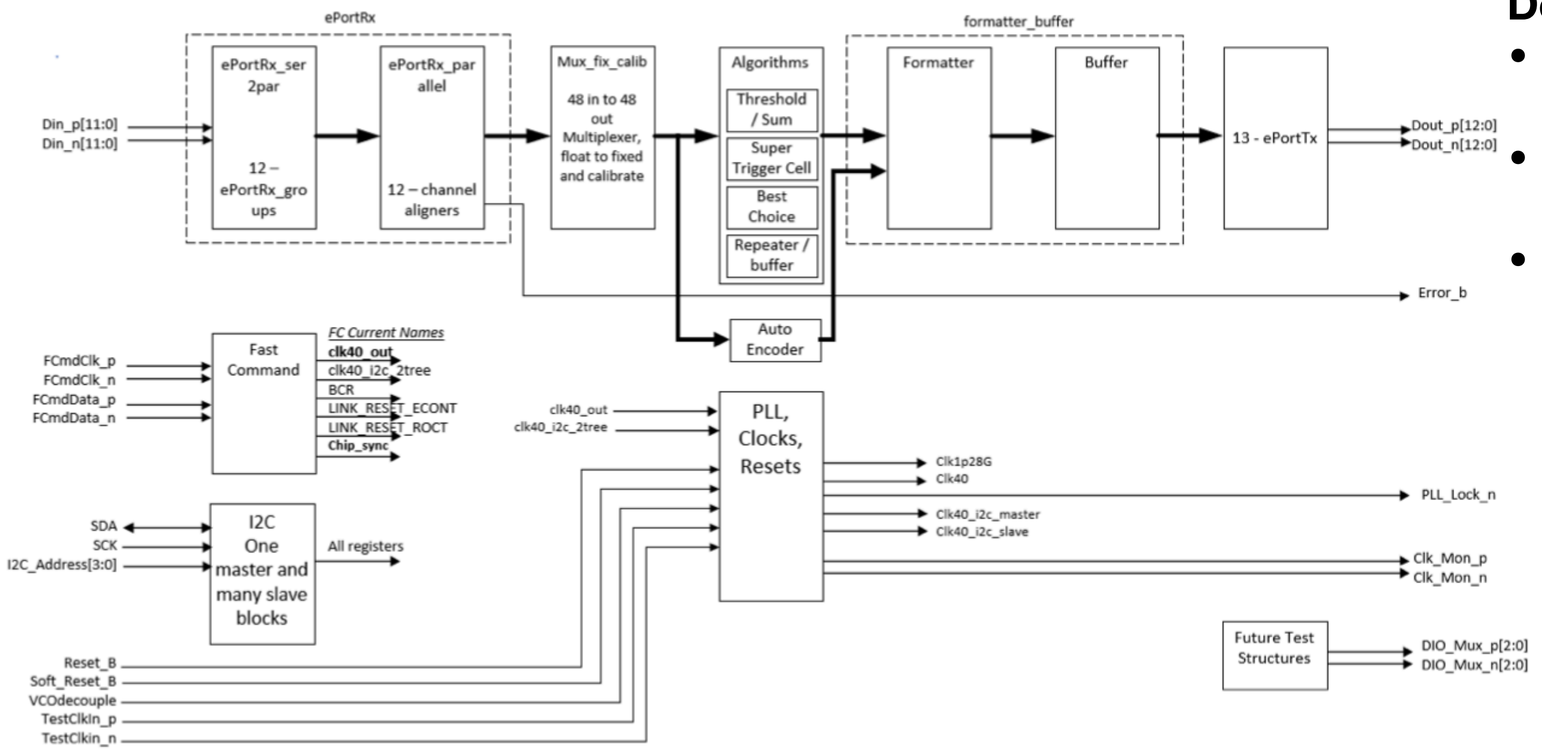
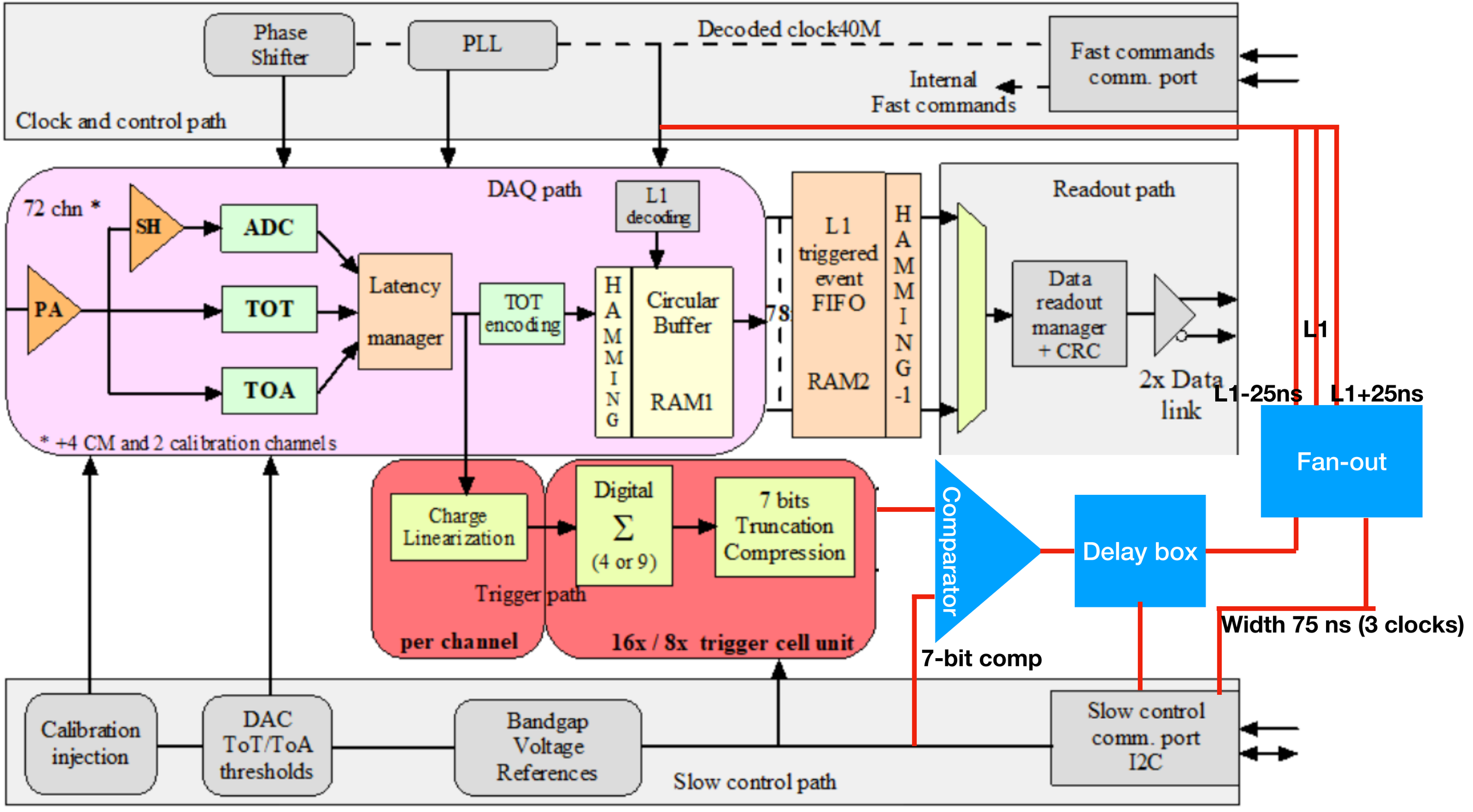
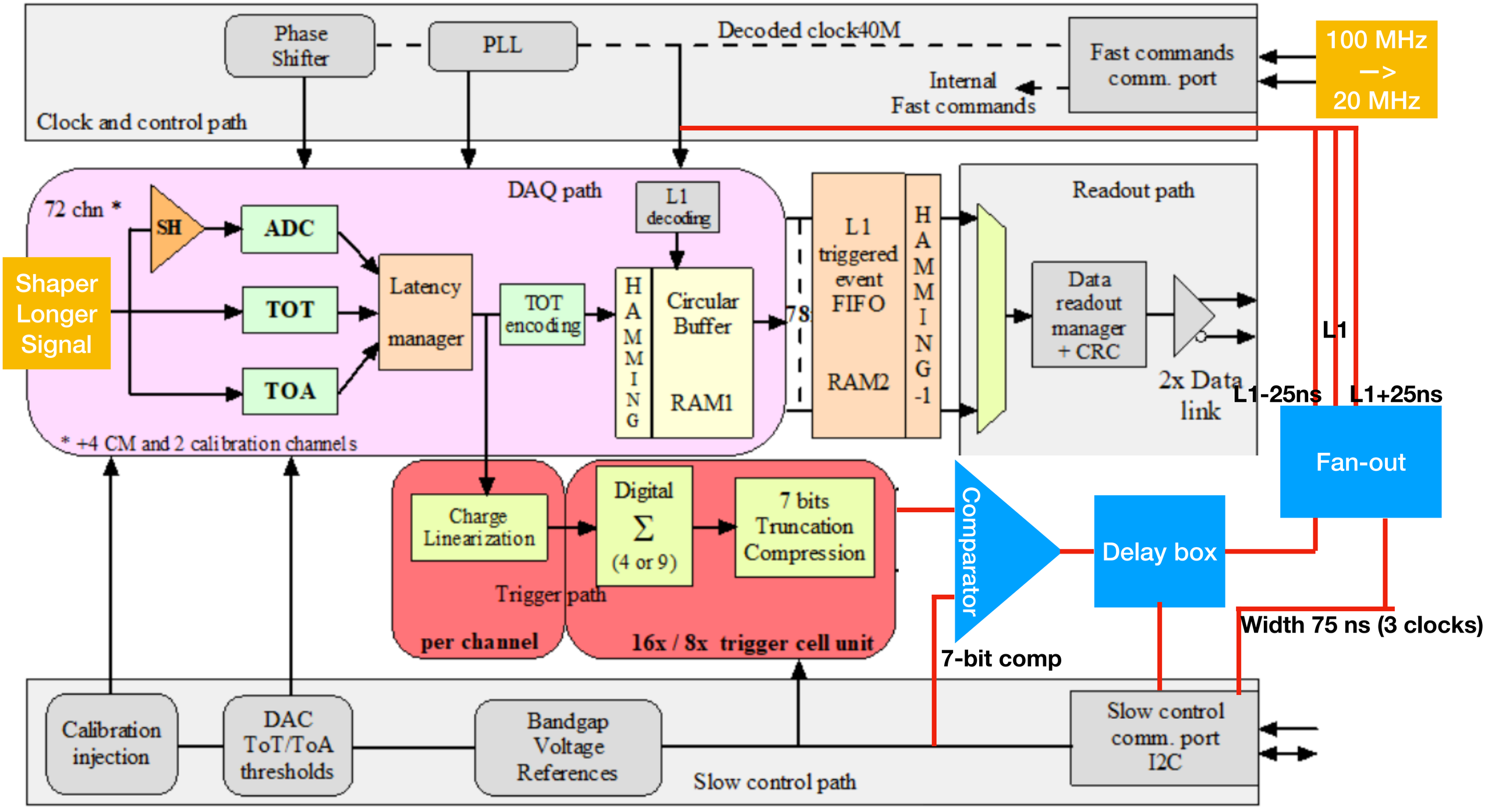



Figure 3 ECON-T Functional Block Diagram

**Developed for CMS HGCal in Fermilab:**

- First submission in March, we want 5-10 of them for testing at least
- Very radiation tolerant, would reduce a lot of cabling, services
- Functionality - sum up more channels, do some extra comparisons/algorithms. Not sure if it would be useful.
  - We plan to not ship out the trigger info, just to the FPGA


Phase Shifter
PLL
Decoded clock40M
Fast commands comm. port
Internal Fast commands
Clock and control path
DAQ path
72 chn *
SH
ADC
PA
TOT
TOA
Latency manager
TOT encoding
L1 decoding
HAMMING
Circular Buffer
RAM1
78
L1 triggered event FIFO
RAM2
HAMMING -1
Readout path
Data readout manager + CRC
2x Data link
L1
L1-25ns
L1+25ns
Fan-out
* +4 CM and 2 calibration channels
Charge Linearization
Digital Σ (4 or 9)
7 bits Truncation Compression
Trigger path
per channel
16x / 8x trigger cell unit
Comparator
Delay box
Width 75 ns (3 clocks)
7-bit comp
Calibration injection
DAC ToT/ToA thresholds
Bandgap Voltage References
Slow control path
Slow control comm. port I2C


Phase Shifter
PLL
Decoded clock40M
Fast commands comm. port
Internal Fast commands
100 MHz —> 20 MHz
Clock and control path
DAQ path
72 chn *
SH
ADC
TOT
TOA
Shaper Longer Signal
Latency manager
TOT encoding
L1 decoding
HAMMING
Circular Buffer
RAM1
78
L1 triggered event FIFO
RAM2
HAMMING -1
Readout path
Data readout manager + CRC
2x Data link
L1
L1-25ns
L1+25ns
Fan-out
* +4 CM and 2 calibration channels
Charge Linearization
Digital Σ (4 or 9)
7 bits Truncation Compression
Trigger path
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