DRS4 calibration

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LAPPD Workshop, 20 April 2023

Calibration of the DRS4 board

- The CAEN v1742 digitizer is a VME board with 32 channels (plus 4 channels for two trigger inputs) based on the DRS4 chip
  - 4 DRS4 chips, 8 (signals) + 1 (trigger) channels each
  - Maximum sampling rate is 5 GS/s, i.e. ~200 ps per cell on average, with 1024 cells per channels (full acquisition window of 204.8 ns)
- The board comes precalibrated from the factory, but the default calibration is largely suboptimal
  - Need to perform a thorough calibration offline to achieve ultimate performances of the DRS4 ASIC
- Two types of calibration
  - Calibration of voltage offsets for each cell
  - Calibration of time width of each cell
- The calibration has to be done cell by cell, which means 1024x(32+2x2) sets of calibration constrants if one wants to calibrate it all

DRS4 cell offset calibration

- The DRS4 chip is based on switched capacitor arrays operated in in sample-and-hold mode
- A fast sequence of write pulses allows the recording of analog waveforms in the capacitors at high frequency, which can later be read out and digitised via ADCs at a much lower speed
- Each cell comes with a random offset which is constant over time
  - But depends on temperature, hence for ultimate precision the temperature has to be kept stable

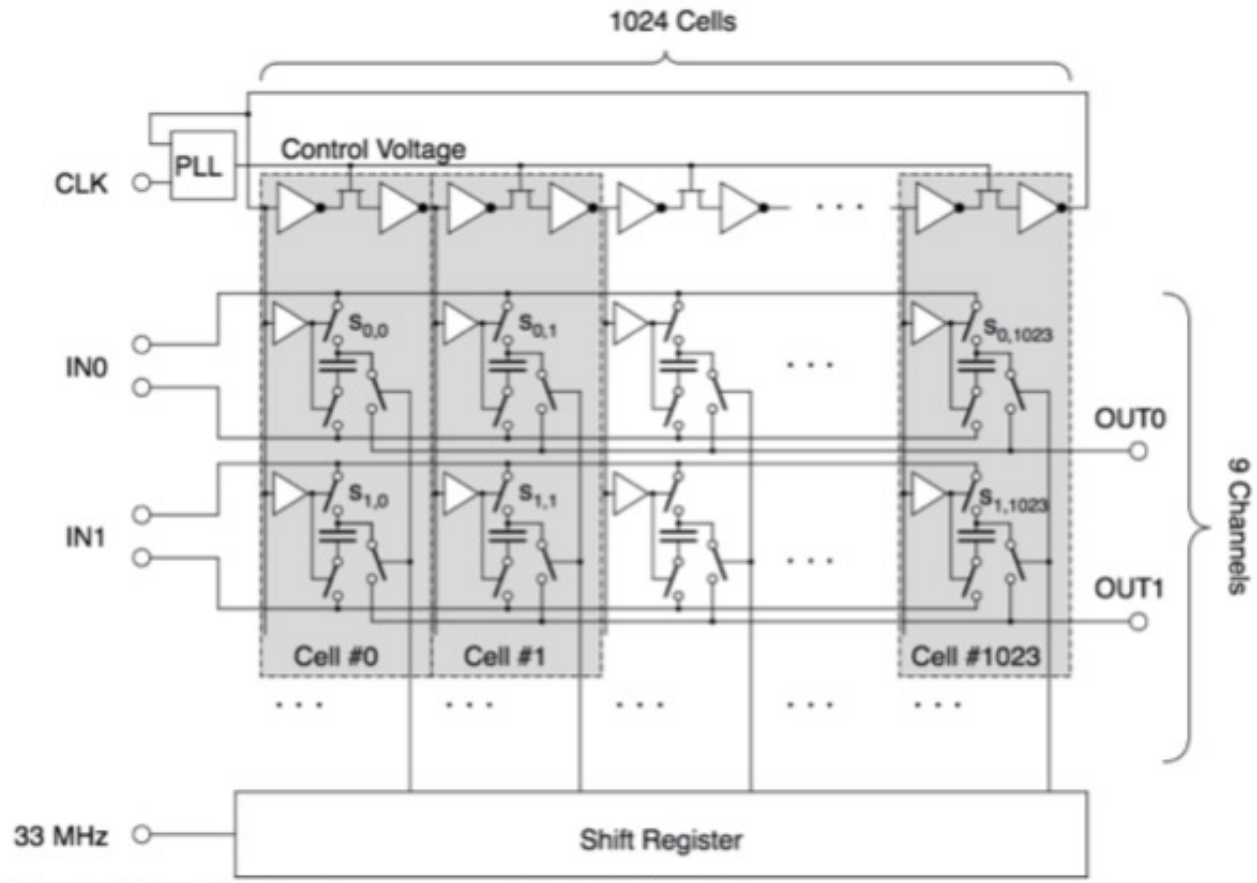


Fig. 1: Simplified schematics of the DRS4 chip.

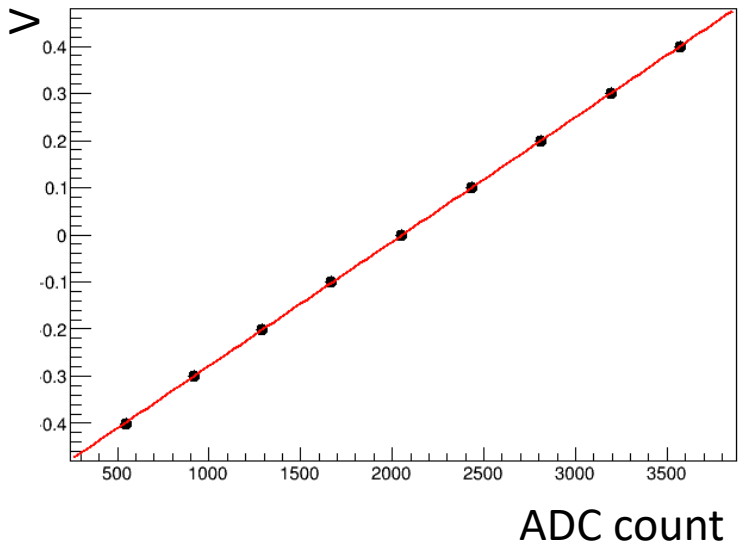
D. Stricker-Shaver *et al.*, *IEEE Trans. Nucl. Sci.* 61 (2014) 3607

DRS4 cell offset calibration

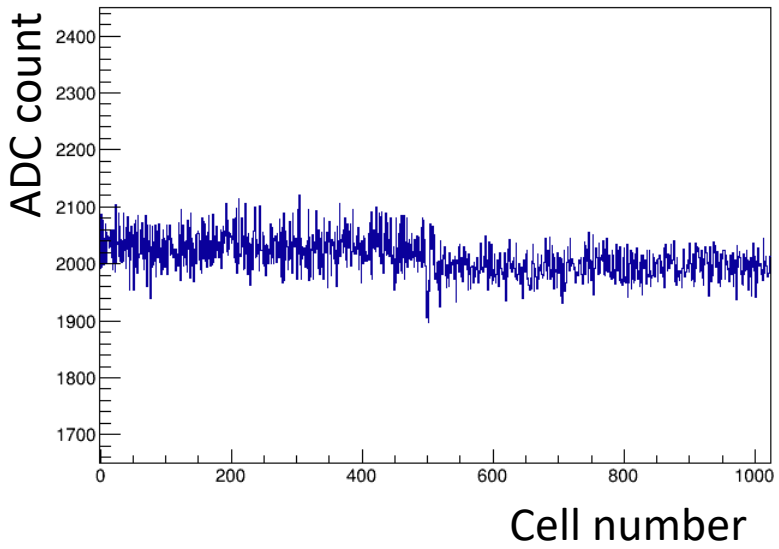
- To calibrate the voltage offsets of each cell we injected into each channel of the board a set of constant voltages, e.g., -0.4V, 0V, +0.4V
  - Three points are already enough
  - The full dynamic range of the DRS4 is 1 V_{pp}
- For each cell a linear fit is performed on voltage as a function of the average ADC counts, and the constants from the fit provide absolute voltage calibration, notably including offset correction

DRS4 cell offset calibration

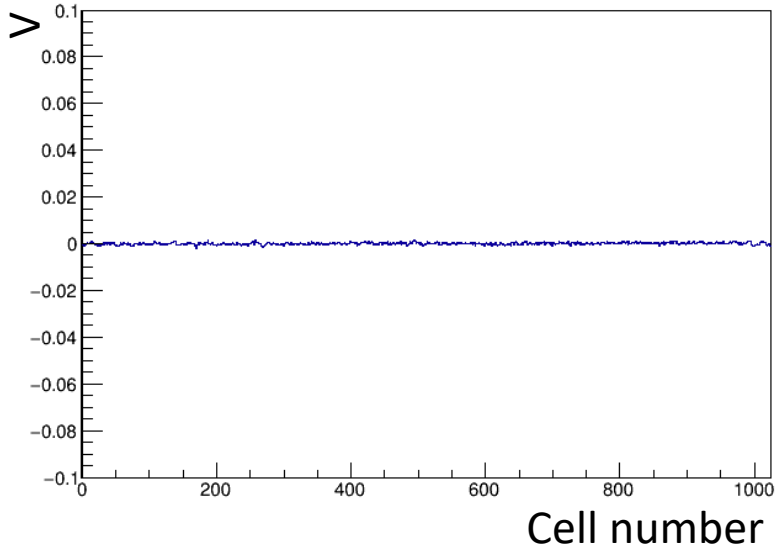
Calibration fit for one cell



Typical 0V line before calibration

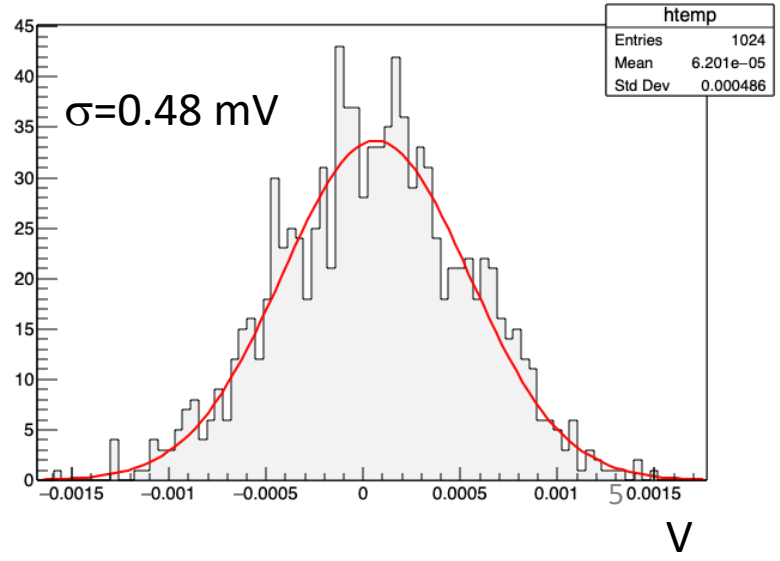


Typical 0V line after calibration



- Residual noise after calibration is about 0.5 mV per cell

Residual noise after calibration

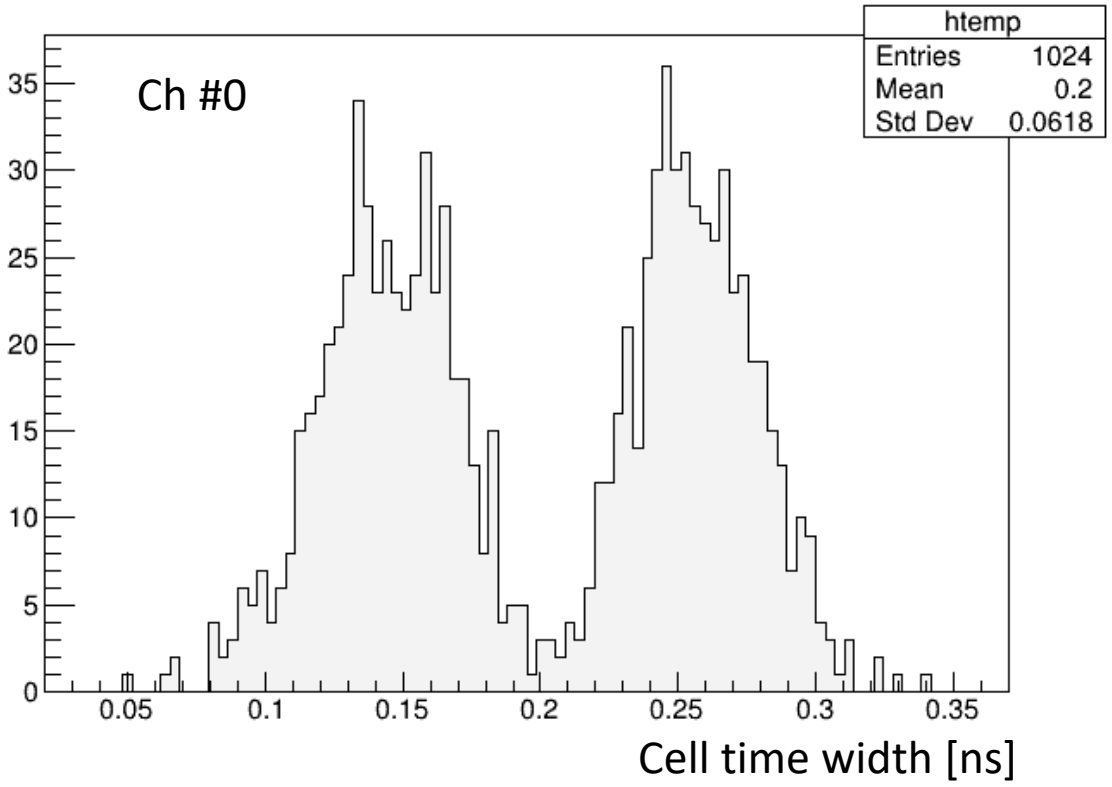


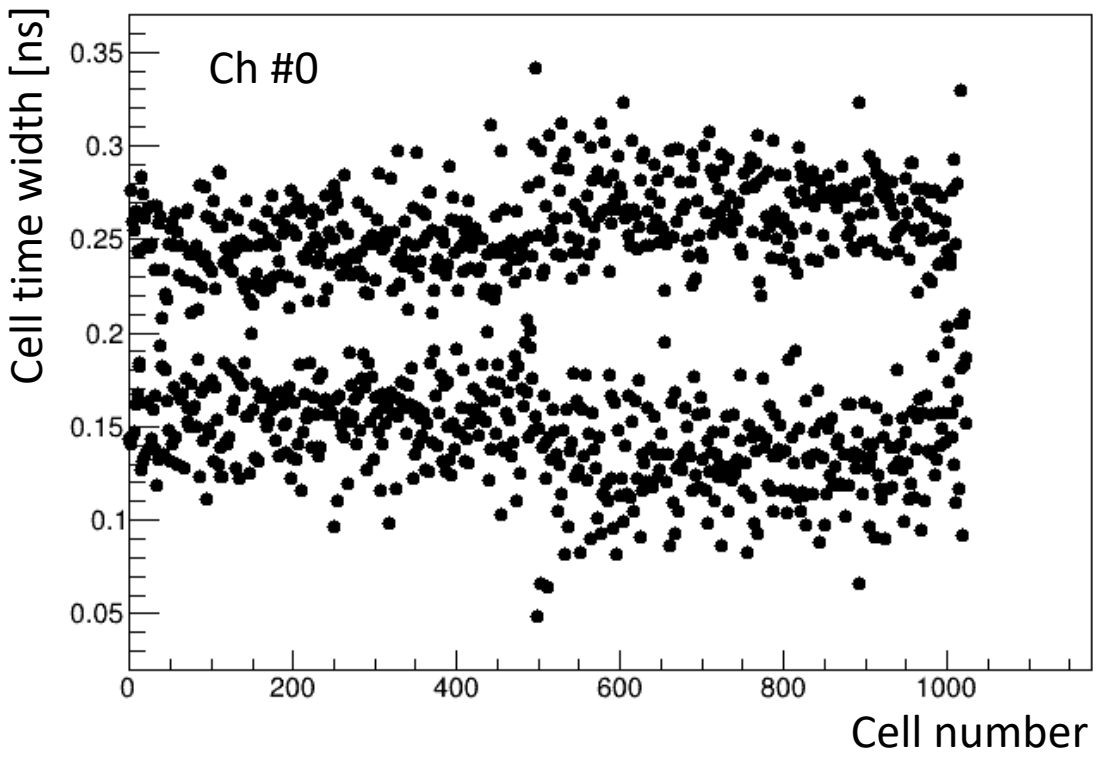
DRS4 cell time-width calibration

- This is more complicated, as one needs to measure the effective time width of every cell
- Basic idea described in D. Stricker-Shaver *et al.*, *IEEE Trans. Nucl. Sci.* 61 (2014) 3607 (same idea described earlier by D. Breton *et al.*)
  - We made an improvement to the technique described in the paper to avoid using an iterative procedure
- The tecnique for time calibration is to inject into the channels of the board 50-100 MHz sine waveform (for 5 GS/s, to be tuned for lower sampling rate) and look for zero crossings
  - Can be done even faster with a triangular waveform, as the linearity allows one to use more points and not only zero crossings, but to reach 100 MHz with triangles one needs a high-ended pulse generator

DRS4 cell time-width calibration

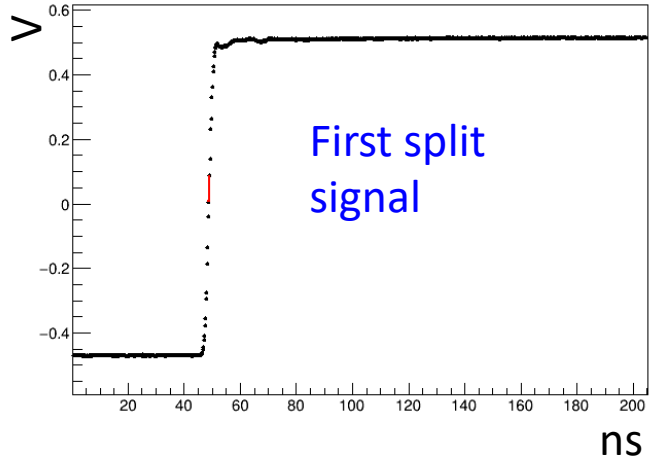
- Odd and even cells for each channel have very different time widths, with large fluctuations
- Plotting the time difference vs cell number, a difference between first 512 cells and the last 512 cells is clearly visible

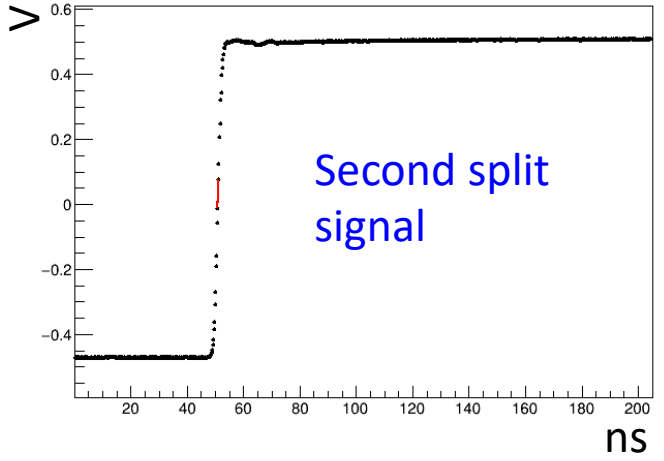


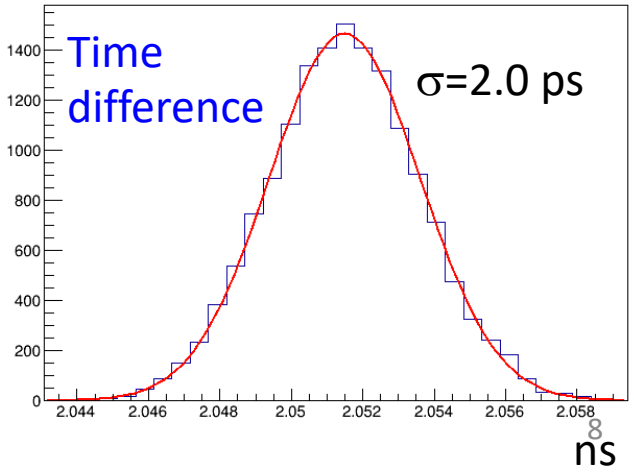


DRS4 calibration tests

- In order to cross-check the time accuracy of the calibration, a signal split test has been performed
- A rising edge is generated via waveform generator, split in two and sent to two distinct channels of the board
  - One of the two signals can be also delayed wrt the other via a longer cable
  - This solution is preferrable to using two synchronised waveform generator outputs to avoid taking care of the generator jitter between the outputs
- A resolution of about 2 ps can be obtained between every pair of channels within a single DRS4 chip
- Syncronization between different DRS4 chips can be used by sharing a common (split) signal on one of the channels, e.g. using the trigger channels

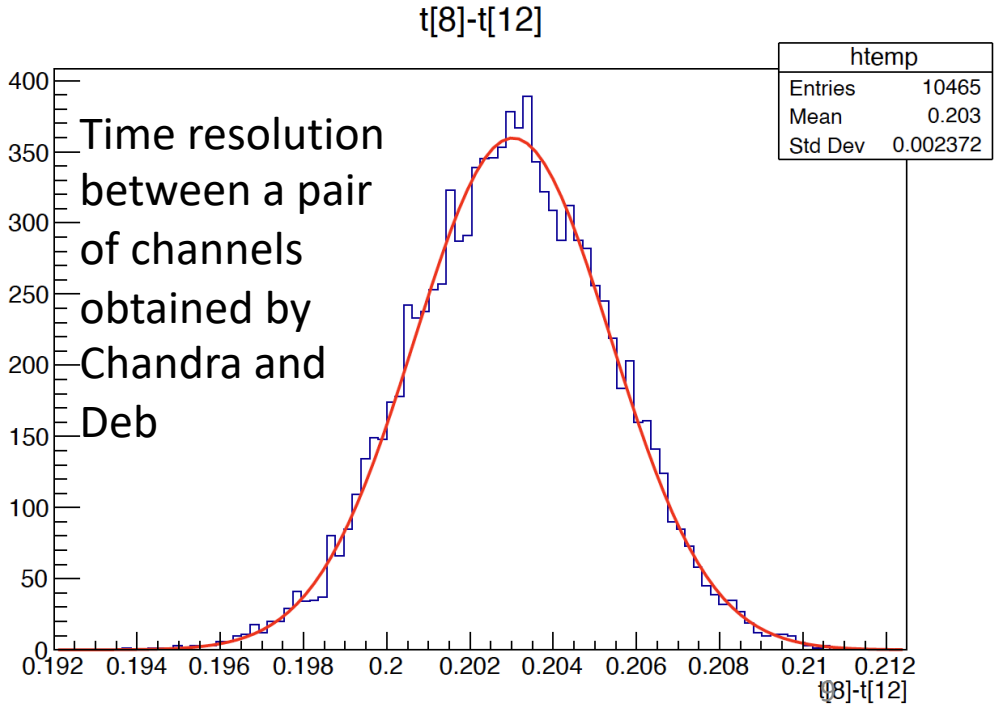




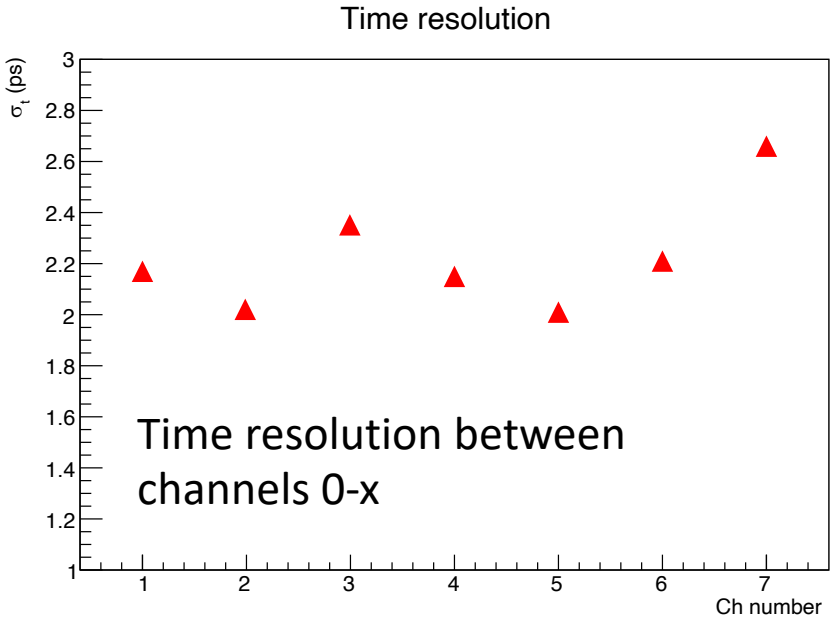


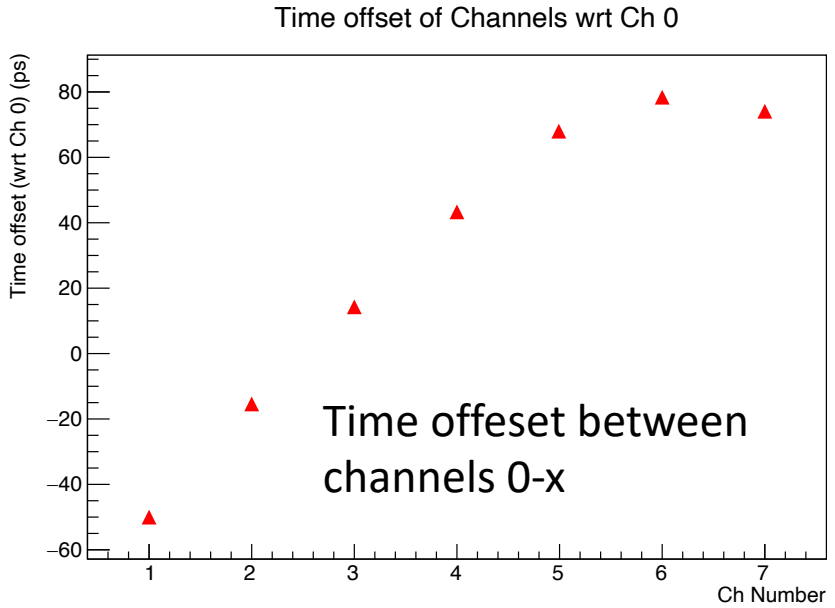
Experience in transferring the knowledge

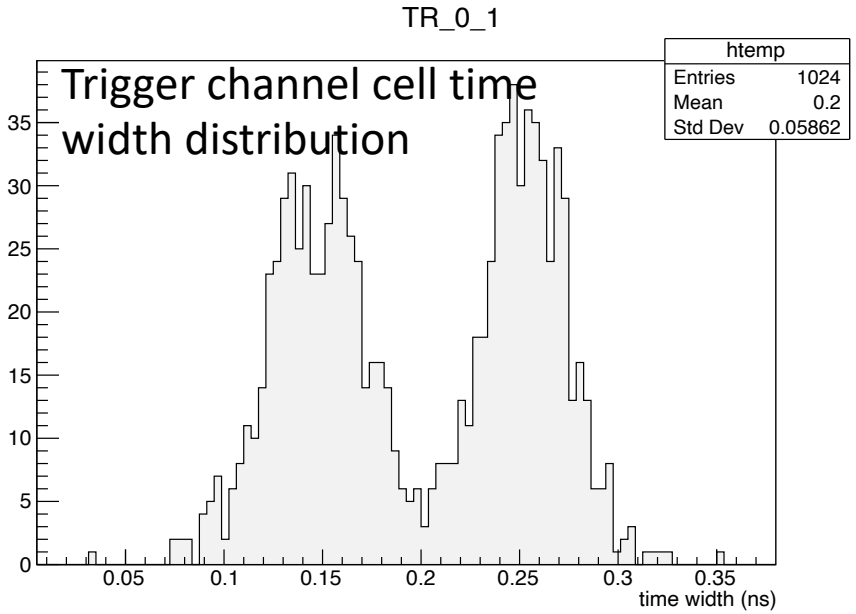
- Chandra and Deb from INFN Trieste came to Bologna last 3-5 April
- Basic tools
  - CAEN v1742 board installed in a minicrate, along with a VME controller read out by a notebook via USB (alternatively, one can use the optical fiber output of the v1742 to read it out)
  - Keysight 33600A pulse generator, two output channels (second output used as trigger signal, but one can also use a different external trigger)
  - ROOT-based software code for producing calibration constants
    - ROOT dependency not essential, can be eliminated relatively easily
- Afternoon of April 3
  - We calibrated together 8 channels (first DRS4 chip) and tested the time resolution between the channels
- Full day April 4
  - Chandra and Deb calibrated by themselves the remaining 24 channels and tested the time resolution within the groups of 8x3 channels
- Morning of April 5
  - Chandra and Deb calibrated the trigger channels and tested the time resolution between the different groups of 8 channels

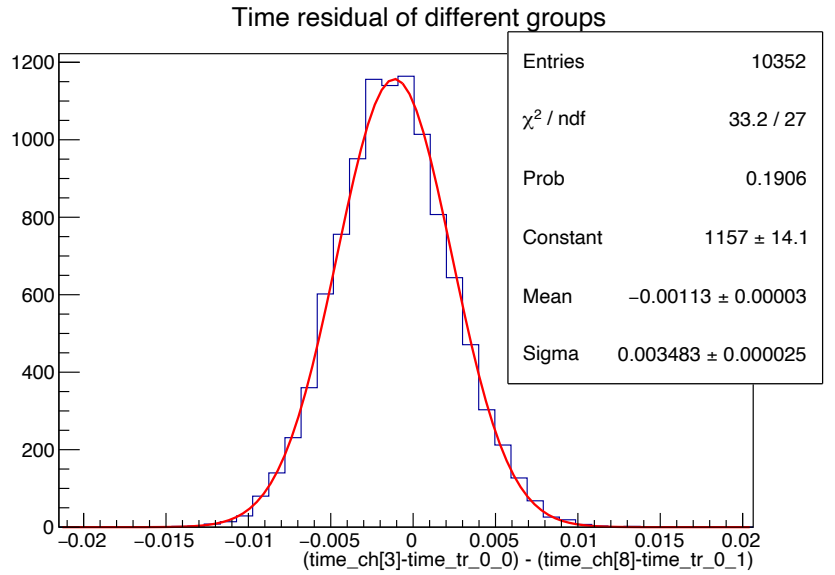


Other plots from Chandra and Deb









Conclusions

- Two full days enough to explain the logic and calibrate all channels of a v1742 CAEN board to about 2-3 ps precision
  - At least with Chandra and Deb, which are very smart guys ;)
- In case one needs to calibrate multiple boards, some automation would be beneficial, but for the moment the calibration procedure and code are not thought for that