Introduction

Newly elected ePIC collaboration spokesperson John Lajoie and deputy Silvia Dalla Torre propose to reorganize the detector efforts within the collaboration as part of their management plan, c.f. https://indico.bnl.gov/event/18482/

Several discussions of this plan with the collaboration have taken place — most recently past Thursday within the Tracking Working Group, c.f. https://indico.bnl.gov/event/18216/

The management plan will be put before the collaboration council upcoming March 24, 2023.

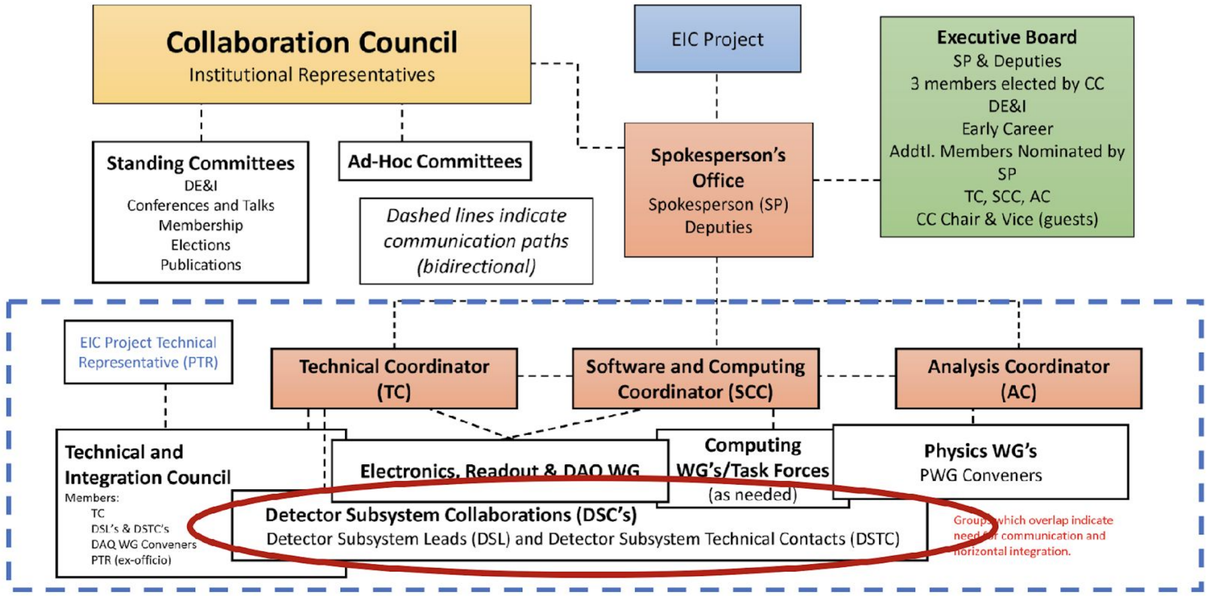
While this plan is thus not finalized, it is timely for us to consider our reaction/response if this plan is adopted. The plan proposes a ~rapid (1-month) and bottom-up approach to forming Detector Subsystem Collaborations with DSC Leads and Technical Contacts,

For this purpose, a DSC is *"a collaboration formed by groups that work together to design, build, and later operate and maintain a detector subsystem."*

Introduction

Collaboration Structure Including the Scientific Structure for the Next Two-Year Term

The matter to be addressed today



- *Need to **evolve DWGs** to a structure more appropriate to the (pre-)TDR/construction phase: **WGs → Detector Subsytems***
- *Each project corresponds to a subdetector built by a **Detector Subsystem Collaboration (DSC)** of the groups and institutions contributing to it*
- *Each project collaboration will choose its **Detector Subsystem Lead (DSL)** and **Detector Subsystem Technical Contact (DSTC)***
- DSL/DSTC (Collab.) <-> L4 Tech. Contacts (Project)

Graphic from past Thursday's Tracking WG meeting, c.f. https://indico.bnl.gov/event/18216/

Topics for discussion today

If the management plan will be adopted,

- **do we want to form a Detector Subsystem Collaboration for the Silicon Vertex Tracker subsystem?**

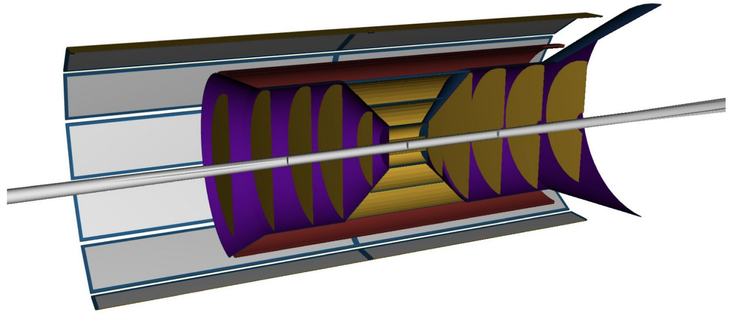
The SVT subsystem is described on the wiki; it is based around a 65nm MAPS sensor and currently consists of five barrel layers (L0—L4), five disks in the hadron-going direction (HD0—HD4), and five disks in the electron-going direction (ED0—ED4).

The **SVT R&D phase** is ongoing. Relevant timelines include:

- EIC vertex sensor qualification in September 2026, concurrent with ALICE-ITS3
- EIC Large Area Sensor production start in February 2027

The **SVT construction phase** will (mostly) follow the R&D phase. Relevant timelines include:

- CD-3, Approve Start of Construction / Execution, is currently anticipated for Spring 2025,
- SVT construction is estimated to take 3—4 years in a technically driven schedule



Topics for discussion today

If we form a Detector Subsystem Collaboration for the Silicon Vertex Tracker,

In the **R&D phase** (— 2027):

- Who will participate?
- Who will do what?
- What resources are available to / within the SVT-DSC?
- What is not covered or missing?

In the **construction phase** (2025 — 2030):

- Who will participate?
- Who will do what?
- What resources are available to / within the SVT-DSC?
- What is not covered or missing?

We started closely related discussions back in October 2022, c.f. https://indico.bnl.gov/event/17418/

Topics for discussion today

Points from past October 10, 2022:

Barrel and Disks will each need:

- Sensors (L0, L1, L2 currently wafer scale similar to ITS3; EIC-LAS elsewhere)
- Mechanical designs
- Cooling
- Power
- Electrical integration
- Cabling strategy

Overall mechanical support and integration of barrel and disks,
Services — cooling, powering, RDO, configuration, and environment
Readout electronics
Interlocks
Slow controls and run control
Power distribution system
DAQ interface

Barrel and disks will have their own assembly structures.

Topics for discussion today

Interests expressed past October 10, 2022 (continued):

Sensor design: RAL, BNL, LBNL
Sensor assembly and testing: INFN, UK, LBNL, LANL, …
Mechanical support — vertex: LBNL, INFN, UK
Mechanical support — sagitta layers: LBNL, ORNL, UK
Mechanical support — disks: LBNL, LANL, UK
Cooling: LBNL, LANL, ORNL
Data cabling: BNL, ORNL
Power distribution: UK, ORNL, LANL, BNL, JLab (?)
Readout: ORNL
DAQ interface: BNL, ORNL
Slow controls:
Interlocks: BNL
Integration: JLab, BNL